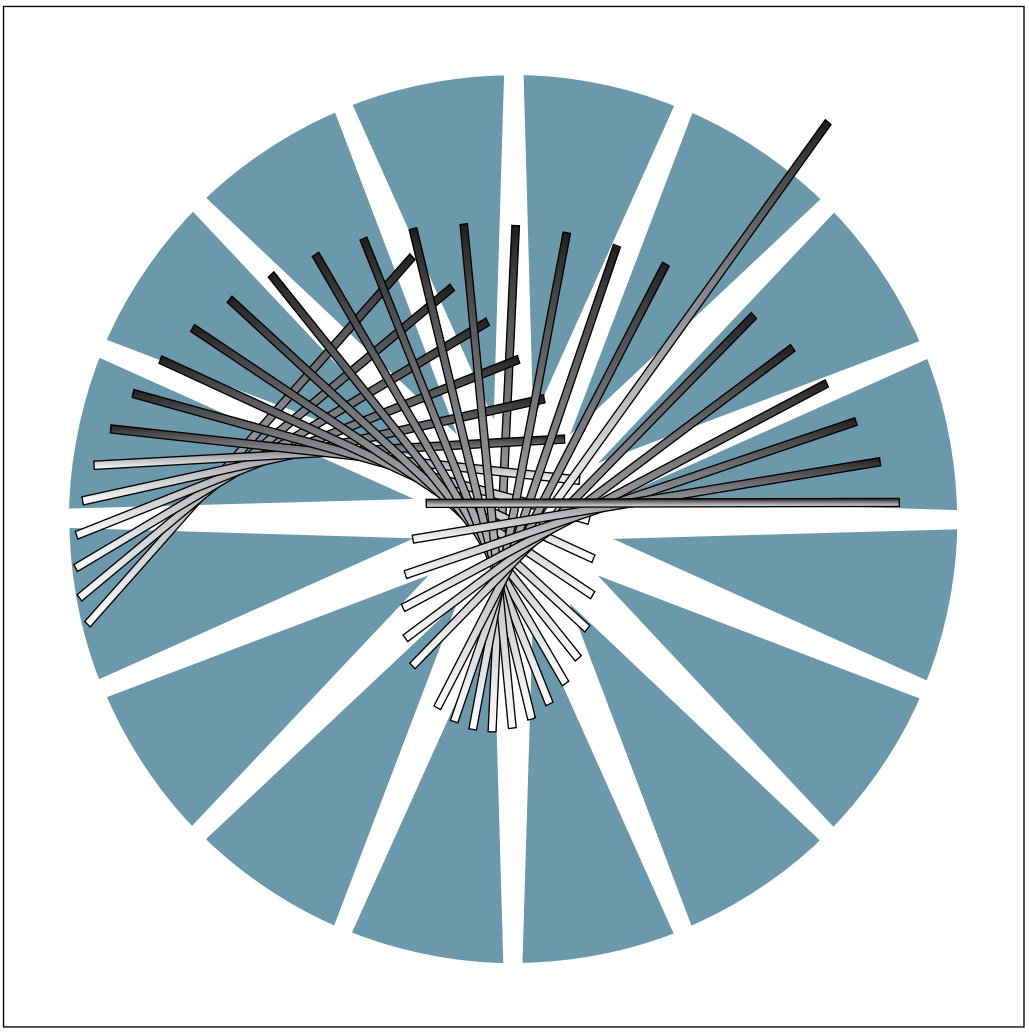
IBM 3745 Communication Controller
Models 210 to 61A

Maintenance Information Reference
Part 1



SY33-2056-8

IBM 3745 Communication Controller
Models 210 to 61A

Maintenance Information Reference
Part 1

SY33-2056-8

Note!

Before using this information and the product it supports, be sure to read the general information under “Notices” on page ix.

Ninth Edition (October 1993)

The information contained in this manual is subject to change from time to time. Any such changes will be reported in subsequent revisions. Changes have been made throughout this edition, and this manual should be read in its entirety.

Order publications through your IBM representative or the IBM branch office serving your locality. Publications are not stocked at the address given below.

A form for readers' comments appears at the back of this publication. If the form has been removed, address your comments to:

IBM France
Centre d'Etudes et Recherches
Service 0798 BP 79
06610 La Gaude
France

- FAX: (33) 93.24.77.97
- EMAIL: FRIBMQF5 at IBMMAIL
- IBM Internal Use: LGERCF at LGEPROFS

When you send information to IBM, you grant IBM a non-exclusive right to use or distribute the information in any way it believes appropriate without incurring any obligation to you.

Contents

Part 1

Part 2

Notices

References in this publication to IBM products, programs or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program, or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, except those expressly designated by IBM, is the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577, U.S.A.

Electronic Emission Notices

Federal Communications Commission (FCC) Statement

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Properly shielded and grounded cables and connectors must be used in order to meet FCC emission limits. IBM is not responsible for any radio or television interference caused by using other than recommended cables and connectors or by unauthorized changes or modifications to this equipment. Unauthorized changes or modifications could void the user's authority to operate the equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Industry Canada Compliance Statement

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Avis de conformité aux normes d'Industrie Canada

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Japanese Voluntary Control Council for Interference (VCCI) Statement

This equipment is Class 1 Equipment (information equipment to be used in commercial and industrial districts) which is in conformance with the standard set by Voluntary Control for Interference by Data Processing Equipment and Electronic Office Machines (VCCI) with an aim to prevent radio interference in commercial and industrial districts. This equipment could cause interference to radio and television receivers when used in and around residential districts. Please handle the equipment properly according to the instruction manual.

情報処理装置等電波障害自主規制協議会
(VCCI)表示

電波障害自主規制届出装置の記述

この装置は、第一種情報装置（商工業地域において使用されるべき情報装置）で商工業地域での電波障害防止を目的とした情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）基準に適合しております。
従って、住宅地域またはその隣接した地域で使用すると、ラジオ、テレビジョン受信機等に受信障害を与えることがあります。

関連マニュアルに従って正しい取り扱いをしてください。

Korean Communications Statement

Please note that this device has been approved for business use with regard to electromagnetic wave interference. If you find this is not suitable for your use, you may exchange it for one designated for non-business purposes.

대한민국 통신문

이 기기는 업무용으로 전자파장해검정을 받은 기기이오니
판매자 또는 사용자는 이 점을 주의하시기 바라며, 만약 잘못
구입하였을 때에는 구입한 곳에서 비업무용으로 교환하시기 바랍니다.

Trademarks and Service Marks

The following terms, denoted by an asterisk (*), used in this publication, are trademarks or service marks of IBM Corporation in the United States or other countries:

ESCON	IBM	LPDA	MVS
NetView	OS/2	PS/2	
RETAIN	VES	VTAM	

Product Safety Information

General Safety

This product meets IBM* safety standards.

For general safety information, see:

- *Telecommunication Products Safety Handbook,* GA33-0126

Safety Notices

See *Safety Notices* located at the beginning of the *Maintenance Information Procedures* manual, SY33-2054.

Service Inspection Procedures

The Service Inspection Procedures helps service personnel check whether the 3745 conforms to IBM safety criteria. They have to be used each time the 3745 safety is suspected.

The *Service Inspection Procedures* section is located at the beginning of the *3745 Maintenance Information Procedures (MIP)* manual.

The 3745 areas and functions checked through service inspection procedures are:

1. External covers
2. Safety labels
3. Safety covers and shields
4. Grounding
5. Circuit breaker and protector rating
6. Input power voltage
7. Power-ON indicator
8. Emergency power OFF.

About This Book

This manual provides:

1. Introductory and how-to-fix information
2. Information for maintaining CSAs (Common Sub-assemblies)
3. Description of IBM 3745 Communication Controller functional units.

The console(s) and operator panel procedures are not provided in this manual, but are provided in the:

- *3745 Advanced Operations Guide*, SA33-0097, and *3745 Service Functions*, SY33-2055, for the maintenance functions used by service personnel.
- *3745 Basic Operations Guide*, SA33-0098, for the control panel functions.

Who Should Use This Book

This manual is intended for the product support-trained CE (PST CE) to service the IBM 3745 Communication Controller whenever the product-trained CE (PT CE) cannot repair the machine using the *Maintenance Information Procedures* (MIP) manual.

The person using this *Maintenance Information Reference* (MIR) manual should:

- Have an understanding of the telecommunications environment.
- Be trained to service the 3745 Communication Controller.
- Be familiar with the data circuit terminating equipment (modems, autocall units, and so on) and the terminals that attach to 3745s.
- Be familiar with the host channel to which the 3745 can be attached.

Service Personnel Definition

See *Maintenance Information Procedures* manual.

How to Use the Maintenance Library

Maintenance on the 3745 is performed only when a failure or suspected failure occurs in the machine. The customer is first expected to perform problem determination to see if a 3745 problem exists. He uses the *Problem Determination Guide* and a host or 3745 console to perform the requested procedures. The problem determination guide generally produces a reference code that the customer should provide to the Hardware Central Service (HCS)

If the HCS is contacted, they will confirm that the initial problem determination has been done correctly, and determine if a hardware failure is indicated. Where hardware replacement is required, the HCS will determine which FRU(s) should be replaced, and dispatch a CE with the information needed to identify and replace them. When replacement has been completed, the CE will test the machine as directed by the *MIP* and *Service Functions* manuals, to verify the repair.

At this point, the *Maintenance Information Procedures* portion of the 3745 Maintenance Library has been exhausted. If additional problem analysis is required, the CE should contact the HCS for assistance, since the problem may require special tools or techniques that are described in the *Maintenance Information Reference* and *Service Functions* manuals, and are applied by a Product Support-Trained CE.

For more details, see "Maintenance Philosophy" in Chapter 1.

Where to Find More Information

See "Bibliography" page X-17.

Summary of Changes

This revised edition gives information concerning the 3745 Models 21A, 31A, 41A, 61A and the 3746 Model 900 connection.

This revised edition also gives information on 3746-900 expansion enclosure and new 3746-900 line processor (CLP) and line couplers (LIC type 11 and LIC type 12).

This edition also corrects minor errors or omissions.

Part 1

Part 1 contains Chapters 01 to 06, the Abbreviation list, Glossary, and Index.

Chapter 1. General Information

Introduction

Controller Organization

The IBM 3745 communication controller is composed of a:

- Control subsystem (CSS)
- Transmission subsystem (TSS), and/or a token-ring subsystem (TRSS), and/or a high performance transmission subsystem (HPTSS) and/or Ethernet subsystem (ESS)
- Maintenance and operator subsystem (MOSS)
- Power control subsystem (PCSS).

A 3746 Model 900 can be connected to the 3745 via the DMA and IOC buses.

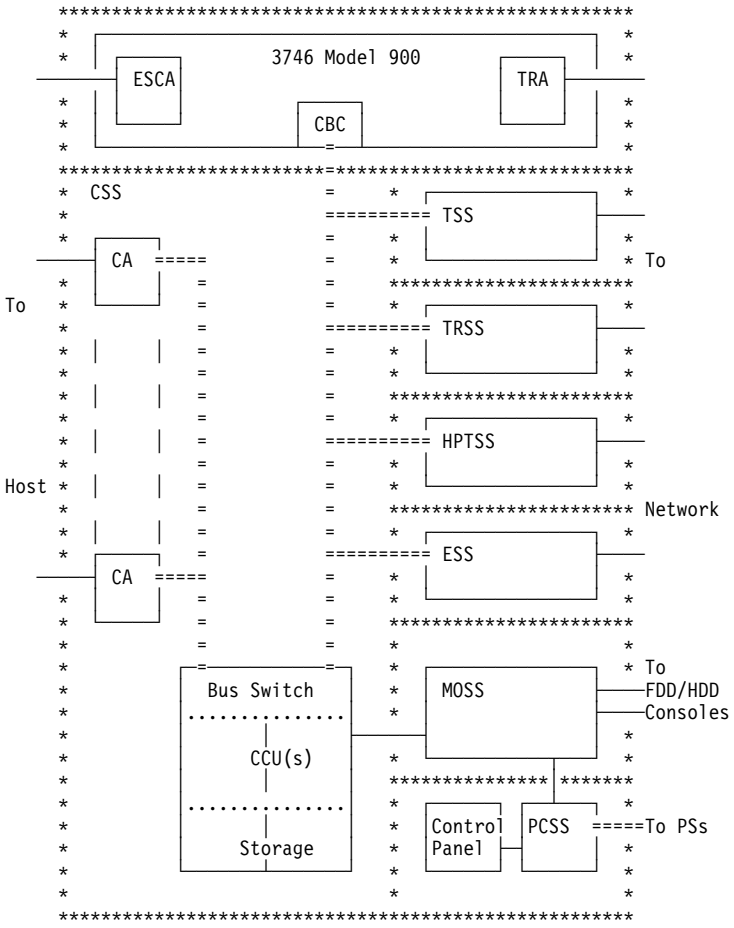


Figure 1-1. Controller Organization

Control Subsystem

The control subsystem (CSS) controls data transfer through the channel interface and executes the control program (NCP, or PEP).

See Figure 1-2 on page 1-7.

It is composed of the central control unit (CCU) with its associated storage (STO), up to eight megabytes, and storage control (SCTL) with the IOC bus switch (IOSW), and the DMA bus switch (DMSW) for direct memory access (DMA), if the HPTSS is installed.

On 3745 Models 31A and 61A a 16 MB storage feature is available. This 16 MB storage is part of a new SCTL3.

Two CCUs can be installed to obtain more availability or better performances.

For more details on the CCU, see Chapter 2, “Central Control Unit (CCU).”

Each CCU controls its associated adapters via two IOC buses, and one DMA bus. A bus switch allows attaching all the adapters to one CCU or to the other, or attaching one group of adapters to one CCU and the remaining group to the other CCU.

For more details on the buses and bus switch, see Chapter 3, “Buses and Bus Switching.”

Channel Adapter: The channel adapters (CA) are part of the control subsystem.

Each channel adapter is composed of a channel adapter logic card (CAL), and a channel adapter driver receiver card (CADR).

Two types of channel adapter are available:

- Channel adapter type 6: Channel adapter data streaming (CADS)
- Channel adapter type 7: Buffer chaining channel adapter (BCCA).

For more details on the channel adapter, see Chapter 7, “Channel Adapter (CA).”

Transmission Subsystem

The transmission subsystem (TSS) includes up to 32 low-speed scanners (LSS), also called line adapters (LA). One LSS is composed of a communication scanner processor (CSP) and a front-end low-speed scanner (FESL). This LSS is associated with a multiplex card (DMUX or SMUXA/B).

One DMUX controls up to eight line interface couplers (LICs).
One SMUXA controls up to 16 line interface couplers (LICs).
One SMUXB controls up to eight line interface couplers (LICs).

Three types of LIC, LICs type 1, 3, and 4 are attached to the DMUX card.

Two types of LIC, LICs type 5 and 6 are attached to the SMUXA card or SMUXB card. LICs 5 and 6 have the DCE function integrated along with the DTE function.

Configuration Flexibility: The interconnection between the FESL and the DMUX or the SMUXA/B depends on the machine's configuration.
Any FESL card can be connected to any DMUX or SMUXA/B card.

See Figure 1-2 on page 1-7.

For more details on the transmission subsystem, see Chapter 4, “Transmission Subsystem (TSS).”

Token-Ring Subsystem

The token-ring subsystem (TRSS) includes up to four token-ring adapters (TRAs). The TRA is composed of one token-ring multiplexor card (TRM), and two token-ring interface couplers (TICs).

The TRA occupies one CSP address position, and allows attaching two token-rings via TIC cards.

Two types of TIC are available on the 3745:

- TIC type 1 (TIC1) attaches a token-ring operating at 4 Mbps only.
- TIC type 2 (TIC2) attaches a token-ring operating at 4 or 16 Mbps.

See Figure 1-2 on page 1-7.

For more details on the token-ring subsystem, see Chapter 5, “The Token-Ring Subsystem.”

High Performance Transmission Subsystem

The high performance transmission subsystem (HPTSS) includes up to eight high-speed scanners (HSS), also called line adapters (LA). One HSS is composed of a communication scanner processor (CSP) and a front-end high-speed scanner (FESH). The FESH interfaces with main storage via a DMA bus.

The HSS can be installed in all 3745 models in the ELA positions.

Lines cables are connected directly to the FESH card, via the tail gate.

See Figure 1-2 on page 1-7.

For more details on the high performance transmission subsystem, see Chapter 6, “High Performance Transmission Subsystem (HPTSS).”

Ethernet Subsystem

The Ethernet subsystem (ESS) includes up to eight Ethernet LAN adapters (ELA), also called line adapters (LA). One ELA is composed of a communication scanner processor (CSP) and an Ethernet adapter card (EAC). The EAC interfaces with main storage via a DMA bus.

The ELA can be installed in all 3745 models in the HSS positions.

Lines cables are connected directly to the EAC card, via the tail gate.

See Figure 1-2 on page 1-7.

For more details on the Ethernet subsystem, see Chapter 14, “Ethernet Subsystem (ESS).”

Interfaces

The communication controller interfaces with the user network via the transmission interface. The communication controller interfaces with the host processor(s) via the channel interface.

Maintenance and Operator Subsystem

The maintenance and operator subsystem (MOSS) provides the operating and service facilities to the customer's operator and to the customer engineer (CE).

The MOSS consists a processor and storage, a flexible diskette drive (FDD), a hard disk drive (HDD), their adapter (DFA), and a connection to the consoles through:

- A MOSS console adapter card (MCA) on 3745 Models 210-610
- A MOSS LAN adapter card (MLA) on 3745 Models 21A-61A.

See “Console Summary” on page 1-8 for consoles attached to the 3745.

The interconnection with the CCU is performed through a MOSS adapter card (MAC).

The interconnection with the control panel and the power control is performed through a power logic card (PLC).

See Figure 1-2 on page 1-7.

For more details on the MOSS, see Chapter 8, “Maintenance and Operator Subsystem (MOSS).”

For more details on the control panel and consoles, see Chapter 9, “Control Panel, Operator Consoles, Disk/Diskette Drives.”

Power Control Subsystem

The power control subsystem (PCSS) is basically made of a power logic card (PLC) and a power analog card (PAC). The PLC card is linked to the secondary power control card of each power supply via a power control bus (PCB). The PLC also links the control panel to the MPC card of the MOSS.

The PAC card generates the power analog signals.

See Figure 1-2 on page 1-7.

For more details on the power control subsystem, see Chapter 10, “3745 Power System.”

3746 Model 900 Connectivity Switch

The 3746-900 is a frame connected to the 3745 Models 21A, 31A, 41A, and 61A. This frame is installed at the 3746 A11 or A12 frame location or in addition against the frame A12 according to the 3745 configuration.

The 3746-900 provides new adapters to the 3745 to attach:

- Enterprise Systems Connection (ESCON*) channel
- TIC3 couplers (4 or 16 MBps).
- LIC type 11 (up to 256 kbps)
- LIC type 12 (up to 2 Mbps)

A new MOSS hardware and microcode for connection to the service processor, via the LAN, is installed on the 3745 models 21A-61A. The service processor (PS/2 based) is used as 3745 MOSS console.

For more details on the 3746-900, refer to the soft copy manual: *3746 Model 900 Hardware Maintenance Reference.*

3745 Data Flow

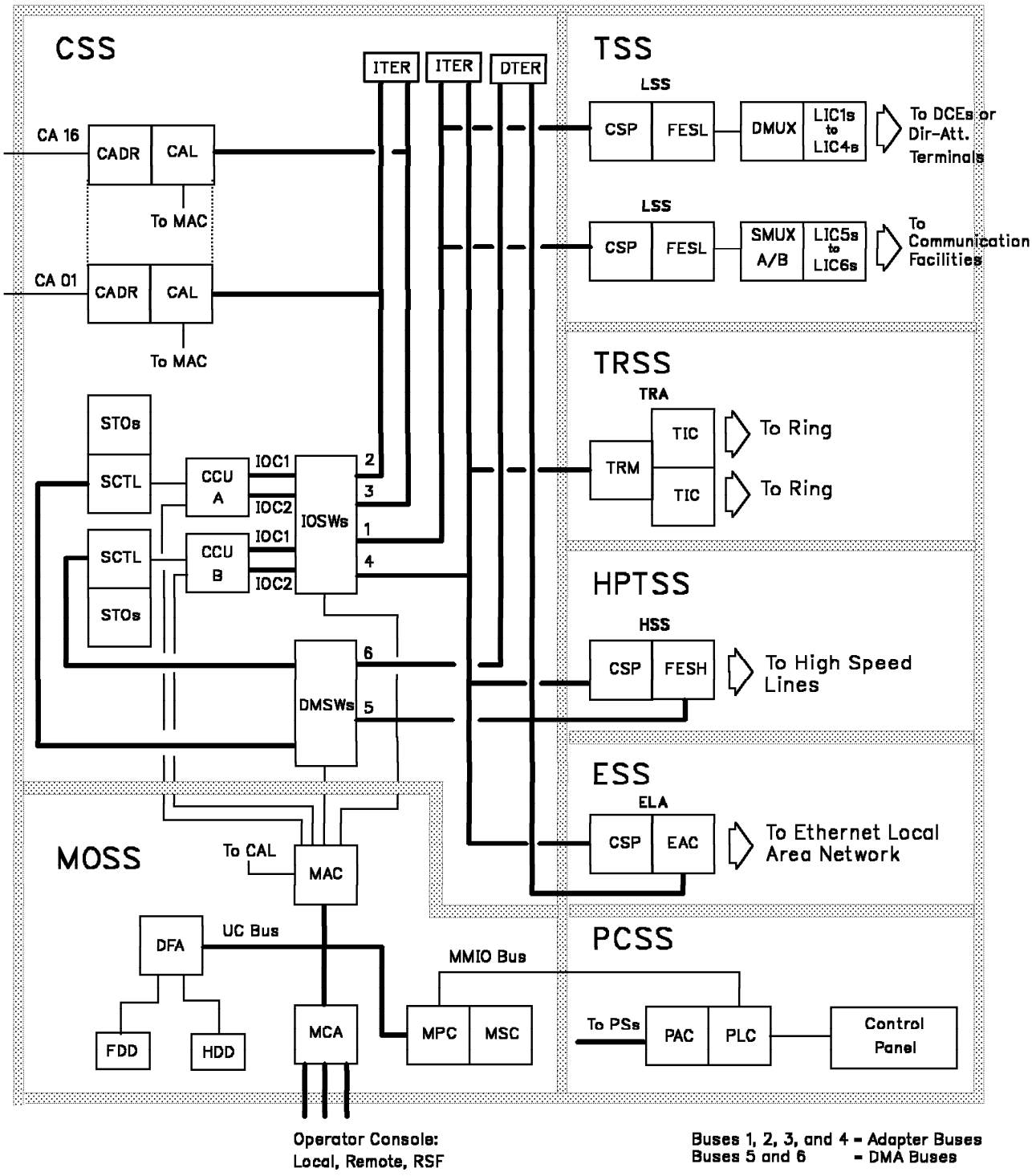
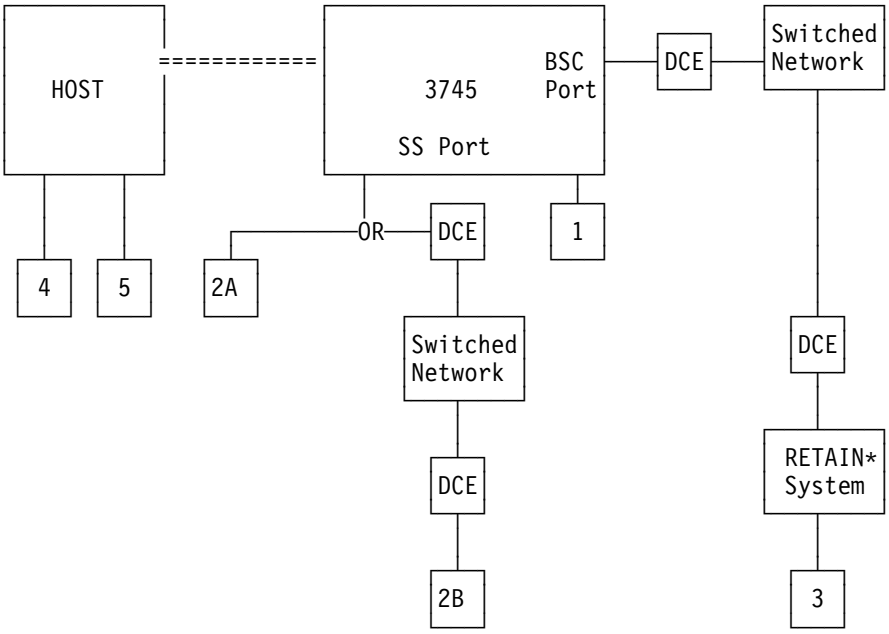


Figure 1-2. 3745 Data Flow. For models 21A-61A, DMA and IOC buses are connected to the CBC in the 3746-900. The MCA card is replaced by the MLA card which interfaces to the MPC card through the MMIO bus. This MLA card links the MOSS to the Service Processor through a LAN.

Console Summary

Console Summary for Models 210-610



1. Local console (mandatory)

2A. Alternate console (direct-attached within 120 meters)

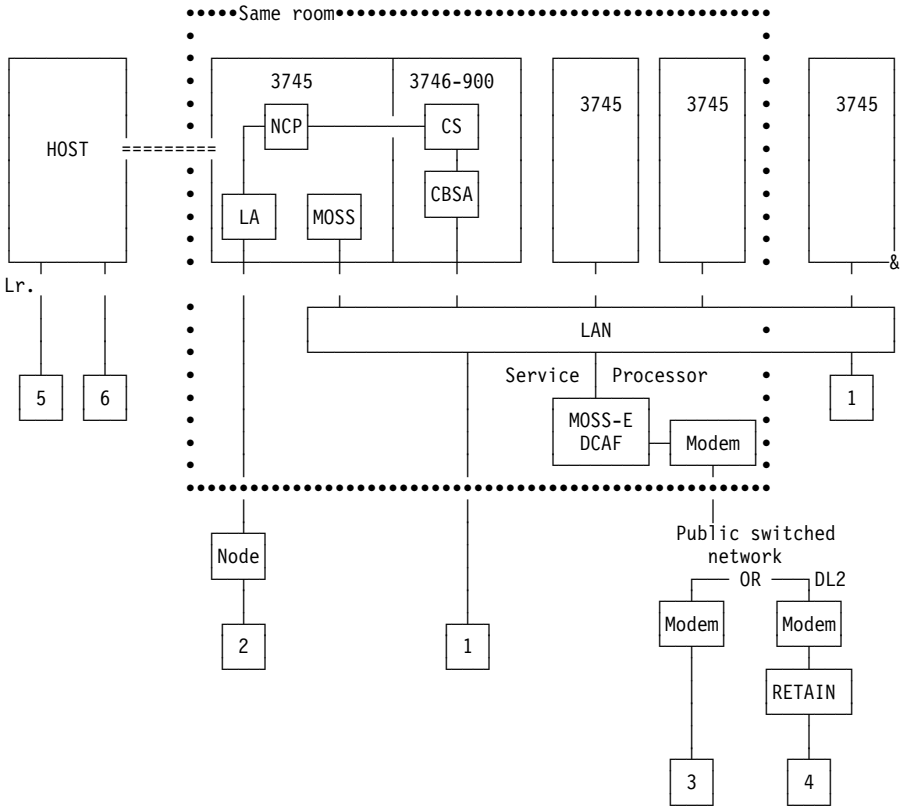
2B. Remote console

3. IBM RSF console

4. Access method console

5. NetView* console.

Console Summary for Models 21A-61A



1. LAN attached console (OS/2 with DCAF)
2. Remote console via user network (PS/2 with DCAF). See Note.
3. RSF console via PSN (OS/2 with DCAF)
4. RETAIN console
5. Access method console
6. NetView console.

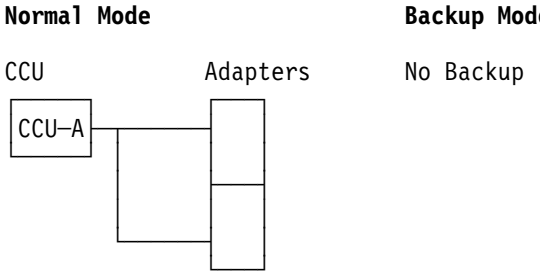
Note: If no 3746-900 is installed the service processor must be connected to the 3745 through a TIC2 for the use of the remote console.

Modes of Operation

The 3745 can be equipped with one or two CCUs. Each CCU is connected to two IOC buses and one DMA bus if HPTSS is installed. These buses can be switched from one CCU to the other under MOSS control, and provide the following modes of operation:

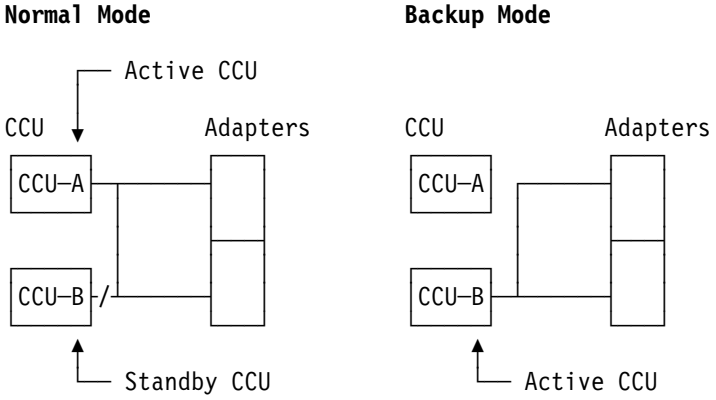
1. Single

   A single CCU is installed. All IOC buses are connected to this CCU. No possibility of backup.



2. Twin standby

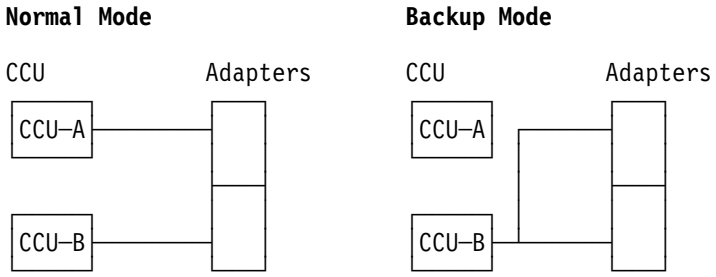
   Two CCUs are installed. One CCU is active, and the other is in standby, ready to take over if the active CCU fails. If one CCU is failing there is therefore no performance or network degradation.



3. Twin backup

   The two CCUs are simultaneously operational, each controlling part of the network.

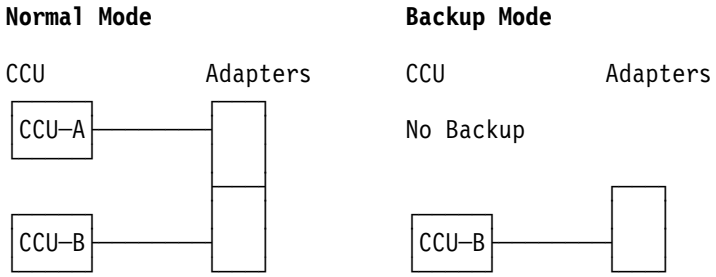
   If one CCU fails the other CCU takes over the entire resources, with a possible reduction of performances.



4. Twin dual

   The two CCUs are simultaneously opreational, each controlling part of the network. There is no provision for an automatic bus switching and so if one CCU fails a part of the network is lost.

   This mode of operation can be considered as operating two different machines in the same box.



Machine Identification and Capacity

3745-210 or 310 (Base Frame or Frame 01)

- One CCU.
- Up to eight line adapters (LSS, HSS, or ELA).
- Up to 128 lines (speed up to 256 kbps), or
- Up to eight high-speed lines (speed up to 2 million bps), or
- Up to 16 Ethenet lines (speed up to 10 million bps), or
- Up to four token-ring adapters (eight token-rings), via four token-ring multiplexers.
- Up to eight channel adapters (CA), or
- Up to four CAs with four TPSs (two-processor switches).
- Four or eight megabytes of storage.
- Console attachments.

3745-410 or 610 (Base Frame or Frame 01)

Same as the 3745-210 or 310 with two CCUs installed.

3746-A11 (Frame 02)

- Up to 16 line adapters (LSS)
- Up to eight channel adapters,
- Or up to four CAs with four TPSs (two-processor switches).

3746-A12 (Frame 03)

- Up to eight line adapters (LSS).

3746-L13 (Frame 04)

- Up to 256 lines.

3746-L14 (Frame 05)

- Up to 256 lines.

3746-L15 (Frame 06)

- Up to 256 lines.

3745 21A, 31A, 41A, and 61A

These models have the equivalent capacity to models 210 to 610. They have a service processor for console and can have an additional 3746 Model 900 frame 07 connected with the capacity of:

- Up to 10 ESCON channels or
- Up to 21 token ring couplers or
- Up to 21 LIC type 11 or LIC type 12.

The 3745 models 31A and 61A can have up to 16 megabytes storage.

Starting EC D55657 (from machine serial number 57-45xxx) on 3745 Models 21A and 41A, the TCM is replaced by a PUC type 1 (PUC1) card.

3745 Model Identification

Following models are available:

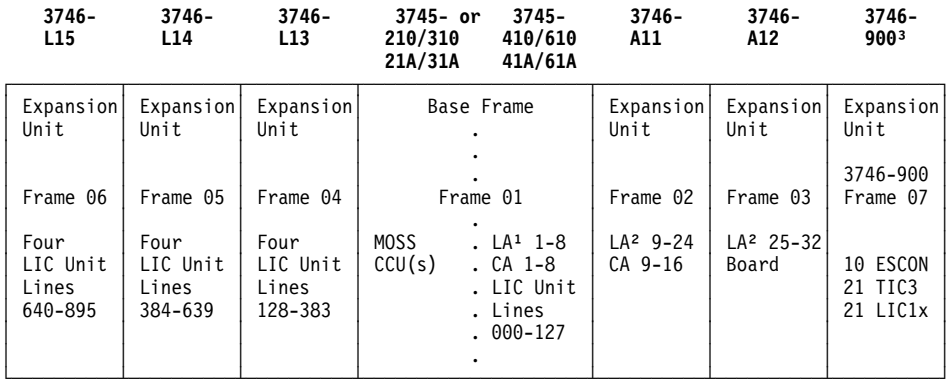
1. Model 210: 3745 equipped with only one CCU, TCM type (thermal conduction module).
2. Model 310: 3745 equipped with only one CCU, PUC type (processor unit card).
3. Model 410: 3745 equipped with two CCUs, TCM type (thermal conduction module).
4. Model 610: 3745 equipped with two CCUs, PUC type (processor unit card).
5. Models 21A to 61A: Equivalent to models 210 to 610 with an additional 3746-900 frame.

Basic Configuration (Minimum Configuration)

Feature	Model	Quantity	Location
4 MB storage	21x	1	01B-A1 E0
	31x	1	01B-A1 B0
	41x	2	01B-A1 E0 and 01B-A1 RO
	61x	2	01B-A1 B0 and 01B-A1 UO
LSS adapter	ALL	2	In board 01G-A1
LIC Unit (LIB1)	ALL	1	01P
LIC type 1, 3, 4A, or 4B	ALL	8	First 8 LICs installed in the 3745

Frame Locations

- Frame 01 (3745 all models) for base frame
- Frame 02 (3746-A11) for an extension of up to 16 LAs (LSS) and eight channel adapters
- Frame 03 (3746-A12) for an extension of up to eight LAs (LSS)
- Frame 04 (3746-L13) for an extension of up to 256 lines.
- Frame 05 (3746-L14) for an extension of up to 256 lines.
- Frame 06 (3746-L15) for an extension of up to 256 lines.
- 3746-900 frame 07 for an extension of up to 10 ESCON channels or up to 21 token ring lines or up to 21 LIC type 11 or LIC type 12.



¹ = LSS, HSS, ELA, or TRA
² = LSS only
³ = 3746-900 frame can also be installed in place of 3746-A11 or -A12 but must be the last frame.

Figure 1-3. Frame Locations (Front View)

Base Frame, Frame 01 Component Locations

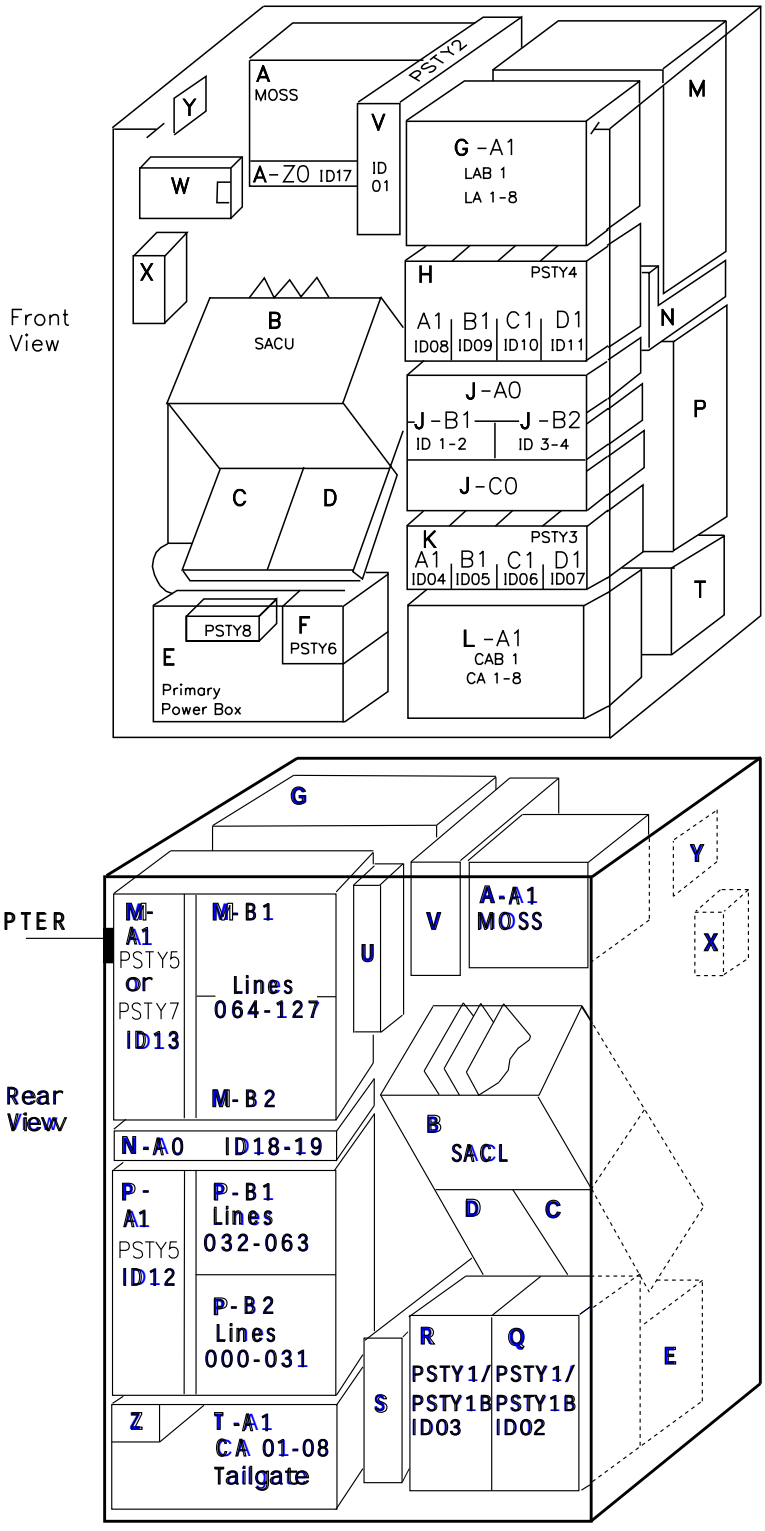


Figure 1-4. Base Frame, Frame 01 Component Locations

A MOSS board and fan
See Chapter 8, “Maintenance and Operator Subsystem (MOSS)” on page 8-1, or “Power Supply Type 2 (PS Type 2)” on page 10-15 for details.

B CCUs control board: See Chapter 2, “Central Control Unit (CCU)” on page 2-1.

C CCU-A for models 21x and 41x: See Chapter 2, “Central Control Unit (CCU)” on page 2-1.

D CCU-B for model 41x: See Chapter 2, “Central Control Unit (CCU)” on page 2-1.

E Primary power box and PS type 8
See “Power Supply Type 8 (PS Type 8)” on page 10-37 for PS type 8.

F PS type 6, PS for power supplies control
See “Power Supply Type 6 (PS Type 6)” on page 10-30.

G Line adapter board (LSS, TRA, HSS, ELA)
See Chapter 4, “Transmission Subsystem (TSS)” on page 4-1, or Chapter 5, “The Token-Ring Subsystem” on page 5-1, or Chapter 6, “High Performance Transmission Subsystem (HPTSS)” on page 6-1.
Chapter 14, “Ethernet Subsystem (ESS)” on page 14-1.

H PS type 4, up to four PS, one PS for two LAs
See “PS Type 4 Frame 01 Connection Layout” on page 10-21.

J AC and DC distribution
See page YZ511.

K PS type 3, up to four PS, one PS for two CAs
See “PS Type 3 Frame 01 Connection Layout” on page 10-18.

L Channel adapter board (CAs 01 to 08)
See Chapter 7, “Channel Adapter (CA)” on page 7-1.

M LIC unit (from line 64 to line 127 for LICs 1-4, or line 64 to line 95 for LICs 5-6)
See Chapter 4, “Transmission Subsystem (TSS)” on page 4-1,
or “PS Type 5 Frame 01 Connection Layout” on page 10-26 for PS type 5 details,
or “PS Type 7 Frame 01 Connection Layout” on page 10-33 for PS type 7 details.

N Fan for LIC unit
See “PS Type 5 Frame 01 Connection Layout” on page 10-26 for PS type 5 details, or “PS Type 7 Frame 01 Connection Layout” on page 10-33 for PS type 7 details.

P LIC unit (from line 00 to line 63 for LICs 1-4)
See Chapter 4, “Transmission Subsystem (TSS)” on page 4-1,
or “PS Type 5 Frame 01 Connection Layout” on page 10-26 for PS type 5 details.

Q PS type 1 or 1B, PS for CCU-A.
See "Power Supply Type 1/1B" on page 10-10 or 10-13.

R PS type 1/1B, PS for CCU-B.
See "Power Supply Type 1/1B" on page 10-10 or 10-13.

S Host cable (EPO) connector tail gate.
See pages YZ043 and YZ543.

T Channel adapters 01 to 08 tail gate.
See Chapter 7, “Channel Adapter (CA)” on page 7-1.

U HSS/ELA/TRA tail gate, console and customer power control connectors.
See Chapter 6, “High Performance Transmission Subsystem (HPTSS)” on page 6-1, or Chapter 5, “The Token-Ring Subsystem” on page 5-1, or Chapter 9, “Control Panel, Operator Consoles, Disk/Diskette Drives” on page 9-1. Chapter 14, “Ethernet Subsystem (ESS)” on page 14-1.

V PS type 2, PS for MOSS. See “Power Supply Type 2 (PS Type 2)” on page 10-15.

W Control panel and FDD
See Chapter 9, “Control Panel, Operator Consoles, Disk/Diskette Drives” on page 9-1.
or “Disk and Diskette Drive ON/OFF Control” on page 10-38 for details on the power supply.

X HDD
See Chapter 9, “Control Panel, Operator Consoles, Disk/Diskette Drives” on page 9-1, or “Disk and Diskette Drive ON/OFF Control” on page 10-38 for details on the power supply.

Y Auxiliary connector
See page YZ051.

Z Auxiliary power box
See pages YZ051 and YZ551.

Adapter Frame, Frame 02 Component Locations

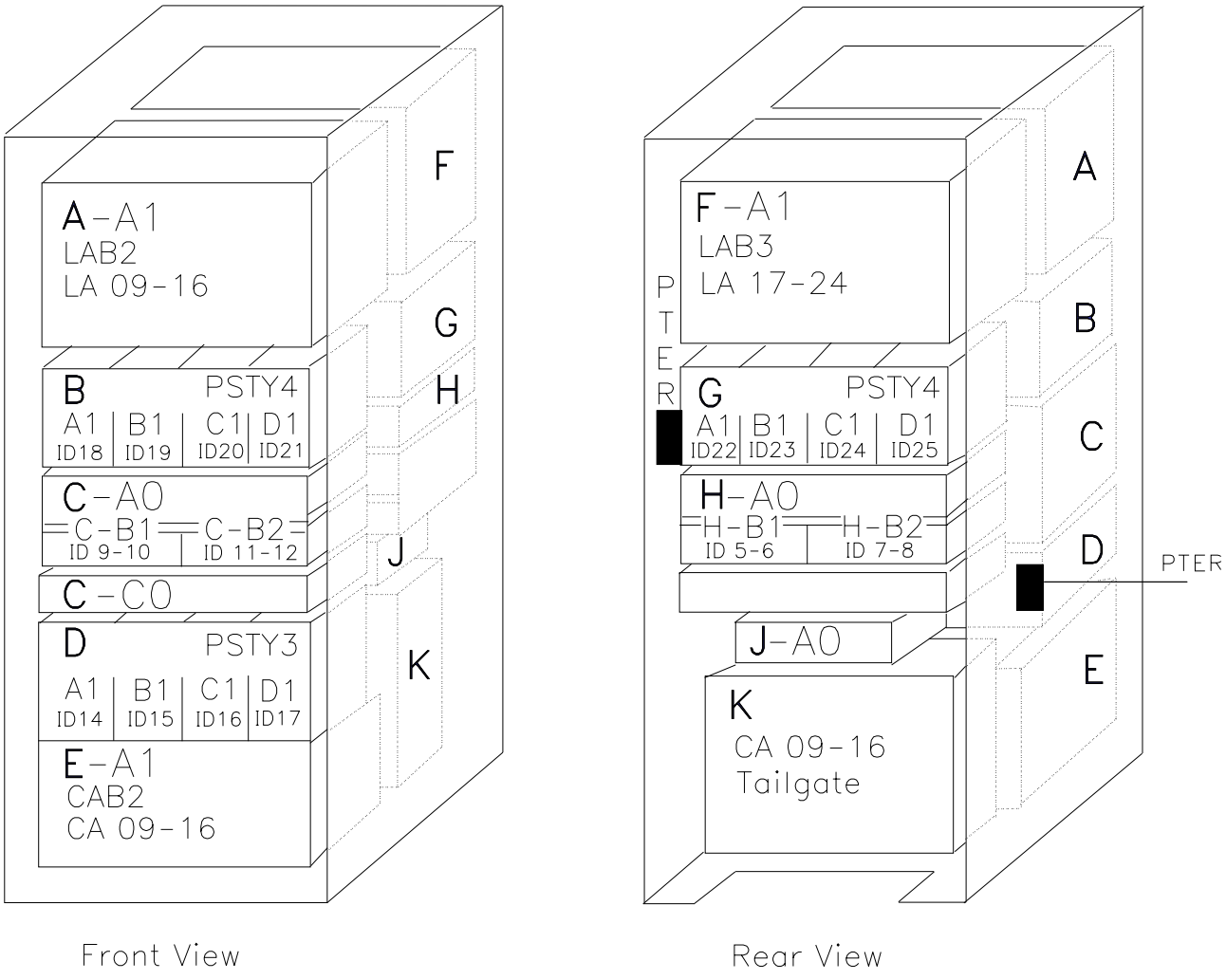


Figure 1-5. Adapter Frame, Frame 02 Component Locations

A Line adapter board (LA 09 to 16)
See Chapter 4, “Transmission Subsystem (TSS)” on page 4-1.

B PS type 4, up to four PS, one PS for two LAs
See “PS Type 4 Frame 02 Connection Layout” on page 10-21.

C AC and DC distribution
See page YZ511.

D PS type 3, up to four PS, one PS for two CAs
See “PS Type 3 Frame 02 Connection Layout” on page 10-18.

E Channel adapter board (CAs 09 to 16)
See Chapter 7, “Channel Adapter (CA)” on page 7-1.

F Line adapter board (LA 17 to 24)
See Chapter 4, “Transmission Subsystem (TSS)” on page 4-1.

G PS type 4, up to four PS, one PS for two LAs
See “PS Type 4 Frame 02 Connection Layout” on page 10-21.

H AC and DC distribution
See page YZ512.

J Auxiliary power box
See “Auxiliary Power Box Frame 02 (02J-A0)” on page 10-8.

K Channel adapters 09 to 16 tail gate
See Chapter 7, “Channel Adapter (CA)” on page 7-1.

Adapter Frame, Frame 03 Component Locations

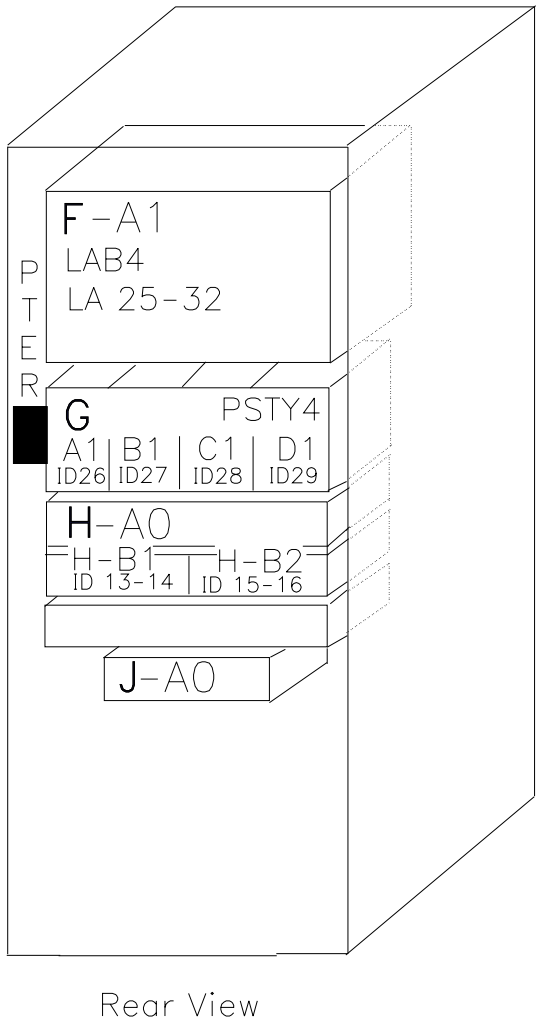


Figure 1-6. Adapter Frame, Frame 03 Component Locations

F Line adapter board (LA 25 to 32)
See Chapter 4, “Transmission Subsystem (TSS)” on page 4-1.

G PS type 4, up to four PS, one PS for two LAs
See “PS Type 4 Frame 03 Connection Layout” on page 10-22.

H AC and DC distribution
See page YZ513.

J Auxiliary power box
See “Auxiliary Power Box Frame 03 (03J-A0)” on page 10-8.

Line Frame, Frame 04 Component Locations

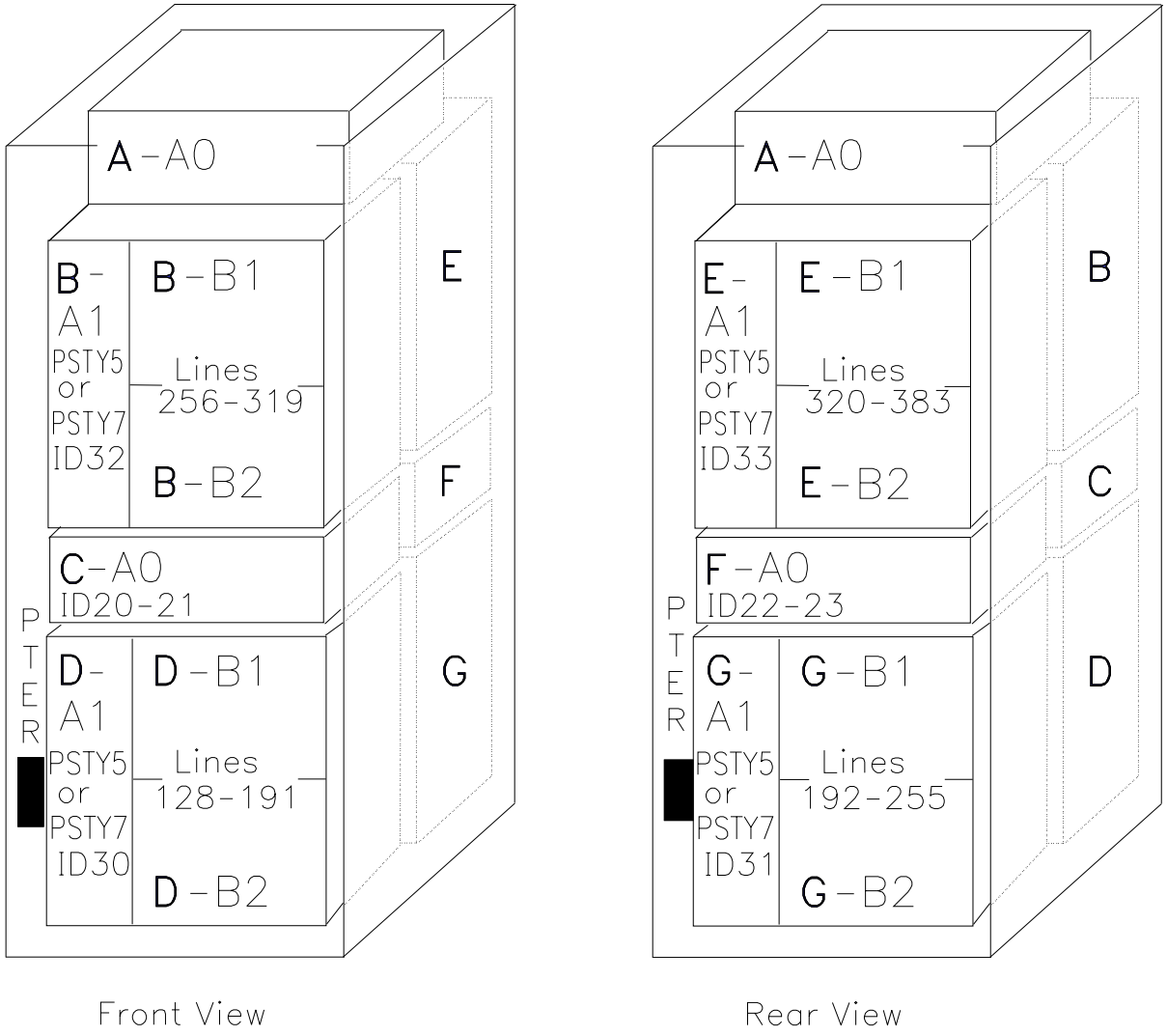


Figure 1-7. Line Frame, Frame 04 Component Locations

A AC distribution
See "AC-DC Distribution (04A-A0, 05A-A0, 06A-A0)" on page 10-9.

B LIC unit (from line 256 to line 319 for LICs 1-4, or line 256 to line 287 for LICs 5-6)
See Chapter 4, "Transmission Subsystem (TSS)" on page 4-1,
or "PS Type 5 Frame 04 Connection Layout" on page 10-26 for PS type 5 details,
or "PS Type 7 Frame 04 Connection Layout" on page 10-33 for PS type 7 details.

C Fan for LIC unit
See "PS Type 5 Frame 04 Connection Layout" on page 10-26, or "PS Type 7 Frame 04 Connection Layout" on page 10-33 for details.

D LIC unit (from line 128 to line 191 for LICs 1-4, or line 128 to line 159 for LICs 5-6)
See Chapter 4, "Transmission Subsystem (TSS)" on page 4-1,
or "PS Type 5 Frame 04 Connection Layout" on page 10-26 for PS type 5 details,
or "PS Type 7 Frame 04 Connection Layout" on page 10-33 for PS type 7 details.

E LIC unit (from line 320 to line 383 for LICs 1-4, or line 320 to line 351 for LICs 5-6)
See Chapter 4, "Transmission Subsystem (TSS)" on page 4-1.
or "PS Type 5 Frame 04 Connection Layout" on page 10-26 for PS type 5 details,
or "PS Type 7 Frame 04 Connection Layout" on page 10-33 for PS type 7 details.

F Fan for LIC unit
See “PS Type 5 Frame 04 Connection Layout” on page 10-26, or “PS Type 7 Frame 04 Connection Layout” on page 10-33 for details.

G LIC unit (from line 192 to line 255 for LICs 1-4, or line 192 to line 223 for LICs 5-6)
See Chapter 4, “Transmission Subsystem (TSS)” on page 4-1,
or “PS Type 5 Frame 04 Connection Layout” on page 10-26 for PS type 5 details,
or “PS Type 7 Frame 04 Connection Layout” on page 10-33 for PS type 7 details.

Line Frame, Frame 05 Component Locations

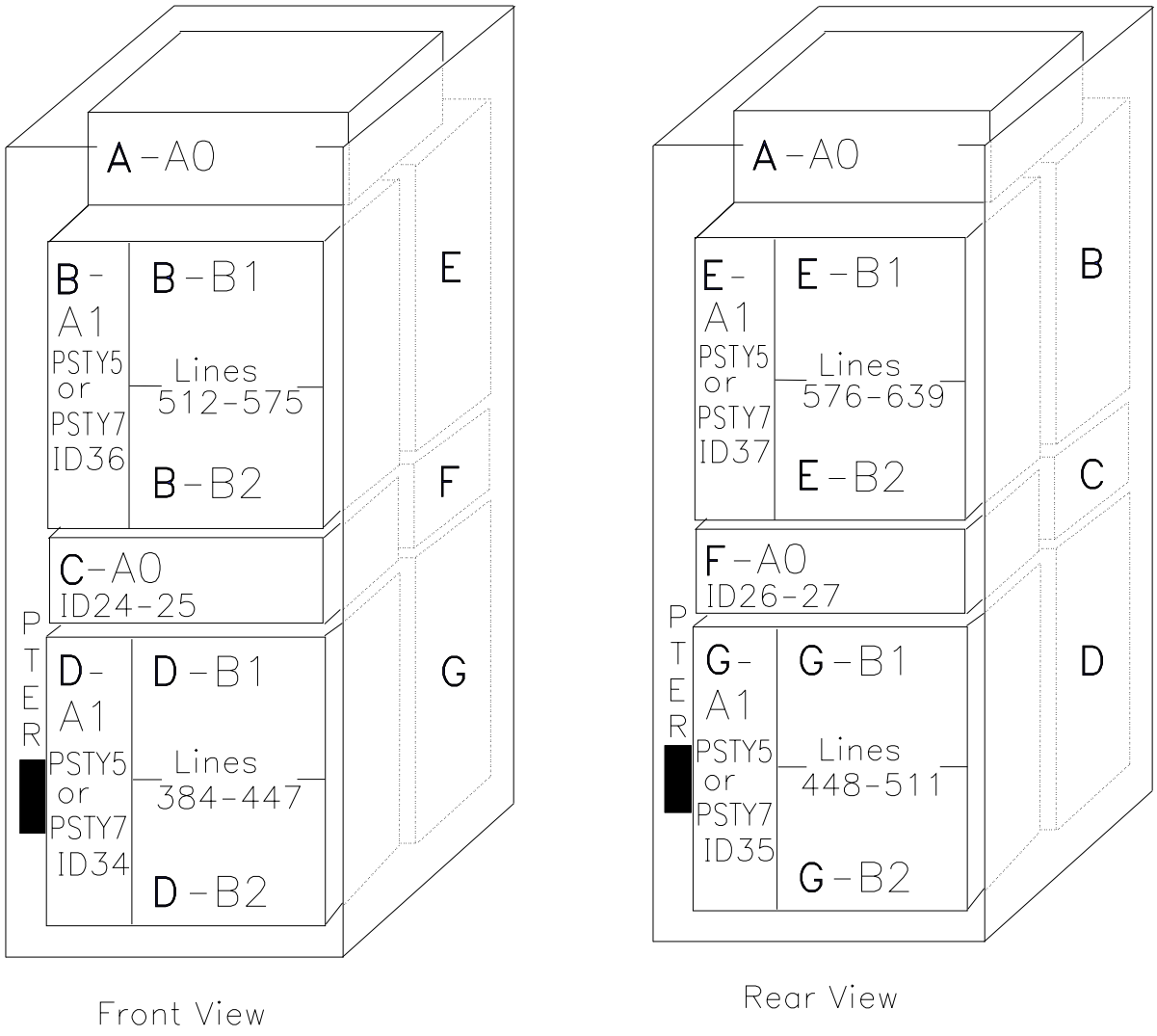


Figure 1-8. Line Frame, Frame 05 Component Locations

A AC distribution
See "AC-DC Distribution (04A-A0, 05A-A0, 06A-A0)" on page 10-9.

B LIC unit (from line 512 to line 575 for LICs 1-4, or line 512 to line 543 for LICs 5-6)
See Chapter 4, "Transmission Subsystem (TSS)" on page 4-1,
or "PS Type 5 Frame 05 Connection Layout" on page 10-27 for PS type 5 details,
or "PS Type 7 Frame 05 Connection Layout" on page 10-34 for PS type 7 details.

C Fan for LIC unit
See "PS Type 5 Frame 05 Connection Layout" on page 10-27, or "PS Type 7 Frame 05 Connection Layout" on page 10-34 for details.

D LIC unit (from line 384 to line 447 for LICs 1-4, or line 384 to line 415 for LICs 5-6)
See Chapter 4, "Transmission Subsystem (TSS)" on page 4-1,
or "PS Type 5 Frame 05 Connection Layout" on page 10-27 for PS type 5 details,
or "PS Type 7 Frame 05 Connection Layout" on page 10-34 for PS type 7 details.

E LIC unit (from line 576 to line 639 for LICs 1-4, or line 576 to line 607 for LICs 5-6)
See Chapter 4, "Transmission Subsystem (TSS)" on page 4-1.
or "PS Type 5 Frame 05 Connection Layout" on page 10-27 for PS type 5 details,
or "PS Type 7 Frame 05 Connection Layout" on page 10-34 for PS type 7 details.

F Fan for LIC unit
See “PS Type 5 Frame 05 Connection Layout” on page 10-27, or “PS Type 7 Frame 05 Connection Layout” on page 10-34 for details.

G LIC unit (from line 448 to line 511 for LICs 1-4, or line 448 to line 479 for LICs 5-6)
See Chapter 4, “Transmission Subsystem (TSS)” on page 4-1,
or “PS Type 5 Frame 05 Connection Layout” on page 10-27 for PS type 5 details,
or “PS Type 7 Frame 05 Connection Layout” on page 10-34 for PS type 7 details.

Line Frame, Frame 06 Component Locations

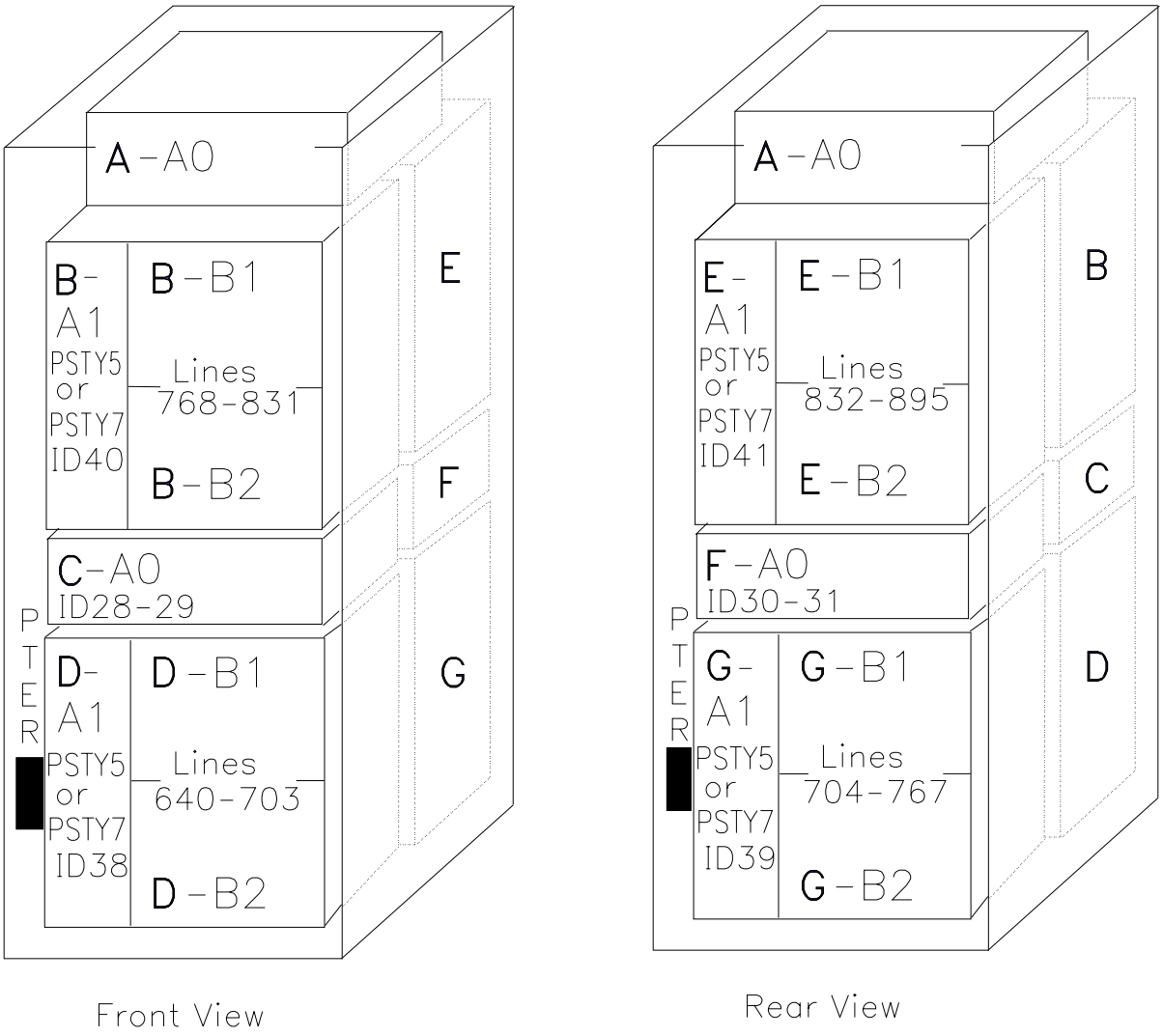


Figure 1-9. Line Frame, Frame 06 Component Locations

A AC distribution
See "AC-DC Distribution (04A-A0, 05A-A0, 06A-A0)" on page 10-9.

B LIC unit (from line 768 to line 831 for LICs 1-4, or line 768 to line 799 for LICs 5-6)
See Chapter 4, "Transmission Subsystem (TSS)" on page 4-1,
or "PS Type 5 Frame 06 Connection Layout" on page 10-27 for PS type 5 details,
or "PS Type 7 Frame 06 Connection Layout" on page 10-34 for PS type 7 details.

C Fan for LIC unit
See "PS Type 5 Frame 06 Connection Layout" on page 10-27, or "PS Type 7 Frame 06 Connection Layout" on page 10-34 for details.

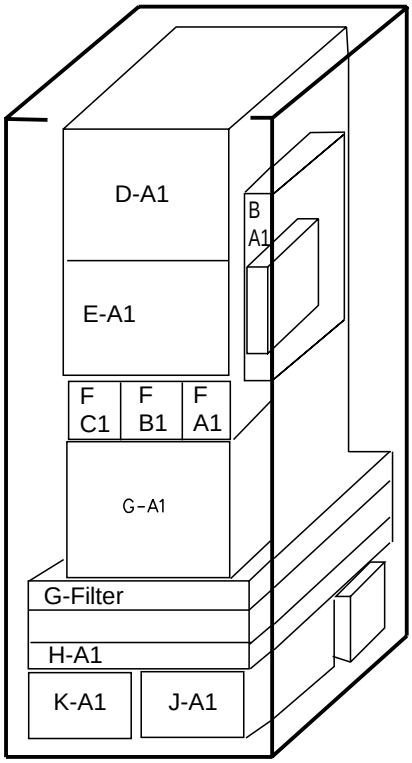
D LIC unit (from line 640 to line 703 for LICs 1-4, or line 640 to line 671 for LICs 5-6)
See Chapter 4, "Transmission Subsystem (TSS)" on page 4-1,
or "PS Type 5 Frame 06 Connection Layout" on page 10-27 for PS type 5 details,
or "PS Type 7 Frame 06 Connection Layout" on page 10-34 for PS type 7 details.

E LIC unit (from line 832 to line 895 for LICs 1-4, or line 832 to line 863 for LICs 5-6)
See Chapter 4, "Transmission Subsystem (TSS)" on page 4-1.
or "PS Type 5 Frame 06 Connection Layout" on page 10-27 for PS type 5 details,
or "PS Type 7 Frame 06 Connection Layout" on page 10-34 for PS type 7 details.

F Fan for LIC unit
See “PS Type 5 Frame 06 Connection Layout” on page 10-27, or “PS Type 7 Frame 06 Connection Layout” on page 10-34 for details.

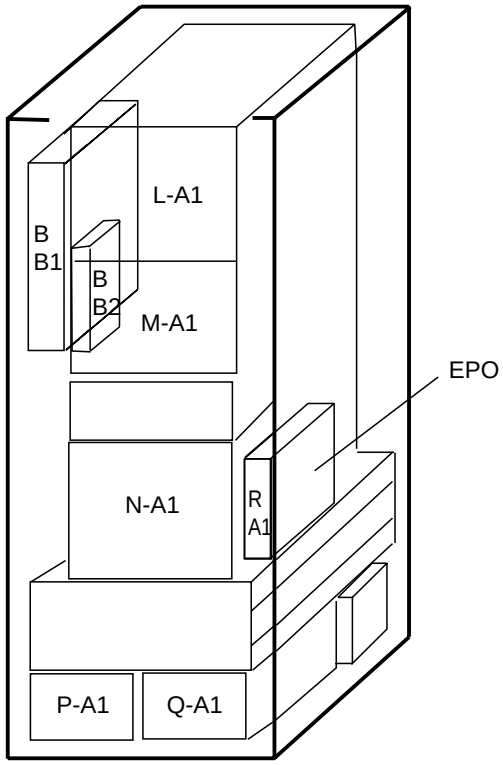
G LIC unit (from line 704 to line 767 for LICs 1-4, or line 704 to line 735 for LICs 5-6)
See Chapter 4, “Transmission Subsystem (TSS)” on page 4-1,
or “PS Type 5 Frame 06 Connection Layout” on page 10-27 for PS type 5 details,
or “PS Type 7 Frame 06 Connection Layout” on page 10-34 for PS type 7 details.

3746 Model 900, Frame 07 Component Locations



FRONT View

Figure 1-10. 3746 Model 900



REAR View

Figure 1-11. 3746 Model 900

B-A1/B1 Connectivity switch

E Expansion enclosure PRC

F Fans

G Basic enclosure PRC/SPS

J Backup ACPW or DCPW

K Basic ACPW

B-B2 Connectivity switch DC/DC

M Expans. enclos. CLP/SPD2

N Basic enclos. CLP/SPD1

P Transformer if backup ACPW installed

Q Transformer

R EPO

IBM 3745 Programming Support

The 3745 operates under the control of IBM licensed programs:

- Controller-resident programs, and
- Host-resident programs.

For details on these programs, refer to the publication mentioned in Appendix C of the *3745 Introduction*, GA33-0092.

Controller-Resident Programs

Network Control Program

The NCP provides major capabilities for SNA networks. However, existing start-stop and binary synchronous networks can be migrated to the 3745.

For start-stop protocols, the NCP supports a variety of transmission codes including ASCII, EBCDIC, EBCD, BCD, and correspondence code, for which it provides translation to and from EBCDIC. For the BSC protocol, support and translation are performed by the communication scanners.

ACF/NCP allows the controller to meet the demands of an ever-expanding network. It works with the host access method to control networks, from the simplest single-domain network with a single controller, to complex multiple-domain networks using advanced communications function networking, in accordance with the concepts of SNA.

NCP supports Internet Protocol (IP) using the ESS and also enveloped in SNA for transport over wide area networks.

Emulation Program

The 3745 runs under the control of the Emulation Program (EP) either standalone or in partitioned emulation programming (PEP) mode to support non-SNA devices.

Partitioned Emulation Program

PEP is a feature of the NCP. PEP lets the NCP operate certain lines in network control mode while operating others under EP control mode.

PEP can run only in a channel-attached controller. One subchannel address is required per line. Channel attachment must be byte-multiplex.

The partitioned emulation program emulates most of the functions of the IBM 2701 Data Adapter Unit, 2702 Transmission Control Unit or 2703 Transmission Control Unit and can communicate with various access methods running in the host. Most programs written for these machines can operate in the 3745 without modification. However, programs that involve timing or special hardware considerations may have to be changed.

Licensed Program

The following licensed programs can also reside in the 3745 together with the NCP:

- Network Terminal Option (NTO), which provides SNA protocol enveloping of the start-stop data stream for NCP-attached ASCII devices.
- X.25 NCP Packet Switching Interface (NPSI), for connections over X.25 NCP packet-switched networks.
- X.25 SNA Interconnection (XI) provides an X.25 DCE interface at the 3745 which is part of the SNA network. The SNA network can be used as a transport network for data exchange between two X.25-compatible DTEs attached to a 3745 node operating with XI.
- NCP coexists also with the following IBM licensed programs:
  - Network Routing Facility (NRF)
  - X.21 Short Hold Mode/Multiple Port Sharing (X.21 SH/MPS)
  - Non-SNA interconnection (NSI)

Host-Resident Programs

System Program Support

The host-resident programs that support the 3745 are:

- ACF/System Support Programs (ACF/SSP).

  The 3745 running under NCP/PEP is supported by ACF/SSP in a host. This program is used to generate control program load modules and load them in controller storage. It also allows dumping the controller storage, and transferring disk files to the hosts, including control program dump.

- Access methods located in one or more hosts:

  ACF/NCP communicates with one or several hosts through:

  - Virtual Telecommunications Access Method (VTAM*) or TPF

  PEP communicates with different access methods in the host processor:

  - Basic Telecommunication Access Method (BTAM),
  - BTAM Extended Support (BTAM-ES).

- Network Management Product (NetView).

NetView

NetView is an IBM licensed program used to monitor a network, manage it, and diagnose its problems.

NetView consists of the following components:

- Command facility: NCCF
- Session monitor: NLDM
- Hardware monitor: NPDA
- Status monitor: VCNA
- Help facility: NMPF
- Browse facility

As a cohesive set of SNA host network management services, NetView offers improvements:

- Consistency and usability in its support for network management,
- Easy installation procedure,
- Link between components and functions,
- Device support,
- Operator usability.

Network Performance Monitor

The network performance monitor aids network support personnel in managing controller networks. It collects data in the host and NCP to identify traffic conditions.

The 3745 also supports the Line Problem Determination Application (LPDA*).

Generating and Loading the Control Program

ACF/SSP is used in the host to generate the control program and load it into controller storage. The control program for the controller is generated from standard program modules of the NCP library using the SYSGEN procedure. The control program must reflect the required controller configuration. Several control programs can be generated to handle different subsets of lines attached to the same controller.

The twin CCU configuration implies generating and loading two distinct NCP twins in dual. For the twin in standby mode configuration, the switching capability transfers the control of the adapters of the failing CCU to the standby CCU.

When in twin backup configuration both NCPs must be able to control critical parts of the whole network.

At the initial loading of the control program, the NCP load module can be saved on the disk. This will allow initialization of the CCU from the controller disk. The host operator can also define the stand-alone IPL at any IPL operation.

VTAM and MOSS have been modified to allow new keywords. These new keywords inform MOSS to perform specific actions:

- Save load module to disk.
- Load NCP from disk after an NCP abend or power On.
- Dump NCP to disk after an abend.

VTAM also has a 'MOSS Assist Command'. VTAM can tell MOSS to load from disk.

The dump capability of MOSS allows dump transfer to the host.

Migration/Coexistence

The 3745 running under ACF/NCP can coexist with other IBM communication controllers.

The NCP with the PEP feature permits migration from the 2701, 2702, 2703, and 3704/3705/3720/3725/EP controllers.

The 3745 offers a path for conversion from existing systems and for continuing growth. A system designed with a 3725 may be transferred to the 3745 after modification and regeneration of the control program. The control program generation deck that was used in the 3725 program generation can be used with some modifi-

cations to the definition statements (assuming that the controller has the same line configuration).

Preventive Maintenance

Air filters and the battery are replaced by maintenance personnel.

An alert notifies the customer for air filters and battery replacement, and provides the CE with a reference code.
The *Maintenance Information Procedures*, Chapter 5 "IBM 3745 FRU Exchange" guides the maintenance personnel for replacement procedures.

Maintenance Philosophy

See *Maintenance Information Procedures*, Chapter 1 "Introducing the IBM 3745 Communication Controller".

Maintenance Aids

Tools and Test Equipment

See *Maintenance Information Procedures*, Chapter 1 "Introducing the IBM 3745 Communication Controller".

Chapter 2. Central Control Unit (CCU)

The CCU in 3745 Data Flow

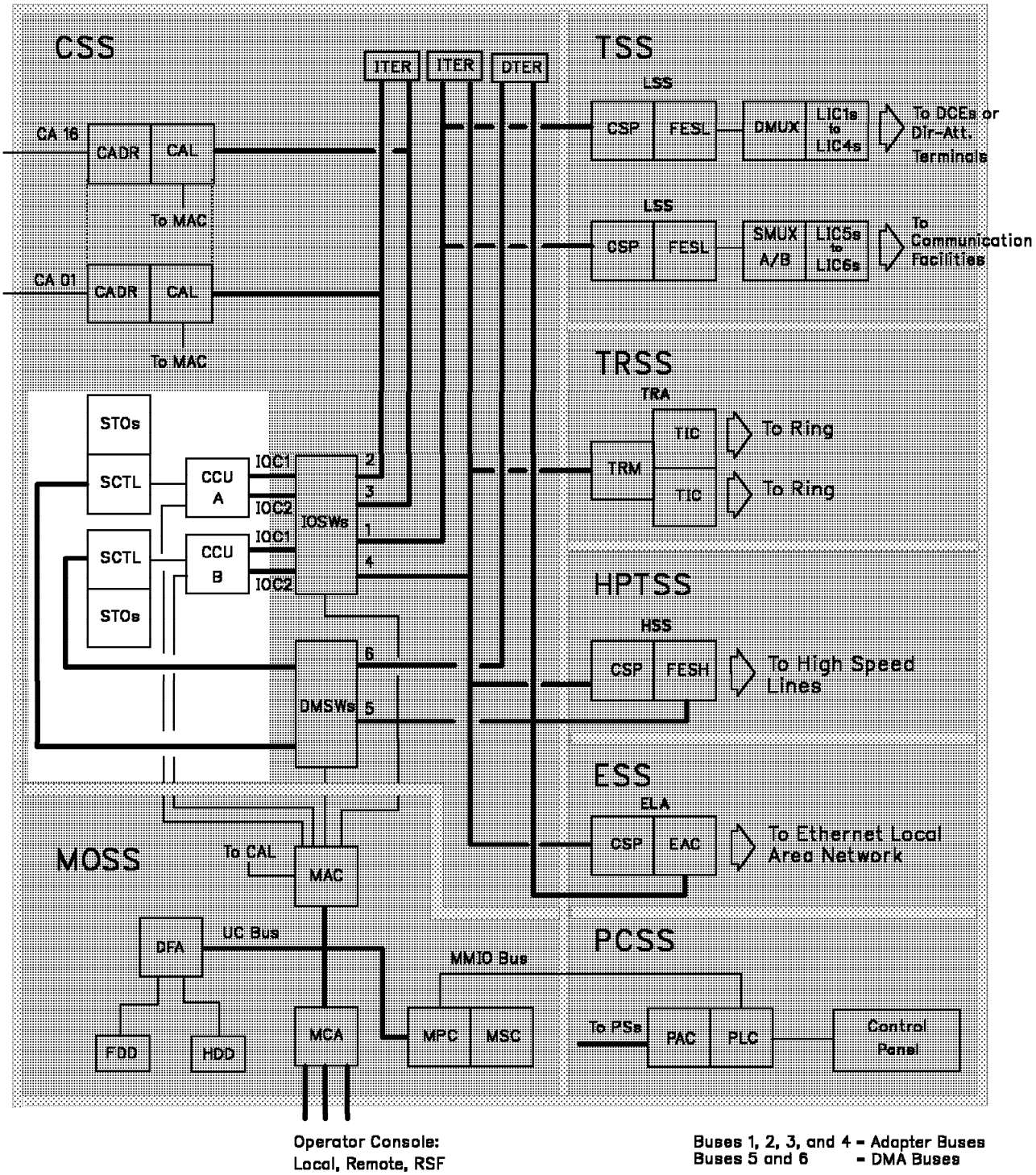


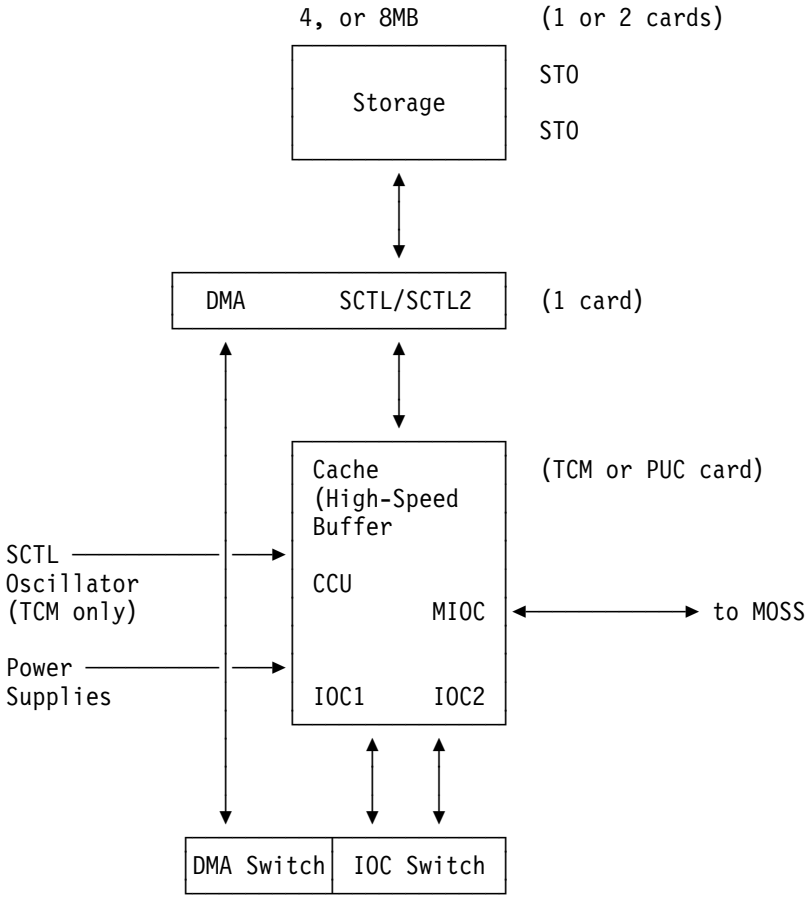
Figure 2-1. The CCU in 3745 Data Flow. For models 21A-61A, DMA and IOC buses are connected to the CBC in the 3746-900. The MCA card is replaced by the MLA card which interfaces to the MPC card through the MMIO bus. This MLA card links the MOSS to the Service Processor through a LAN.

General Description

One or two CCUs can be present on the 3745:

- The 3745 Model 210/21A or 310/31A is equipped with one CCU.
- The 3745 Model 410/41A or 610/61A is equipped with two CCUs.

Data Flow Without a 16 MB Feature



Packaging

See pages YZ032 for TCM and YZ022 for PUC for locations.

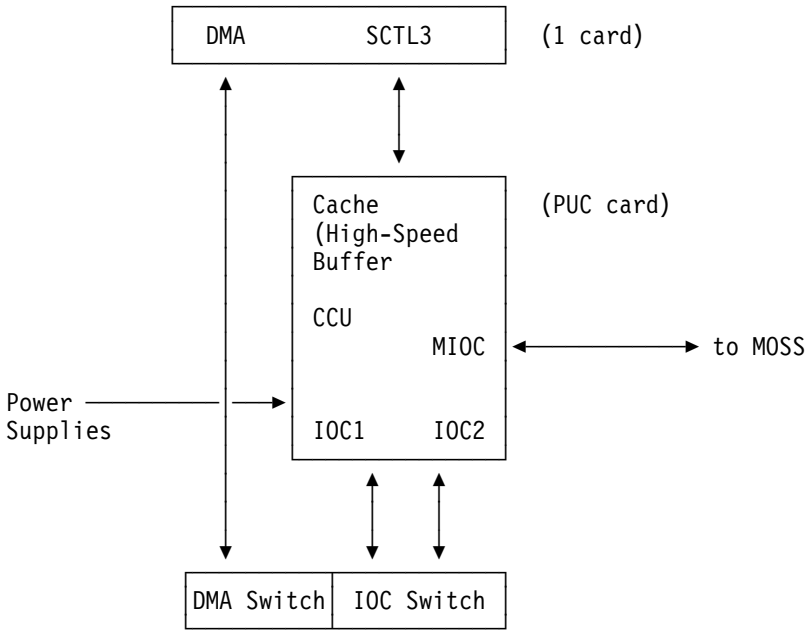
The CSS includes the following components:

- Processor Unit (TCM or PUC card)
- Storage Basic Card (STO)
- Storage Expansion Card (STO)
- Storage Control Card (SCTL/SCTL2/DMA).

Data Flow With a 16 MB Feature

On 3745 Models 31A and 61A a 16 MB storage feature is available. This 16 MB storage is part of the SCTL3 card. No STO card is installed

On 3745 Model 61A if the 16 MB feature is installed, it must be installed on both sides.



Functional Description

The central control unit (CCU) is an interrupt-driven processor with a stored program (called the 'control program' in this manual) that controls the data transfers on the channel and transmission interfaces.

The CCU:

- Executes the machine instruction set (CCU cycle=75 ns for TCM or 56 ns for PUC). to perform arithmetic or logical operations, exchange data between main storage and the working registers, and also between the local store and the work registers.

  Data transit between the CCU and main storage is achieved via a high-speed buffer (cache) under the control of the SCTL logic.

  Data can also transit directly between main storage and high-speed adapters via the 'Direct Memory Access' (DMA) logic.

- Communicates with adapters through the IOC logic in PIO or AIO mode:

  PIO mode: The exchange operation is initiated by IOH/IOHI instructions in the CCU.

  AIO mode: The operation uses cycle steals for data exchange between adapters and main storage without control program intervention.

  Two buses: IOC1 and IOC2 give access to the adapters' environment through the IOC switch.

- Communicates with the MOSS through the MOSS IOC. The operations performed can be direct or indirect (MIOH/MIOHI). MOSS uses the CCU level scan sensitive design (LSSD) to read or write any CCU discrete latch.

Program Levels

The controller hardware has five operational program levels:

- **Program level 1**

  This is the highest priority program level. Interrupt requests assigned to level 1 include all critical check conditions such as CCU checks, program checks, addressing exceptions, and adapter checks. Initial Program Load (IPL) and address compare interrupts are also handled at this level.

- **Program level 2**

  Normal operational interrupt requests from the communication adapters are assigned to this program level and certain program controlled interrupts (PCIs) are also assigned to this level.

- **Program level 3**

  Normal operational interrupt requests from the channel adapters, interval timers and program-controlled interrupt 3 (PCI) requests and panel interrupts are assigned to this level.

- **Program level 4**

  Certain program-controlled interrupt (PCI) requests and the supervisor call request (generated when the exit instruction is executed at program level 5), and MOSS request service and request response are assigned to this interrupt program level. This level is the lowest priority interrupt level.

- **Program level 5**

  This level is the lowest priority level and is normally active when none of the other four levels requires program cycles.

Masking Program Level Priorities

Programs at levels 1, 2, 3, or 4 can mask all interrupt requests for program levels 2, 3, or 4 and can mask adapter interrupt requests for level 1. Moreover program execution in level 5 can be masked.

The normal operational priority structure can be changed by output instructions X'7E' and X'7F' (set/reset mask register).

When the mask is set for one or more of program levels 2, 3, or 4, interrupt requests for those levels will not cause an interrupt. When the mask is set for program level 1, requests by adapters for level 1 will not cause an interrupt though any other request will be honored.

When the mask for level 5 is set, the use of machine cycles for program execution in level 5 is prevented. Thus, level 5 program execution is masked. In this case, when no program is executing in levels 1, 2, 3, or 4, the CCU enters the WAIT state and no program executes.

To selectively mask one or more program levels, one of the active general registers is loaded with the bits corresponding to those program levels to be masked. Output instruction X'7E' (set mask register) is then executed using the general register as input to the mask register. To selectively unmask one or more program levels, the same procedure is followed except that the output X'7F' (reset mask register) instruction is executed.

Interrupts

The communication controller operates in response to requests from either the control program or the hardware. Since these requests may have varying degrees of urgency, a priority system is used. Each program, CCU and adapter request, is assigned a particular priority level. A request for use of the controller by the control program or hardware functions is called an interrupt request.

Interrupt Mechanism

The interrupt mechanism determines when an interrupt can be handled. If the interrupt request is to be allowed, the change from the active program level to the interrupting program level takes place immediately after completion of the current instruction. If several interrupt requests having different priorities are present at the same time, the one with the highest priority obtains use of the controller. When an interrupt request is granted use of the controller, it can be interrupted in that use by another request having a higher priority.

When an interrupt occurs, instruction execution at the lower priority program level is suspended until instruction execution is completed at the higher priority level. An

interrupt to a specific program level prevents future interrupt requests assigned to either that level or to a lower priority program level from causing another interrupt until the servicing of the first interrupt is complete.

Interrupt Request Determination

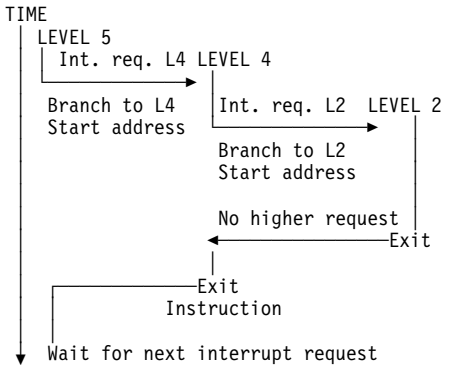
The priority of simultaneous interrupt requests assigned to the same interrupt program level is resolved by the order in which the program tests the set/reset condition of the CCU and adapter interrupt request latches.

Interrupt requests from the CCU and the adapters are grouped together according to their source for ease of identification. The set/reset condition of a specific interrupt request latch can be determined by checking the interrupt request group to which it is assigned. Input X'77' indicates the non-level 1 interrupt requests that are set by the adapters. Input X'7F' indicates the non-level 1 interrupt requests that are set by CCU or program. Input X'7E' indicates all level 1 requests. These inputs load the contents of the appropriate interrupt request group into an active general register. The program may then test the general register to identify the request.

Setting/Resetting Interrupt Requests

A particular interrupt request latch can be set as a result of a hardware-detected condition or, in some cases, by the program through the execution of an output instruction. The latch can be reset by one of several output instructions, depending upon the specific interrupt request. The procedures for setting and resetting individual adapter interrupt requests are described in the adapter sections.

For special service requests, program levels 1, 2, 3, and 4 may issue a program-controlled interrupt (PCI) request to program levels 2, 3, and 4. Output instructions X'7B' (set PCI L2), X'7C' (set PCI level 3), and X'7D' (set PCI level 4) set the PCI interrupt requests. Certain bits in output X'77' (miscellaneous control) reset the PCI requests and other CCU interrupt requests such as the interval timer level 3 request and the SVC level 4 request. If any bits are ON in registers 77, 7E, 7F, a request for a particular program level is active and must be reset or masked before the program can execute in a lower level. The following example illustrates the interrupt mechanism.



Interrupt Request Sources

Interrupt L1

Adapter L1 Request (Error)
Address Compare L1
Address Exception L1
L5 I/O Check L1
Protect Check L1
Invalid Op Check L1
IPL Request L1
MOSS Inoperative L1
Hard Error L1 (Hard errors stop the CCU unless it is in bypass mode.)
I/O Parity Error
I/O Time out Error

Interrupt L2

Adapter L2 Request (LA)
Program-Controlled Interrupt L2
MOSS Diag L2

Interrupt L3

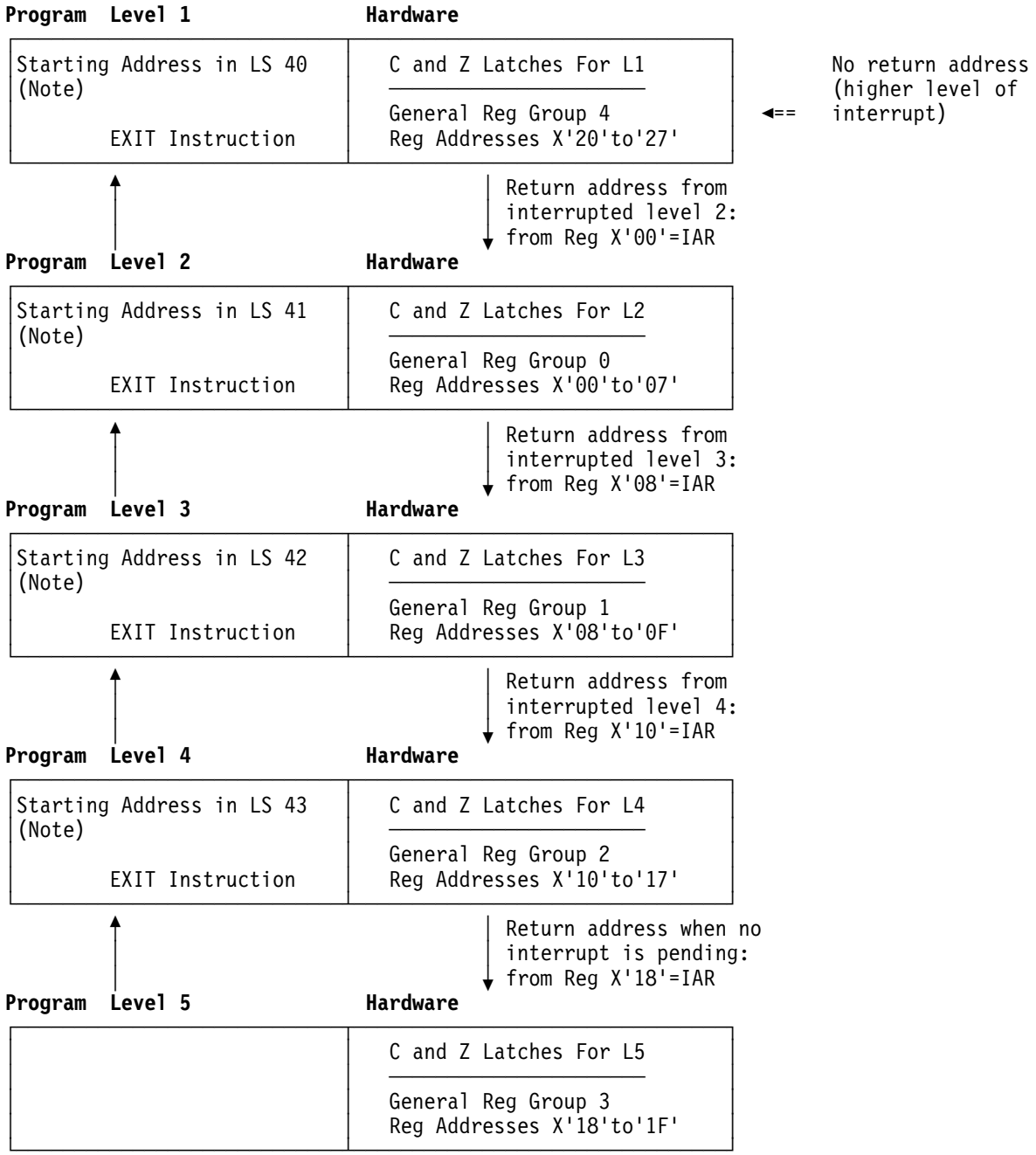
Adapter L3 Request (CA)
MOSS Diag L3
Interval Timer L3
Program-Controlled Interrupt L3
Panel Interrupt Request L3

Interrupt L4

Adapter L4 Request (Not Used)
Program-Controlled Interrupt L4
MOSS Req SVC L4
MOSS Req Response L4
SVC L4 (Call from Level 5)

Level 5 No interrupt (first entry)

The following figure shows the various links between the different priority levels.



Note: The interrupt levels 1, 2, 3, and 4 starting addresses are set during IPL via output instructions X'40' through X'43'.

Instruction Set

The 3745 contains 53 executable instructions.

Any attempt at program levels 2, 3, 4, or 5 to execute an operation code other than one of the 53 specified operations results in a level 1 interrupt with the 'invalid op' check bit set ON in the CCU interrupt request group 1 register 7E.

An attempt to execute an invalid op code in program level 1 sets the 'hard error' bit in the CCU check register along with an invalid Op check bit. In all cases, execution is suppressed.

For details on instruction operation, refer to *3745 Principles of Operation*, SA33-0102. However, hereafter is the list of instructions with their different formats for quick reference only.

Instruction		Format															See Note(s)
		CZ	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
B	Branch		1	0	1	0	1	Displacement										+	9
BCL	Branch On C Latch		1	0	0	1	1											−	9
BZL	Branch On Z Latch		1	0	0	0	1												9
BCT	Branch On Count		1	0	1	1	1				1	Displacement						+	1, 2, 9
BB	Branch On Bit		1	1	M	M	1				M							−	1, 2, 9, 10
LRI	Load Reg. Imm.	*	1	0	0	0	0												1, 2
ARI	ADD Reg. Imm.	*	1	0	0	1	0												1, 2
SRI	Subtract Reg. Imm.	*	1	0	1	0	0		R	N	Immediate Data								1, 2
CRI	Compare Reg. Imm.	*	1	0	1	1	0												1, 2
XRI	Exclu. or Reg. Imm.	*	1	1	0	0	0												1, 2
ORI	Or Reg. Imm.	*	1	1	0	1	0												1, 2
NRI	And Reg. Imm.	*	1	1	1	0	0												1, 2
																			1, 2
TRM	Test Reg.Under Mask	*	1	1	1	1	0				Mask Bits								1, 2
LCR	Load Charac. Reg.	*	0				0				0	0	0	0	1	0	0	0	4, 5
ACR	Add Charac. Reg.	*	0				0				0	0	0	1	1	0	0	0	4, 5
SCR	Subt. Charac. Reg.	*	0				0				0	0	1	0	1	0	0	0	4, 5
CCR	Comp. Charac. Reg.	*	0	R2		N2	0	R1		N1	0	0	1	1	1	0	0	0	4, 5
XCR	Exclu. Or Char. Reg	*	0				0				0	1	0	0	1	0	0	0	4, 5
OCR	Or Char. Reg.	*	0				0				0	1	0	1	1	0	0	0	4, 5
NCR	Add Char. Reg.	*	0				0				0	1	1	0	1	0	0	0	4, 5
LCOR	Ld Ch. W/Offset Reg	*	0				0				0	1	1	1	1	0	0	0	4, 5

Instruction		Format																See Note(s)
		CZ	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
ICT	Ins. Char. & Count		0				0				0	0	0	1	0	0	0	0	1, 2, 8
STCT	St. Char. & Count		0				0				0	0	1	1	0	0	0	0	1, 2, 8
IC	Insert Char.	*	0				1	R		N	0	Displacement							1, 2, 7
STC	Store Char.		0				1				1								1, 2, 7
LH	Load Halfword	*	0		B		0				0							1	6, 7
STH	Store Halfword		0				0	R			1							1	6, 7
L	Load	*	0				0				0						1	0	6, 7
ST	Store		0				0				1						1	0	6, 7
LHR	Load Half. Reg.	*	0				0				1	0	0	0	0	0	0	0	3
AHR	Add Half. Reg.	*	0		R2		0	R1			1	0	0	1	0	0	0	0	3
SHR	Sub. Half. Reg.	*	0				0				1	0	1	0	0	0	0	0	3
CHR	Comp. Half. Reg.	*	0				0				1	0	1	1	0	0	0	0	3
XHR	Exc. Or Half. Reg.	*	0				0				1	1	0	0	0	0	0	0	3
OHR	Or Half. Reg.	*	0		R2		0	R1			1	1	0	1	0	0	0	0	3
NHR	And Half. Reg.	*	0				0				1	1	1	0	0	0	0	0	3
LHOR	Ld.Hw W/Offset Reg	*	0				0				1	1	1	1	0	0	0	0	3
LR	Load Register	*	0				0				1	0	0	0	1	0	0	0	3
AR	Add Register	*	0				0				1	0	0	1	1	0	0	0	3
SR	Subtract Register	*	0				0				1	0	1	0	1	0	0	0	3
CR	Compare Register	*	0				0				1	0	1	1	1	0	0	0	3
XR	Exclu. Or Reg.	*	0				0				1	1	0	0	1	0	0	0	3
OR	Or Register	*	0				0				1	1	0	1	1	0	0	0	3
NR	And Register	*	0				0				1	1	1	0	1	0	0	0	3
LOR	Load With Of. Reg.	*	0				0				1	1	1	1	1	0	0	0	3
BALR	Branch & Link Reg.		0		R2		0	R1			0	1	0	0	0	0	0	0	3
IOH	Adapter In/Out	*	0				0				0	1	0	1	0	0	0	0	3, 12, 14
IOHI	Adapter IO immed.	*	0		000		0	R			0	1	1	1	0	0	0	0	16/31 3, 12, 15
IN	CCU Register In		0				0								1	1	0	0	6, 12, 13
OUT	CCU Register Out		0		E		0	R			E				0	1	0	0	6, 12, 13
BAL	Branch and Link		1	0	1	1	1				0	1	A (**)						16/32 6, 11
LA	Load Address		1	0	1	1	1				0	0	A (**)						6, 11
EXIT	Exit		0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	

* = Indicates that the C and Z registers are changed by the execution of the instruction.

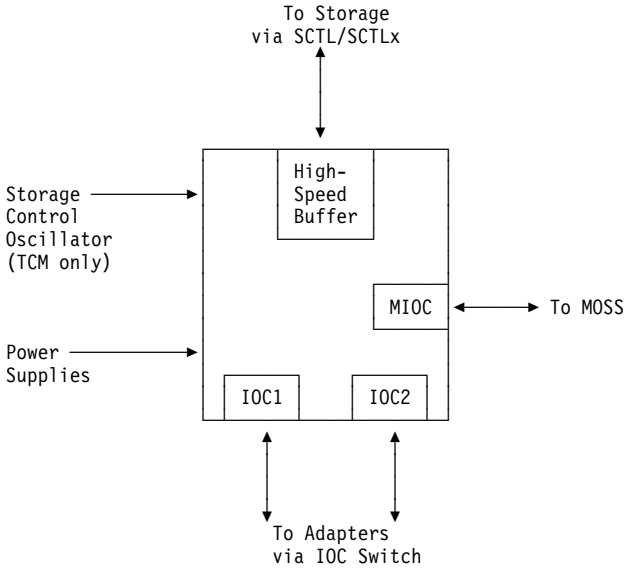
** = The A field contains 22 bits, therefore the branch address is always below four megabytes.

Notes:

1. The R field addresses the general registers. As the R field is only 2 bits long, these bits form the 2 high-order bits of the register address. The low-order bit of the address is created by hardware, and is always 1. This means that only odd-numbered general registers (1, 3, 5, 7) can be addressed.
2. The bit marked N is used to select one (or sometimes both) of the bytes of the general register selected by the associated R field.
3. The R1 and R2 fields address the general registers. As the R1 and R2 fields are 3 bits long, these bits can take any value from 0 to 7, and all 3 bytes of the register are used in the operation.
4. The R1 and R2 fields address the general registers. As the R1 and R2 fields are only 2 bits long, these bits form the 2 high-order bits of the register address. The low-order bit of the address is created by hardware, and is always 1. This means that only odd numbered general registers (1, 3, 5, 7) can be addressed.
5. The bit marked N is used to select one (or sometimes both) of the bytes of the general register selected by the associated R1/R2 field.
6. The R field addresses the general registers. As the R field is 3 bits long, these bits can take any value from 0 to 7, and all 3 bytes of the register are used in the operation.
7. The effective storage address is formed by adding the displacement to the contents of the base register selected by bits 1-3.
8. The contents of the base register specified are incremented by 1 after storage access.
9. The displacement field is added to the address of the next sequential instruction (contained in general register 0) to form the branch address.
10. The 3 bits of the mask (M) field specify the bit to be tested.
11. The 22 bits contained in the extension byte and in bytes 0 and 1 form an address. In the case of the branch and link instruction, these 22 bits form the branch address. In the case of the load address instruction, the 22 bits are treated as immediate data and loaded into the register specified by R.
12. The Input X'n' and Output X'n' instructions can address only the **CCU** external registers. The IOH and IOHI instructions can address only the **adapter** external registers. See below for lists of these registers.
13. The E field consists of 7 bits and addresses one of the 128 external CCU registers.
14. The contents of R2 includes the address of the adapter external register.
15. The second half-word contains the address of the adapter external register.

CCU Environment

The figure below shows all interconnections to the CCU.



- **Storage Control Interconnection (SCTL/SCTLx)**

  Writing data to main storage is performed through the write storage data register (this register is 27 bits wide; 24 data bits + 3 parity bits). Data read from storage is written directly into one or more CCU registers and/or in local storage. Main storage is read and written across the storage data bus (bidirectional, 36 bits wide) which is the only port to/from main storage for the whole machine.

- **MIOC Interconnection**

  Through the MIOC interface, the MOSS will be able to obtain/alter the state of 3745.

- **IO Buses**

  These are multipurpose compatible buses that are used as the base attachment interface for all channel adapters, IO Switch, and LAs to the CCU.

- **CCU Main Oscillator**

  For models 21x and 41x, the oscillator is packaged in the SCTL card. The SCTL 53.1914 MHz quartz oscillator signals are used by the TCM to generate its timings.

  For models 31x and 61x, the oscillator is packaged in the PUC card. The PUC 80.9824 MHz quartz oscillator signals are used by the PUC and SCTL2/3 to generate their timings.

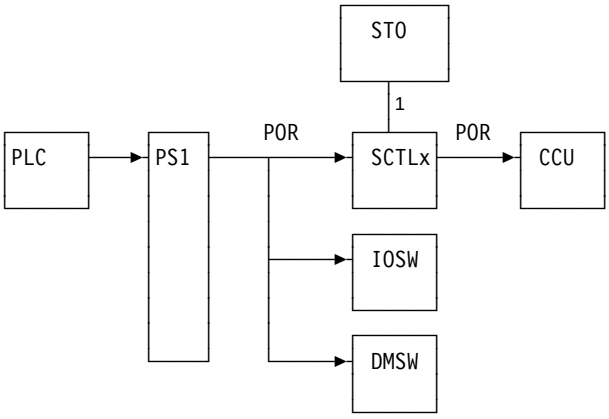
- **Power Interface**

  The power interface provides the CCU with all necessary power voltage requirements needed to operate all 3745 functions.

CCU Subsystem POR

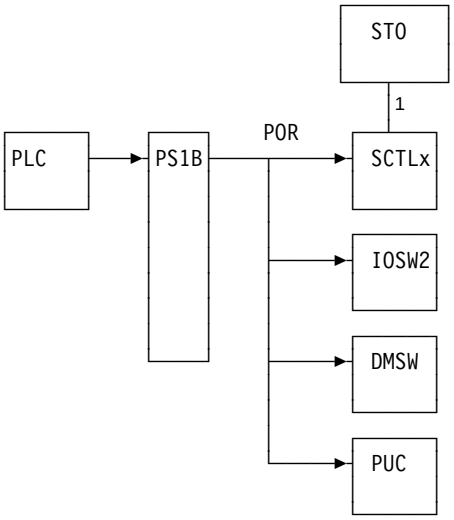
POR is activated at the machine power ON, or at machine reset.
The MOSS code can ask the PLC to activate the POR line.

Models 21x and 41x



1: STO is zeroed.

Models 31x and 61x



1: STO is zeroed.

Storage control

At the end of the POR signal, the following sequence of 'warm up' storage is started.

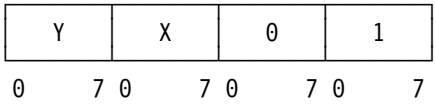
1. Clear all latches and counters.
2. Then, perform 128 cycles to initialize storage.
3. Perform one cycle to configure storage type and size.
4. Then, blank storage with proper ECC.

During all that time, incoming requests are inhibited.

Main Storage

The main storage contains the control program. It is packaged on one or two cards of 4MB each, allowing configurations of 4, or 8MB.

The storage word consists of 4 bytes, referenced as follows:

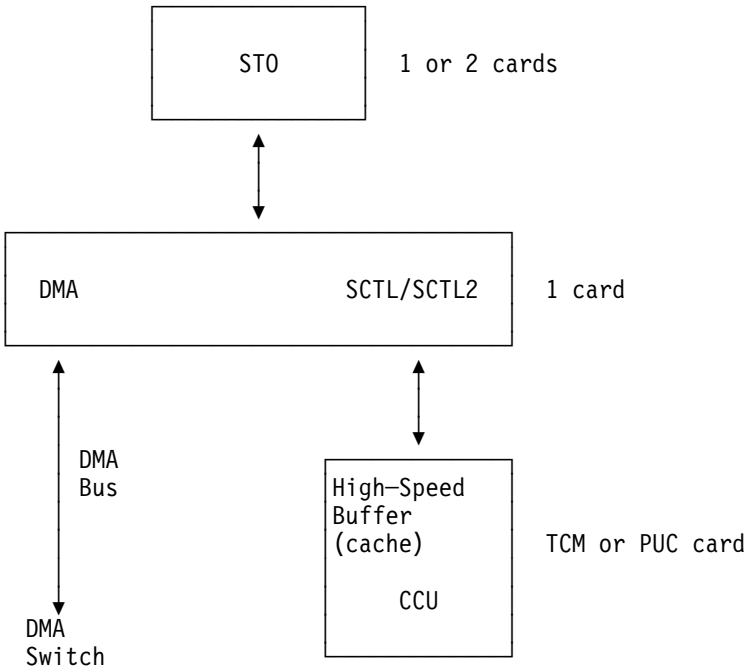


The bytes are addressed from the storage address register, which is 27 bits wide.

Storage Environment

The main storage communicates with:

1. The CCU via the storage control
2. The high-speed adapters via the 'Direct Memory Access' (DMA).



The SCTL and DMA are packaged on the same card.

On 3745 models 31A and 61A if the 16 MB feature is installed, the SCTL3 replaces the SCTL/SCTL2 card and no STO card is needed.

Storage Control/Direct Memory Access (SCTL/DMA)

The SCTL/DMA main functions are:

1. Allocate main storage access to the different users (CCU/HSB and DMA).
2. Control the different storage operations and ensure data transfer integrity:
   - CCU Read/Write

Write requests are buffered in SCTL/DMA so that CCU and storage operations can overlap.

- HSB line loading
- DMA burst transfers

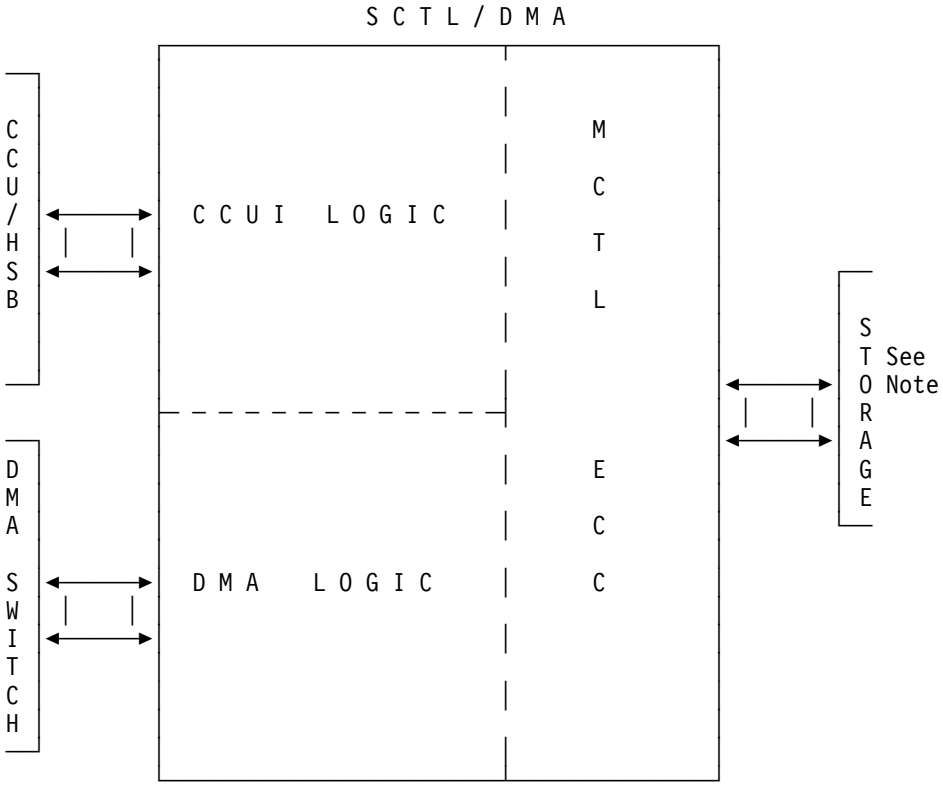
  Data is aligned and temporarily stored in a buffer so as to optimize the use of memory bandwidth.

3. Control the HSB operations (line loading). Maintain HSB consistency with storage during DMA write operations, by means of an HSB line invalidation mechanism.
4. Check for unauthorized DMA write operations with a DMA storage protect mechanism.
5. Provide phase signals from a four-phase oscillator to allow CCU/HSB to generate CCU and SCTL clocks (TCM only).

Function Partitioning

The SCTL/DMA card can be partitioned into three distinct functional parts:

- CCUI LOGIC
- DMA LOGIC
- MCTL/ECC.



Note: Storage is part of the SCTL3 when 16 MB feature is installed on 3745 Models 31A and 61A.

1. CCUI LOGIC

   The CCUI (CCU Interconnection) logic interconnects the CCU/HSB. It receives and buffers requests from CCU/HSB and controls HSB line loading. It controls HSB line invalidation and accesses the DMA storage protect RAM (during DMA write operations) on behalf of the DMA logic. The CCUI logic makes storage requests to the MCTL/ECC.

2. DMA LOGIC

   The DMA logic interconnects the DMA bus on which the FESH adapters are hooked. It receives requests from DMA adapters. It performs data alignment, reads or writes its DMA buffer and makes storage requests to the MCTL/ECC. During a DMA write storage transfer, it makes requests to the CCUI logic for HSB line invalidations and for access to the DMA storage protect RAM.

3. MCTL/ECC

   The MCTL/ECC (Storage Control/Error Checking and Correction) interconnects the storage. It receives storage requests from the CCUI logic and the DMA logic. It performs arbitration between these two users, accesses storage and controls the ECC mechanism.

The storage control contains an error correction code which permanently stores a word, either with its original parity or inverted, thus allowing to mask at least one error on top of the one-bit correction.

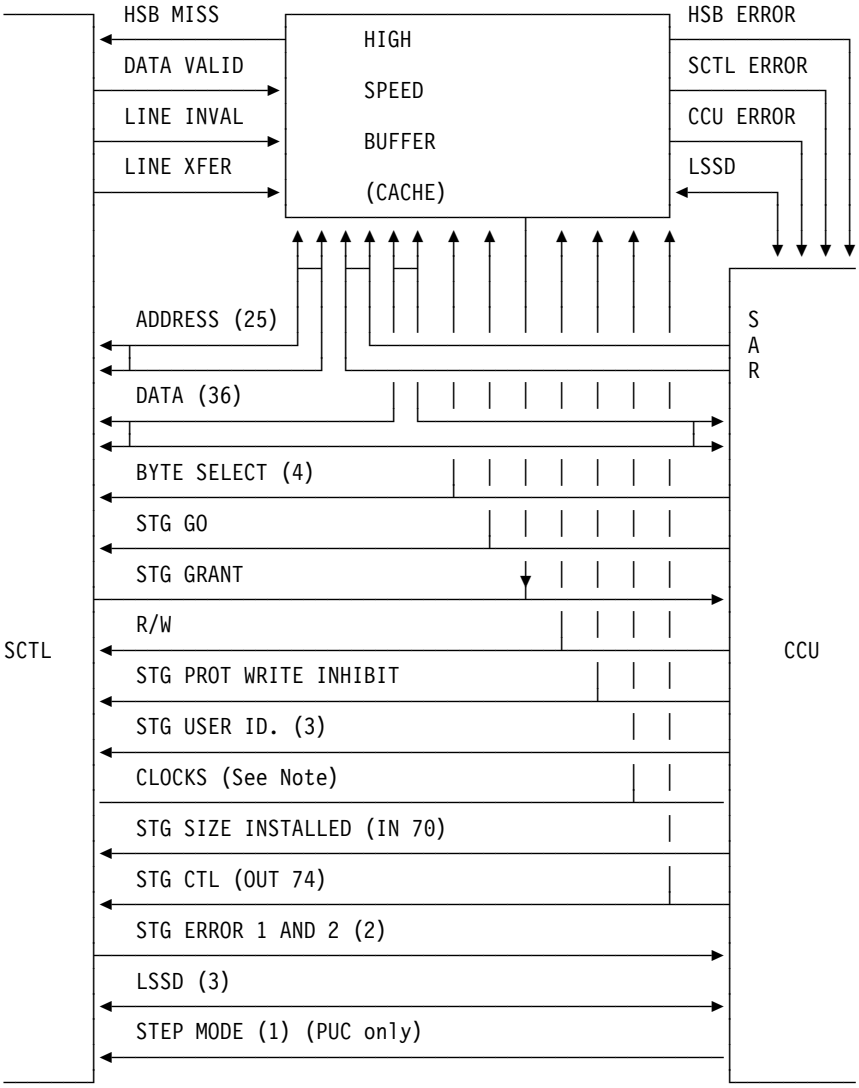
The correcting capability of the ECC depends on the type of bit error, whether it is a hard error (storage position stuck to 0 or 1), or a soft (transient) error.

The correction coverage is the following:

Type of fault	Coverage	Notes
One hard	100%	As in 3725
One soft	100%	As in 3725
One hard and one soft	100%	As in 3725
Two hard	100%	New capability
Two hard and one soft	50%	New capability
Two soft	0%	Not possible

SCTL/CCU-HSB Interconnection

For locations see the pages YZ032 for TCM and YZ022 for PUC.



Note: 7 wires from SCTL to TCM
9 wires from PUC to SCTLx

Storage Control Mode

See the output X'74' instruction page 2-29.

DMA/DMA-Switch Interconnection

See “DMA Buses” on page 3-37.

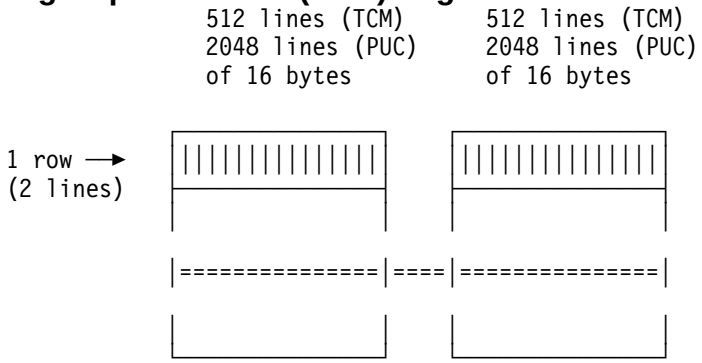
CCU to/from Storage

High-Speed Buffer (HSB or CACHE)

The HSB, packaged on the TCM or the PUC card together with the CCU, provides the CCU with instructions and data at cycle rate.

If the instruction or data is not in the HSB when it is fetched, the 16 contiguous bytes are automatically transferred into the HSB. The probability is high that the next instruction(s) or data will be in these 16 bytes, then, as long as instructions and data are found in the HSB, the CCU is not slowed down by main storage and can run at full speed.

High-Speed Buffer (HSB) Organization



On CCU request, the HSB can either write one byte, one halfword, or one fullword. However, the HSB is always loaded from storage with 16 contiguous bytes forming a line.
For the TCM the 16KB HSB is made of 1024 x 16-byte lines and its directory is two-set associative. The HSB organization is thus: 512 rows x 2 sets x 16 bytes.
For the PUC the 64KB HSB is made of 4096 x 16-byte lines and its directory is two-set associative. The HSB organization is thus: 2048 rows x 2 sets x 16 bytes.

The HSB is controlled by means of an X'74' out instruction. The following table summarizes the various HSB data path functions:

REQUEST	STORAGE USER	HSB FUNCTION	MANAGEMENT
READ	I– fetch Prog. READ	HIT: HSB read MISS: line loaded from storage + HSB read	LRU update LRU update
	other than I–fetch and Prog. Read	HIT: HSB read MISS: storage read	LRU update ———
WRITE	Any user	HIT: HSB write + storage write MISS: storage write	LRU update ———
LINE INVALIDATE	DMA	INVALIDATE a line in the HSB	LRU update

Write Policy

Write requests are always presented both to the HSB and main storage (store-through policy). The WRITE request is sent to storage but as soon as it is accepted by the SCTL, the CCU proceeds to the next instruction without waiting for storage update completion. This policy ensures that HSB and storage are always consistent with each other and minimizes housekeeping when an HSB line must be replaced.

Since on a write request, main storage is always updated (regardless of HSB hit or miss), and since the CCU does not wait for write completion, there would be no gain in loading a line in the HSB in case of an HSB miss. This new line would most probably replace a more useful line in the HSB. Therefore, the HSB is not loaded with a new line on a WRITE miss.

Read Policy

A CCU read request can come from different sources: The source (called the storage user) can be the MOSS, the branch trace, the PREFETCH mechanism, the program, or one of the IOCs (cycle steal mode).
In order to increase the HSB hit ratio, the HSB is loaded with a new line only when a read miss is caused by an I-fetch or a program read. Any other storage user causing a read miss results in the data being loaded directly from memory to the CCU without HSB involvement.

Line Invalidation

Because of DMA operation, the SCTL requests the HSB to invalidate a line. An invalidation request has priority over a CCU request.

When a line invalidation is requested, the SCTL raises the 'line INV' line which instructs the HSB not to propagate SAR to the SAD bus and to latch the address presented by the SCTL. In the cycle following the address transfer, the HSB invalidates the line in the HSB and the SCTL ignores requests at the interconnection.

Storage Protection

Storage Protect/Address Exception (SP/AE)

Storage protect is a means of notifying the control program whenever the contents of storage are accessed for unauthorized modification or unauthorized code execution. Attempts to modify storage and attempts to execute instructions are monitored by the following three mechanisms:

1. Address exception based on address exception key.
2. Storage protect based on read-only key.
3. Storage protect based on storage protection key and user key.

Main Storage Protection State

With the storage protect/address exception mechanism, a main storage position can be placed in any of the following states:

- Write free
- Write and instruction fetch controlled
- Read-only
- Write/read forbidden.

SP/AE Instructions

The CCU controls the SP/AE mechanism with the input X'73' and output X'73' instructions.

SP/AE Keys

Address Exception Key This key indicates whether an 8KB block of storage is accessible.

Read Only Key This key indicates whether a 4KB block of storage is in the read only state. For example, machine configuration data is placed in such a storage block.

Storage Protection Key: This key determines the key value (3 bits) for writing in a defined 4KB block of storage.

User Key: Every user is assigned a 3 bit register that holds the storage protection key it must use for writing in storage and fetching instructions for execution.

For more details, refer to the *Principles of Operations*, GA33-0102.

SP/AE Key Locations

The storage keys are located in a local storage (storage key RAM) and the user keys are located in registers.

To perform the necessary initialization, the program must execute output X'73' instructions for setting the storage keys for all installed 4KB blocks of storage and up to 6 output X'73' instructions for setting the user keys.

CCU Timers

Two timers are available in the CCU. They are the 100 ms interval timer and the high/low resolution timer.

100 ms Interval Timer

Every 100 ms, this timer requests a CCU level 3 interrupt. Output X'77', byte 1, bit 1 ON is used to reset the timer interrupt. The 100 ms timer is used to:

- Maintains a count of real time in storage
- Perform long and short time outs
- Perform supervisory functions on a cyclical basis.

High/Low Resolution Timer

The high/low resolution timer does not raise any interrupts. It is driven by CCLK pulses (every 75 ns for TCM or 56 ns for PUC). Output X'7A' selects the mode and initializes the current timer value to X'00'; input X'7A' reads the current timer value.

CCU to/from Adapters (CA-LA)

The CCU interconnects with the various adapters via the IOC1 and IOC2 buses and the switch logic (SWL). See Chapter 3, “Buses and Bus Switching” on page 3-1 for details.

IOC Control Logic

Data, address, and control information exchanges take place between the CCU work registers and the adapters attached to the I/O buses. They use the IOC1 and IOC2 control logic.

The IOC logic, located in the TCM or the PUC card, operates in two different ways, depending on whether the program initiates the operation (PIO), or an adapter initiates it (AIO).

The data bus carries interrupt requests from the adapters (levels 1, 2, and 3) when it is not busy with PIO or AIO operations.

IOC Data Flow

The I/O bus is an 18-bit (16 for data + 2 for parity) bidirectional bus with necessary tags and controls.

- **D - Register:** It is an 18-bit (16 for information + 2 for parity) register. It is the buffer used with the IO Bus for the exchange of all addresses, commands and data to and from the adapters.
- **A - Register:** It is a 27-bit (24 for information + 3 for parity) register. In an IOH/IOHI operation it is loaded by the R1 field. In AIO operation it contains the cycle steal address.

  The IOC Bus operations are under the control of the 'IOC control logic' using a handshaking protocol between the CCU and the adapters.

LVL2 and LVL3 Interrupt Reporting

1. IOC1 byte 1, bit 0 and IOC2 byte 1, bit 0 are ORed to produce a single CA LVL3 interrupt request to the CCU.
2. IOC1 byte 0, bit 1 and IOC2 byte 0, bit 1 are ORed to produce a single LA LVL2 interrupt request to the CCU.
3. After interrupt recognition, the CCU executes an input X'77' instruction to identify the LVL2 and 3 interrupt request origin. (See IN'77' in this chapter.)

IN '77' byte 0 is dedicated to level 2 interrupts, and byte 1 to level 3. In each case, bits 0 and 1 define which bus must be selected. There is always one and only one of these bits ON, even when there are simultaneous interrupts on both buses.

To be able to decide on the IOC selection, the hardware uses a latch (one for each level) to remember which IOC has been previously selected.

For instance:

LATCH = 1 if IOC1 last selected

LATCH = 0 if IOC2 last selected.

The IN '77' bits are then set according to the logical rules:

IOC1 select = (IOC1 INT.) and (LATCH=1 or NO IOC2 INT.)

IOC2 select = (IOC2 INT.) and (LATCH=0 or NO IOC1 INT.).

and the LATCH is then updated at IN '77' time according to the current IOC selection.

LVL1 Interrupt Reporting

1. IOC1 bus byte 0, bit 5 and IOC2 byte 0, bit 5 are ORed to produce a single CA LVL1 interrupt request.
2. IOC1 bus byte 1, bit 5 and IOC2 byte 1, bit 5 are ORed to produce a single LA LVL1 interrupt request.
3. After interrupt recognition, the CCU executes an input X'7E' instruction to identify the LVL1 interrupt request origin. (See IN'7E' in this chapter.)
4. When the CCU executes the input X'76' instruction, the bit assignment of byte 0 is for IOC1 and the bit assignment of byte 1 is for IOC2.

Cycle Steal Pointer Allocation

Each IOC bus may address up to eight channel adapters. The cycle steal pointer registers are allocated as follows:

Adapter	IOC 1	IOC 2	Pointer type
CAs	30 - 37	60 - 67	Dedicated (NCP)
LAs	3F	6F	Shared pointer

For IOC2, when a cycle steal is initiated, the ROS immediate field, X'6' (as opposed to X'3' for IOC1), is concatenated to the value found in CSCW bits 11-14 (received from the adapter) to produce the pointer register address.

For all AIO operations, bit 5 (equal 0 for CA and 1 for LA) and bits 11-14 (pointer number if bit 5 = 0 and scanner ID if bit 5 = 1) of the CSCW are stored in an external register accessible by the control program using input X'75'. (See IN'75' in this chapter.)

Reset AIO, Stop AIO

See: OUT X'76' and OUT X'79' in this chapter.

Registers

The controller has two types of register: general and external.

General Registers

Forty general registers are available in the controller for program use. The size of each register is 24 bits. The bits are assigned from left to right as byte X, bits 0-7; byte 0, bits 0-7; and byte 1, bits 0-7.

The forty registers are divided into five groups of eight registers each. Each group is assigned to a specific program level. Only one group of general registers is active at a given time (the group associated with the active program level). The registers within the currently active group are directly addressable with program instructions. The control program can access the general registers by specifying them as external registers in input and output instructions.

Instruction Address Register

General register 0 in each group is the instruction address register (IAR). This register is an implied base register and contains the address of the next instruction to be executed for the associated program level. Register 0 of the active group is always incremented to point to the next sequential instruction before the current instruction is executed. However, execution of a branch instruction can cause the IAR to be loaded with a storage address other than that of the current instruction.

External Registers

External registers are registers which are not directly accessible by the control program. Therefore, by using an input instruction, the control program can load the contents of an external register into a general register where it can operate on the data. By using an output operation, the control program can load an external register with the contents of the general register specified in the instruction.

CCU external registers are located in:

- The Local Store (LS address 00 to 7F)

  The local store registers at address X "00 to 27" are the five groups of eight general registers. Each group is associated to one program level.

- The hardware registers:
  - 7 work registers
  - Instruction Address Register (IAR)
  - Lagging Address Register (LAR).

  See “Hardware Registers” on page 2-44 for details.

- Hardware latches

The following tables list the input and output instructions.

Input Instructions

Input	Register/Function	Loc Stor Reg
00 - 07	Gen Reg Group 0 (level 2)	00 - 07
08 - 0F	Gen Reg Group 1 (level 3)	08 - 0F
10 - 17	Gen Reg Group 2 (level 4)	10 - 17
18 - 1F	Gen Reg Group 3 (level 5)	18 - 1F
20 - 27	Gen Reg Group 4 (level 1)	20 - 27
28 - 2F	Not used	
30 - 37	IOC1-CA Pointer Reg 0-7	30 - 37
38 - 3E	Not used	38 - 3E
3F	IOC1-LA Pointer Reg F	3F
40	Prog Int Start Adr. Lvl 1	40
41	" " " " Lvl 2	41
42	" " " " Lvl 3	42
43	" " " " Lvl 4	43
44	Byte-Addressable Base Reg	44
45	Halfword " " "	45
46	Fullword " " "	46
47	CCU SCTL/HSB Control	47
48	IOH TA substitution	48
49 - 4F	Not used	
50 - 5F	Reserved for program use (see Note 1)	50 - 5F
60 - 67	IOC2-CA Pointer Reg 0-7	60 - 67
68	Zero Reg	68
69	Holding Reg for IOH, IOHI, BAL instr.	69
6A	Holding Reg for MOSS IOH	6A
6B	Holding Reg for IOH I	6B
6C - 6E	Not used	
6F	IOC2-LA Pointer Reg F	6F
70	Storage size installed	Hardware Reg
71	Operator Add/Data Entry Reg	71
72	Operator Function Select Controls	72
73	Read SP/AE key	Hardware Reg
74	LAR	Hardware Reg
75	AIO CCW	Hardware Reg
76	IOC Level 1 Interrupt Requests	Hardware Reg
77	Adapter Level 2, 3 or 4 Inter Requests	Hardware Reg
78	Not used	
79	Utility	Hardware Reg
7A	High resolution timer	Hardware Reg
7B	Branch Trace Address Pointer	7B
7C	Branch Trace Buffer Count	7C
7D	CCU Hard Errors Register	Hardware Reg
7E	Level 1 Interrupt Requests	Hardware Reg
7F	CCU Level 2, 3 or 4 Interrupt Requests	Hardware Reg

Notes:

1. Unassigned fullword registers are available for the program at this location.
2. If the control program tries to read locations 28-2F, 38-3E, 49-4F, 6C-6E, 78 an invalid operation condition is detected and a level 1 interrupt is set.

Output Instructions

Outputs	Register/Function	Loc Stor Reg
00 - 07	Gen Reg Group 0 (level 2)	00 - 07
08 - 0F	Gen Reg Group 1 (level 3)	08 - 0F
10 - 17	Gen Reg Group 2 (level 4)	10 - 17
18 - 1F	Gen Reg Group 3 (level 5)	18 - 1F
20 - 27	Gen Reg Group 4 (level 1)	20 - 27
28 - 2F	Not used	
30 - 37	IOC1-CA Pointer Reg 0-7	30 - 37
38 - 3E	Not used	38 - 3E
3F	IOC1-LA Pointer Reg F	3F
40	Prog Int Start Adr. Lvl 1	40
41	" " " " Lvl 2	41
42	" " " " Lvl 3	42
43	" " " " Lvl 4	43
44	Byte-Addressable Base Reg	44
45	Halfword " " "	45
46	Fullword " " "	46
47	CCU SCTL/HSB Control	47
48	IOH TA substitution	48
49 - 4F	Not used	
50 - 5F	Reserved for programs use	50 - 5F
60 - 67	IOC2-CA Pointer Reg 0-7	60 - 67
68	Zero Reg	68
69	Holding Reg for IOH,IOHI, BAL instr.	69
6A	Holding Reg for MOSS IOH	6A
6B	Holding Reg for IOH I	6B
6C - 6E	Not used	
6F	IOC2-LA Pointer Reg F	6F
70	Hard stop	Hardware Reg
71	Display reg. 1	Hardware Reg
72	Display reg. 2	72
73	Write/Select SP/AE key	Hardware Reg
74	Storage Control	Hardware Reg
75	Not writable	
76	Miscellaneous Control	Hardware Reg
77	" "	Hardware Reg
78	Force ALU check	Hardware Reg
79	Utility	Hardware Reg
7A	Utilisation counter	Hardware Reg
7B	Set PCI level 2	Hardware Reg
7C	Set PCI level 3	Hardware Reg
7D	Set PCI level 4	Hardware Reg
7E	Set Mask bits	Hardware Reg
7F	Reset Mask bits	Hardware Reg

Notes:

1. Unassigned fullword registers are available for the program at this location.
2. If the control program tries to write locations 28-2F, 38-3E, 49-4F, 6C-6E an invalid operation condition is detected and a level 1 interrupt is set.

Input/Output '7X' Instructions

The control program uses input and output instruction to access CCU registers and/or to control and monitor the status of the CCU.

Input Instructions

- **Input X'70'** (Storage Size Installed):
  This instruction loads a general register with a combination of bits that indicates the amount of storage installed.
- **Input X'71'** (Operator Address/Data Entry Reg):
  This instruction loads a general register with a combination of bits to indicate data to be used in a control panel function.
- **Input X'72'** (Operator Function Select Control):
  This instruction loads a general register with a combination of bits to indicate the Operator Display/Function Select. Through the use of this instruction, the program can accept information from the operator.
- **Input X'73'** (Read SP/AE Key):
  This instruction loads a general register with the Storage Protect/Address Exception key addressed by the last Output X'73' instruction executed.
- **Input X'74'** (Lagging Address Register):
  This instruction loads a general register with the contents of the lagging address register. When this input is executed, the address transferred into the general register is that of the last instruction executed before the input instruction (this might not be true in case of error: refer to *Principles of Operations*.)
- **Input X'75'** (AIO CCW):
  This instruction loads a general register with bits of the CCW received by the IOC for an AIO which has been suspended/stopped due to an error detected by the hardware. Otherwise, the data loaded in this general register is NOT valid.
- **Input X'76'** (IOC LVL 1 Interrupt Requests):
  This instruction loads a general register with information that can be used to determine the type of error encountered.
- **Input X'77'** (Adapter level 2, 3, or 4 Interrupt Requests):
  This instruction loads a general register with information that can be used to determine which adapter type caused a level 2, 3, or 4 interrupt.
- **Input X'79'** (Utility):
  This instruction loads a general register with utility information. When it is executed in program level 1, byte 1, bits 0-3 designate the program level that was operating before the level 1 interrupt. When it is executed in program levels 2, 3, or 4 (or level 1 if level 1 is re-entered immediately after a level 1 exit), byte 1, bits 0-3 have no significance and are set to zero. When input X'79' is executed at any level, byte 0, bits 6 and 7 indicate the state of the program level 5, C, and Z condition latches.
- **Input X'7A'** (High Resolution Timer):
  This instruction loads a general register with the high resolution timer.

- **Input '7B'** (BT ADR Pointer):
  This instruction loads a general register with the branch trace address pointer.
- **Input '7C'** (BT Buffer Count):
  This instruction loads a general register with the branch trace buffer count.
- **Input X'7D'** (CCU Hard Errors Reg):
  This instruction loads a general register with information showing which CCU hard error has been detected.
- **Input X'7E'** (PGM Level 1 Interrupt Requests):
  This instruction loads a general register with bits to indicate interrupt requests for program level 1 interrupt. Also shown is the CCU hard error summary bit.
- **Input X'7F'** (Level 2, 3, or 4 Interrupt Requests):
  This instruction loads a general register with bits to indicate interrupt requests for program levels 2, 3, and 4.

Output Instructions

- **Output X'70'** (Hard stop):
  This instruction causes the CCU to enter a hard stop state. In this state, program execution, program interrupts and adapter cycle steals are prevented. The bit settings of the general register are ignored.
- **Output X'71'** (Display Register 1):
  This instruction loads the contents of the general register into display register 1.
- **Output X'72'** (Display Register 2):
  This instruction causes the contents of the general register to be loaded into display register 2.
- **Output X'73'** (Read SP/AE Reg):
  This instruction causes the contents of the general register to be used to address and/or set the storage and protect keys.
- **Output X'74'** (Storage Control):
  This instruction causes the contents of the general register to be used to set the state of the HSB and the SCTL/ECC.
- **Output X'76' and Output X'77'** (Miscellaneous Control):
  These instructions cause the contents of the specified general register to be used to set or reset various interrupt requests.
- **Output X'78'** (Force ALU Check):
  This instruction provides the means for testing the ALU compare circuit under diagnostic control. It causes an ALU compare check by degating one of the two redundant ALUs and forces error parity on the data at the ALU output.
- **Output X'79'** (Utility):
  This instruction causes the contents of the specified general register to set and/or reset various hardware latches.

  It permits 'Set IPL REQ' (bit 0.2). This results in an interrupt to MOSS. It does not stop the control program. If the control program is to stop after setting an IPL REQ, by using the Output X'70' instruction a hard stop must be sent by the control program in addition to output X'79'. It permits remote power off (bit 0.4). A remote power off line is sent to the power subsystem.
- **Output X'7A'** (Utilization Counter):

This instruction causes the contents of the specified general register to control the high resolution timer and the utilization counter.

- **Output X'7B'** (Set PCI L2):
  This instruction causes a program-controlled interrupt request to be set for program level 2 (PCI L2). This allows a program level to transfer a processing requirement to a different priority program level. The bit settings of the general register are ignored. A PCI interrupt request is immediately effective.
- **Output X'7C'** (Set PCI L3):
  This instruction causes a program-controlled interrupt request to be set for program level 3 (PCI L3). This allows a program level to transfer a processing requirement to a different priority program level. The bit settings of the general register are ignored. A PCI interrupt request is immediately effective.
- **Output X'7D'** (Set PCI L4):
  This instruction causes a program-controlled interrupt request to be set for program level 4 (PCI L4). This allows a program level to transfer a processing requirement to a lower priority level. The bit settings of the general register are ignored. A PCI interrupt request is immediately effective.
- **Output X'7E'** (Set Mask Bits):
  This instruction causes the mask bits of the program levels to be set according to the contents of the general register. When a mask bit is set ON, interrupt requests for the program level that corresponds to that bit are ignored. When the mask bit for program level 5 is ON, program execution at that level is not allowed.
- **Output X'7F'** (Reset Mask Bits):
  This instruction causes the mask bits of the program levels to be reset according to the contents of the general register. If an interrupt for a particular level is pending when the mask bit for that level is reset, an interrupt for that level will occur before the next instruction is executed.

Input/Output X'7X' Register Bits

X'70'	Input: Storage Size Installed	Output: Hard stop
Byte X, Bit 0	0	*
1	0	*
2	0	*
3	0	*
4	0	*
5	0	*
6	0	*
7	0	*
Byte 0, Bit 0	See Input: Byte 0 below	*
1	"	*
2	"	*
3	"	*
4	"	*
5	"	*
6	"	*
7	"	*
Byte 1, Bit 0	0	*
1	0	*
2	0	*
3	0	*
4	0	*
5	0	*
6	0	*
7	0	*

* Ignored

Storage Size	Storage Card Combination	Input: Byte 0, Bit 0 1 2 3 4 5 6 7 P
4	4	1 1 X X X 0 0 1 X
8	4-4	1 0 X X X 0 1 1 X
16	None	1 0 X X X 0 0 0 X
Illegal	Wrong	0 1 X X X X X X X

Notes:

1. Bits 0.2, 0.3, and 0.4 carry the EC level of the SCTL cards.
2. A good parity is delivered to CCUI/DMA (it includes the EC bits).
3. If no card is installed or if an illegal configuration is detected, a storage control error is reported to CCUI/DMA.
4. 16 MB storage is a feature only on 3745 Models 31A and 61A.

X'71'	Input: Oper. Add/Data (LS) Entry Reg	Output: Program Display Register 1 (DR1)
Byte X, Bit 0	Addr/Data Byte X, Bit 0	DR1 Byte X, Bit 0
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
Byte 0, Bit 0	Addr/Data Byte 0, Bit 0	DR1 Byte 0, Bit 0
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
Byte 1, Bit 0	Addr/Data Byte 1, Bit 0	DR1 Byte 1, Bit 0
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7

X'72'	Input: Operator Function Select Control	Output: Program Display Register 2 (DR2)
Byte X, Bit 0	0	DR2 Byte X, Bit 0
1	0	1
2	0	2
3	0	3
4	0	4
5	0	5
6	0	6
7	0	7
Byte 0, Bit 0	Function Select 8	DR2 Byte 0, Bit 0
1	" " 9	1
2	" " A	2
3	Storage Address	3
4	Register Address	4
5	Function Select B	5
6	" " C	6
7	" " D	7
Byte 1, Bit 0	" " E	DR2 Byte 1, Bit 0
1	Function Select 1	1
2	" " 2	2
3	" " 3	3
4	" " 4	4
5	" " 5	5
6	" " 6	6
7	" " 7	7

	Storage Protect/Address Exception	
X'73'	Input:	Output:
Byte X, Bit 0	0	SKA Bit 0
1	0	" 1
2	0	" 2
3	0	" 3
4	0	" 4
5	0	" 5
6	0	" 6
7	0	" 7
Byte 0, Bit 0	0	SKA Bit 8
1	0	" 9
2	0	" 10
3	0	" 11, UKA Bit 0
4	0	1
5	0	2
6	0	3
7	0	4
Byte 1, Bit 0	0	*
1	0	ENABLE ST PROT/ADDR EXCEPT
2	0	0 user 0 Stor 1 Excp 1 read only
3	0	0 key 1 key 0 key 1 key
4	0	Modify Key Value
5	Key value bit 0	Key value bit 0
6	Key value bit 1	Key value bit 1
7	Key value bit 2	Key value bit 2

* Not Significant
Byte 1, bit 7 = 1 means: storage not installed for exception key, if bits 2 and 3 = 10.
Byte 1, bit 7 = 1 means: prevent write for read-only key, if bits 2 and 3 = 11.

X'74'	**Input: Lagging Address Register (LAR)**	**Output: Storage Control**
Byte X, Bit 0	LAR Byte X Bit 0	See Output: Byte X below
1	1	"
2	2	"
3	3	"
4	4	"
5	5	"
6	6	"
7	7	"
Byte 0, Bit 0	LAR Byte 0 Bit 0	Reserved
1	1	"
2	2	"
3	3	"
4	4	"
5	5	"
6	6	"
7	7	"
Byte 1, Bit 0	LAR Byte 1 Bit 0	"
1	1	"
2	2	"
3	3	"
4	4	"
5	5	"
6	6	"
7	7	"

Output: Byte X, Bit	0 1 2 3 4 5 6 7
HSB Disable	0 0 0 0 X X X X
HSB Flush	1 0 X 0 X X X X
HSB Normal	0 0 0 1 X X X X
HSB Wait State	0 0 1 1 X X X X HSB FUNCTIONS
HSB Retry State	1 0 1 1 X X X X
HSB Directory Test	0 0 1 0 X X X X
HSB Data Array Test	1 0 0 1 X X X X
Disable CCUI Interface	X X X X 0 0 1 X
Bypass HSB	X X X X 0 1 1 X CCUI FUNCTIONS
CCUI Normal Operation	X X X X 0 0 0 X
DMA SP RAM INIT	X X X X 0 1 0 X
SCTL Normal Operation	0 1 0 0 0 0 0 0 for both CCUI
DISAB SCTL ERR Action	0 1 X X 1 1 X X and MCTL
ECC Disable	X 1 1 0 1 X X X
ECC Transparent	X 1 0 1 1 X X X MCTL Functions
MCTL Error Wrap	0 1 1 1 1 X X 0
ECC only Mode	0 1 1 1 1 X X 1
NO Refresh Mode	0 1 X X 1 X 1 X
Force Storage Errors	1 1 X X 1 0 0 0 Force Y.7 at 0
" " "	1 1 X X 1 0 1 0 " Y.7 at 1
" " "	1 1 X X 1 1 0 0 " Y.7 , X.7 at 0
" " "	1 1 X X 1 1 1 0 " Y.7 , X.7 at 1
" " "	1 1 X X 1 1 0 1 " Y.7, X.7 & 1.0at 0
" " "	1 1 X X 1 1 1 1 " Y.7, X.7 & 1.0 at 1

X'75'	Input: CSCW	Output: N/A
Byte X, Bit 0		
1		
2		
3		
4		
5		
6		
7		
Byte 0, Bit 0	IOC1 CSCW Bit 5 (Note 1)	
1	" " " 11 (Note 2)	
2	" " " 12 "	
3	" " " 13 "	
4	" " " 14 "	
5	0	
6	0	
7	0	
Byte 1, Bit 0	IOC2 CSCW Bit 5 (Note 1)	
1	" " " 11 (Note 2)	
2	" " " 12 "	
3	" " " 13 "	
4	" " " 14 "	
5	0	
6	0	
7	0	

Notes:

1. Bit 0 = 0: AIO from CAs.
   Bit 0 = 1: AIO from LAs.
2. Bits 1 to 4 are IOC relative address of adapter.

X'75' Register LA Addresses Decoding

Byte 0 0 1 2 3 4	Byte 1 0 1 2 3 4	IOC1 LA Number	IOC2 LA Number
1 0 0 0 0	0 0 0 0 0	01	
1 0 0 0 1	0 0 0 0 0	02	
1 0 0 1 0	0 0 0 0 0	03	
1 0 0 1 1	0 0 0 0 0	04	
1 0 1 0 0	0 0 0 0 0	09	
1 0 1 0 1	0 0 0 0 0	10	
1 0 1 1 0	0 0 0 0 0	11	
1 0 1 1 1	0 0 0 0 0	12	
1 1 0 0 0	0 0 0 0 0	17	
1 1 0 0 1	0 0 0 0 0	18	
1 1 0 1 0	0 0 0 0 0	19	
1 1 0 1 1	0 0 0 0 0	20	
1 1 1 0 0	0 0 0 0 0	25	
1 1 1 0 1	0 0 0 0 0	26	
1 1 1 1 0	0 0 0 0 0	27	
1 1 1 1 1	0 0 0 0 0	28	
0 0 0 0 0	1 0 0 0 0		05
0 0 0 0 0	1 0 0 0 1		06
0 0 0 0 0	1 0 0 1 0		07
0 0 0 0 0	1 0 0 1 1		08
0 0 0 0 0	1 0 1 0 0		13
0 0 0 0 0	1 0 1 0 1		14
0 0 0 0 0	1 0 1 1 0		15
0 0 0 0 0	1 0 1 1 1		16
0 0 0 0 0	1 1 0 0 0		21
0 0 0 0 0	1 1 0 0 1		22
0 0 0 0 0	1 1 0 1 0		23
0 0 0 0 0	1 1 0 1 1		24
0 0 0 0 0	1 1 1 0 0		29
0 0 0 0 0	1 1 1 0 1		30
0 0 0 0 0	1 1 1 1 0		31
0 0 0 0 0	1 1 1 1 1		32

X'75' Register CA Addresses Decoding

Byte 0 0 1 2 3 4	Byte 1 0 1 2 3 4	IOC1 CA Number	IOC2 CA Number
0 0 0 0 0	0 0 0 0 0	01	
0 0 0 0 1	0 0 0 0 0	02	
0 0 0 1 0	0 0 0 0 0	03	
0 0 0 1 1	0 0 0 0 0	04	
0 0 1 0 0	0 0 0 0 0	09	
0 0 1 0 1	0 0 0 0 0	10	
0 0 1 1 0	0 0 0 0 0	11	
0 0 1 1 1	0 0 0 0 0	12	
0 0 0 0 0	0 0 0 0 0		05
0 0 0 0 0	0 0 0 0 1		06
0 0 0 0 0	0 0 0 1 0		07
0 0 0 0 0	0 0 0 1 1		08
0 0 0 0 0	0 0 1 0 0		13
0 0 0 0 0	0 0 1 0 1		14
0 0 0 0 0	0 0 1 1 0		15
0 0 0 0 0	0 0 1 1 1		16

X'76'	Input: IOC L1 Interrupt Request	Output: Miscellaneous Control
Byte X, Bit 0	0	*
1	0	*
2	0	*
3	0	*
4	0	*
5	0	*
6	0	*
7	0	*
Byte 0, Bit 0	IOC1 ADDR except)	RST IOC1 Errors
1	IOC1 Storage PROT) Note	*
2	IOC1 Invalid CCW)	*
3	0	CCU Program REQ to MOSS
4	IOC1 Time out	CCU Program RESP to MOSS
5	IOC1 Bus in PTY	*
6[1]	IOC1 Adapt. INIT Operation	*
7[1]	IOC1 MOSS INIT Operation	*
Byte 1, Bit 0	IOC2 ADDR Except)	RST IOC2 Errors
1	IOC2 Storage PROT) Note	*
2	IOC2 Invalid CCW)	*
3	0	*
4	IOC2 Time out	*
5	IOC2 BUS in PTY	*
6[1]	IOC2 ADAPT. INIT Operation	*
7[1]	IOC2 MOSS INIT Operation	*

* Not Significant

[1] = This bit does not generate a Level 1 interrupt.

Note: In byte 0 or 1, if bits 4 and 5 are zero, bits 0, 1, 2, and 3 are as shown.

If bit 4 or bit 5 is one, bits 0, 1, 2, and 3 contain IOC internal status at the time of the error. (See the following table on input X'76' state meaning for time out or bus in PTY error.)

Input X'76' State Meaning for Time Out or Bus-in Parity Error

Input X'76' State Meaning: Time Out / Bus-in Parity Error

State Latch Decode	Valid Tags (See Note)	'Time out' Meanings	"Bus in PTY Error" Meanings
0	08	I/O TAG is off	No
1	10	I/O TAG raised new AIO or IOH	No
2	18-11	No response to TA or Channel Grant	No
3	-	CCW Pty error	CCW Pty error
4	10	VH didn't fall after TD fall	AIO data READ or CH pointer register READ 2nd xfer
5	18-16 11	No response to TD for AIO data read IOH data read	Bus in parity error on AIO data read, or IOH data read
6	18-16 11	No response to TD for AIO data write IOH data write	No
7	10	VH didn't fall after TD fall (byte boundary xfer with STG)	No
8	08	I/O TAG is OFF, VH must rise (EOC after CH. pointer updating in local store)	CH pointer reg read xfer last xfer (EOC)
9	10	VH didn't fall after CG fall AIO CCW: S/L or D/I.D or D/I.D.WR	No
A	08	I/O TAG is OFF, VH must rise (last AIO xfer data read is on byte boundary)	No
B	10	No	Loading of CCW
C	18-11	No response to TD for AIO pointer initialization	Bus in parity error AIO address sent to adapter during AIO direct operation
D	-	No	No
E	10	VH didn't fall after TD fall for AIO pointer initialization	CH pointer register read 1st xfer
F	08	I/O TAG is OFF, VH must rise (IOH end or AIO end after data exchange)	Last AIO data read (EOC or VB M)

Note:

Tags Encode	Tags
08	VH
10	IRR
11	IRR, EOC
16	IRR, VB, M
18	IRR, VH

'Output: Miscellaneous'

For details on I/O TAG, refer to "Chapter 3" AIO, IOH, or PIO opration.

X'77'	Input: Adapter Level 2, 3, 4 Interrupt Requests	Control
Byte X, Bit 0	0	*
1	0	*
2	0	*
3	0	*
4	0	*
5	0	*
6	0	*
7	0	*
Byte 0, Bit 0	LVL2 Bus 2 Priority	Rst IPL L1 and not init bit
1	LVL2 Bus 1 Priority	Rst CCU Hard Checks
2	LVL2 on Bus 1	Rst MOSS Panel Inter REQ L3
3	LVL2 on Bus 2	Rst MOSS Diag Req L3
4	0	Rst MOSS SVC Req L4
5	0	Rst MOSS SVC Resp L4
6	0	
7	0	Rst PCI L2
Byte 1, Bit 0	LVL3 Bus 1 Priority	Rst MOSS/Inoperative L1
1	LVL3 Bus 2 Priority	Rst Interval Timer L3
2	LVL3 on Bus 1	Rst PCI L3
3	LVL3 on Bus 2	Rst MOSS L2 Diag Request
4	0	Rst Address Compare L1
5	0	Rst Program Errors
6	0	Rst PCI L4
7	0	Rst SVC L4

* Not Significant

Byte 0 refers to level 2 and byte 1 to level 3. For each byte, bits 0 and 1 show which bus requires service based on whether one or both buses are interrupting and which was last serviced. The Priority Bits in byte 0 for level 2 are independent of those in byte 1 for level 3.

Notes:

1. The following description applies to either byte.

   One of the priority bits in a byte will be set to '1' if and only if one or both of the bus interrupt bits in that byte are '1'. However, the priority will be set one cycle after the interrupt bit(s) is set, therefore there is a 1"cycle window in which either or both interrupt bits can be '1' without either priority bit. This window occurs at the time interrupts are sampled from the adapter bus, not necessarily at Input 77 time, but may affect the result of INPUT 77.

   To avoid this window, it is recommended that the program use Input X'77' in any one of the following ways.
   a. Test only the priority bits in the appropriate byte, ignoring the interrupt bits. This will insure that single and simultaneous bus interrupts will be serviced in turn without the possibility of missed interrupts or ambiguity. In this case, there is no restriction on when Input 77 may be performed.
   b. Test only the interrupt bits, ignoring the priority bits (in this case, the program would have to decide by other means which interrupting bus to service). There is no restriction on when Input 77 may be performed.
   c. If neither procedure above is used, the use of the Input 77 instruction is restricted, as follows: Input 77 should be performed in level 2 or level 3 only if there are no non adapter interrupt(s) for that level.
      If non adapter interrupts are pending, they must be serviced and an Exit performed. In addition to this restriction, Input 77 should not be performed more than once in a level.

2. After the control program issues an IOH to clear an adapter interrupt, at least 22 CCU cycles must be performed before executing an Exit instruction or an INPUT 77/7E (Read Adapter Interrupt) instruction. This is to allow reset and resampling of interrupts from the adapters.

X'78'	Input: Unused (LS)	Output: Force ALU Check
Byte X, Bit 0		*
1		*
2		*
3		*
4		*
5		*
6		*
7		*
Byte 0, Bit 0		*
1		*
2		*
3		*
4		*
5		*
6		*
7		*
Byte 1, Bit 0		*
1		*
2		*
3		*
4		*
5		*
6		*
7		*

* Not Significant

X'79'	Input:	Output:
Byte X, Bit 0	0	*
1	0	*
2	0	*
3	0	*
4	0	*
5	0	*
6	0	*
7	0	*
Byte 0, Bit 0	0	*
1	0	*
2	0	Set Prog. IPL Req.
3	0	*
4	0	Remote Power Off
5	0	Inh. Prog. Level 5C and Z latches
6	Prog. Level 5C Condition	Prog. Level 5C Latch
7	Prog. Level 5Z Condition	Prog. Level 5Z Latch
Byte 1, Bit 0	Prog. Level 2 Int'd (1)	Set AIO stop mode on IOC2 (3)
1	Prog. Level 3 Int'd (1)	Reset AIO stop mode on IOC2 (3)
2	Prog. Level 4 Int'd (1)	Set AIO stop mode on IOC1 (3)
3	Prog. Level 5 Int'd (1)	Reset AIO stop mode on IOC1 (3)
4	0	Set Byp CCU Chk Stop (2/3)
5	0	Rst Byp CCU Chk Stop (2/3)
6	0	Scope Sync Pulse 1
7	0	Scope Sync Pulse 2

* Not Significant

Notes:

1. Only one bit will be ON corresponding to the program level executing when the L1 interrupt was taken.
2. Bypass CCU checkstop mode bit is not set by the CP. This bit is for potential use by diagnostics only.
3. When there is contention between set and reset bits, the set bit has priority.

	High-Resolution Timer	
X'7A'	Input:	Output:
Byte X, Bit 0	0	*
1	0	*
2	Timer Bit 0	*
3	Timer Bit 1	*
4	Timer Bit 2	*
5	Timer Bit 3	*
6	Timer Bit 4	*
7	Timer Bit 5	*
Byte 0, Bit 0	Timer Bit 6	1=Reset Timer/Enable count
1	Timer Bit 7	0=High Res. 1=Low Res.
2	Timer Bit 8	0=Timer 1=Utiliza. Count
3	Timer Bit 9	*
4	Timer Bit 10	*
5	Timer Bit 11	*
6	Timer Bit 12	*
7	Timer Bit 13	*
Byte 1, Bit 0	Timer Bit 14	*
1	Timer Bit 15	*
2	Timer Bit 16	*
3	Timer Bit 17	*
4	Timer Bit 18	*
5	Timer Bit 19	*
6	Timer Bit 20	*
7	Timer Bit 21	*

* Not Significant

X'7B'	Input: Branch Trace (LS) Address Pointer	Output: Set PCI L2
Byte X, Bit 0	BR TRACE ADDR BIT X.0	*
1	BR TRACE ADDR BIT X.1	*
2	BR TRACE ADDR BIT X.2	*
3	BR TRACE ADDR BIT X.3	*
4	BR TRACE ADDR BIT X.4	*
5	BR TRACE ADDR BIT X.5	*
6	BR TRACE ADDR BIT X.6	*
7	BR TRACE ADDR BIT X.7	*
Byte 0, Bit 0	BR TRACE ADDR BIT 0.0	*
1	BR TRACE ADDR BIT 0.1	*
2	BR TRACE ADDR BIT 0.2	*
3	BR TRACE ADDR BIT 0.3	*
4	BR TRACE ADDR BIT 0.4	*
5	BR TRACE ADDR BIT 0.5	*
6	BR TRACE ADDR BIT 0.6	*
7	BR TRACE ADDR BIT 0.7	*
Byte 1, Bit 0	BR TRACE ADDR BIT 1.0	*
1	BR TRACE ADDR BIT 1.1	*
2	BR TRACE ADDR BIT 1.2	*
3	BR TRACE ADDR BIT 1.3	*
4	BR TRACE ADDR BIT 1.4	*
5	BR TRACE ADDR BIT 1.5	*
6	BR TRACE ADDR BIT 1.6	*
7	BR TRACE ADDR BIT 1.7	*

* Not Significant

X'7C'	Input: Branch Trace (LS) Buffer Count	Output: Set PCI L3
Byte X, Bit 0	0	*
1	0	*
2	0	*
3	0	*
4	0	*
5	0	*
6	0	*
7	0	*
Byte 0, Bit 0	|	*
1	|	*
2	|	*
3	|	*
4	|	*
5	|	*
6	|	*
7	|	*
Byte 1, Bit 0	| > Note	*
1	|	*
2	|	*
3	|	*
4	|	*
5	|	*
6	|	*
7	|	*

* Not Significant

Note: Binary indication of BT buffer size in number of bytes.

Actual length is a multiple of 8 bytes; bits 1.5, 1.6, and 1.7 are ignored by the BT mechanism.

CCU Hard Errors

X'7D'	Input: CCU Hard Errors	Output: Set PCI L4
Byte X, Bit 0	0	*
1	0	*
2	0	*
3	0	*
4	0	*
5	0	*
6	0	*
7	0	*
Byte 0, Bit 0	POP Parity Error	*
1	MDOR Parity Error	*
2	MIOC Parity Error	*
3	Storage Error 1	*
4	HSB/CCU Error	*
5	HSB/SCTL Error	*
6	Storage Error 2	*
7	Local Store Parity Error	*
Byte 1, Bit 0	HSB Internal Error	*
1	A/B Bus Parity Error	*
2	D1 Reg Parity Error	*
3	ALU Compare Error	*
4	SAR Parity Error	*
5	ROS Parity Error	*
6	Z Reg Parity Error	*
7	D2 Reg Parity Error	*

* Not Significant

Note: Byte 0, bits 3 and 6 are encoded:

If the value is 01 = Interface Error
If the value is 10 = SCTL Internal Error
If the value is 11 = Unrecoverable Storage Error.

X'7E'	Input: Level 1 Interrupt Requests	Output: Set Interrupt Mask
Byte X, Bit 0	0	*
1	0	*
2	0	*
3	0	*
4	0	*
5	0	*
6	0	*
7	0	*
Byte 0, Bit 0	MOSS Inoperative	*
1	CCU Hard Error Summary	*
2	IOC1-LA	*
3	L5IO Error	*
4	Invalid OP.	*
5	IOC1-CA	*
6	IOC2-LA	*
7	IOC1 L1 Summary	*
Byte 1, Bit 0	Adr Compare L1	*
1	Adr Except Inst Fetch	Adap. Level 1 Req
2	STG Prot. Inst Fetch	Level 2 Req
3	Adr Except PGM Exec	Level 3 Req
4	STG Prot PGM Exec	Level 4 Req
5	IOC2-CA	Prog. Level 5 execution
6	IPL L1	*
7	IOC2 L1 Summary	*

* Not Significant

Notes:

1. CCU hard error summary --> See Input 7D
2. IOC1 L1 summary --> See Input 76
3. IOC2 L1 summary --> See Input 76.

When the CCU executes the Input X'76' instructions, it reads the following IOC level 1 interrupt requests:

Byte 0 is associated with IOC1.

Byte 1 is the same as Byte 0 (same bit assignment) and is associated with IOC2.

X'7F'	Input: CCU Level 2, 3, or 4 Interrupt Requests	Output: Reset Interrupt Mask
Byte X, Bit 0	0	*
1	0	*
2	0	*
3	0	*
4	0	*
5	0	*
6	0	*
7	0	*
Byte 0, Bit 0	PCI L2	*
1	MOSS Diag L2	*
2	MOSS Diag L3	*
3	MOSS Req SVC L4	*
4	MOSS Resp SVC L4	*
5	0	*
6	CE/Oper Int. Req L3	*
7	PCI L4	*
Byte 1, Bit 0	0	*
1	0	Adap. Level 1 Req
2	0	Level 2 Req
3	0	Level 3 Req
4	0	Level 4 Req
5	Interval Timer L3	Prog. Level 5 execution
6	PCI L3	*
7	SVC L4	*

* Not Significant

Hardware Registers

Hardware registers are used to store and pass information essential to controller operation. Some of these hardware registers are available to the control program as external register addresses through the use of input and output instructions.

Instruction Address Register (IAR): See 'General Registers' above.

Lagging Address Register (LAR): The LAR is loaded from the IAR at the beginning of each instruction execution. The lagging address register is a 'came from' register. When displayed by the operator or by the program using input '74' or MOSS indirect input '74', it contains the address of the last instruction executed prior to the instruction that is currently being executed if any (this might not be true in case of error: refer to the *Principles of Operations* manual).

The control program can load the contents of the LAR into a general register by executing an Input X'74' instruction. The control program can then either examine the contents of the general register or display the address on the control panel by using the general register as input to the display registers.

Operation Register (OP REG): The operation register is used to hold the first 16 bits of the instruction being executed. This register can be displayed on the control panel.

Storage Address Register (SAR): The storage address register contains the storage address currently used or last used.

The contents of the SAR can be displayed on the control panel.

Program Display Register 1: This register in local storage (LS ADDR = 79) contains a parameter passed from the program running in the CCU to the program running in MOSS for eventual display as display register 1, to an operator.

It can be loaded by executing an output X'71' Instruction.

Program Display Register 2: This register in local storage (LS ADDR = 7A) contains a parameter passed from the program running in the CCU to the program running in MOSS for eventual display as display REG 2 to an operator.

It can be loaded with data by executing an Output X'72' instruction.

Operator Add/Data Value Register: This register in local storage (LS ADDR = 71) contains a parameter passed from the program running in MOSS to the program running in the CCU when an operator wishes to express an address or data value.

It can be read by executing an input X'71' instruction.

Operator Function Select Value Register - 16 Bits: This register in local storage (LS ADDR = 72) contains a parameter passed from the program running in MOSS to the program running in the CCU when an operator wishes to express a selected function value.

It can be read by executing an input X'72' instruction.

Maintenance Temporary Address Register (MTAR): This register in local storage (LS ADDR = 7E) contains the main storage address used by any operation initiated by the program running in MOSS and involving main storage.

Maintenance Temporary Data Register (MTDR): This register in local storage (LS ADDR = 7F) contains information read out of main storage for the operations described in the section on maintenance temporary address register.

CCU to/from MOSS

The CCU interconnects with the MOSS via the MOSS Input Output Controller (MIOC) logic located in the TCM or the PUC card.

The MIOC enables the MOSS to:

- Read or write any register or storage location in the CCU.
- Set or reset all discrete CCU latches and read out their status.
- Interrupt the CCU (CCU hardware errors, IPL request, and so on).

Also, the MIOC allows the CCU to interrupt the MOSS.

See Chapter 8, “Maintenance and Operator Subsystem (MOSS)” on page 8-1 for details.

CCU Diagnostics

The CCU has diagnostic facilities designed to allow the program to perform test procedures on the controller hardware. The test routines can be either part of the online control program or a stand-alone control program used for testing purposes only. If these test routines are part of the online control program, the telecommunication lines and adapters not being tested are allowed to continue operating.

The following operations are available for program use:

1. Set and reset the bypass CCU check stop mode. Output X'79', byte 1, bit 4 set to 1 prevents CCU hard stop and MOSS interrupt from being set due to a CCU hard check. To reset the bypass mode, the control program must execute an output X'79' instruction with byte 1, bit 5 set to 1.

   However, MOSS can also issue a bypass CCU check stop or a CCU hard stop. The following table shows the resulting CCU mode.

MOSS	PGM	CCU Mode Result
-	-	Normal *
-	Bypass	Bypass
Bypass	-	Bypass
Bypass	Bypass	Bypass
Bus stop (1)	-	Normal *
Bus stop (1)	Bypass	Normal *
Bus stop and Bypass		Bypass

   * See “CCU Error Handling” and “Program Errors” on page 2-51.

   (1): Adapter interface check stop causes adapter interface errors to be handled as hard errors.

2. Set and reset the L1 adapter mask. Program level 1 interrupt requests caused by a check condition in an adapter (scanner or CA) can be masked by using an output X'7E', byte 1, bit 1. To unmask the level 1 requests, the control program must execute an output X'7F' (reset mask bits) with byte 1, bit 1 set to 1.
3. Force CCU checks. The control program can use the output X'78' instruction which will result in an ALU compare error and wrong parity on ALU result.

CCU Error Handling

The following are the basic principles of the CCU error handling strategy:

- CCU-detected hard errors:

  They are high severity errors, usually hardware failures. They stop the CCU. No retry is performed. The error indication latches are sensed by MOSS through the LSSD path.

- CCU-detected non-hard errors:

  They are low severity errors, either program errors, or UC bus errors, or MOSS 'interconnection' errors. They do not stop the CCU. They can be encountered during the following operations:

  1. MOSS operations through the MIOC or adapter operations (AIOs) performed with the MOSS flag.

These errors are reported to MOSS only.

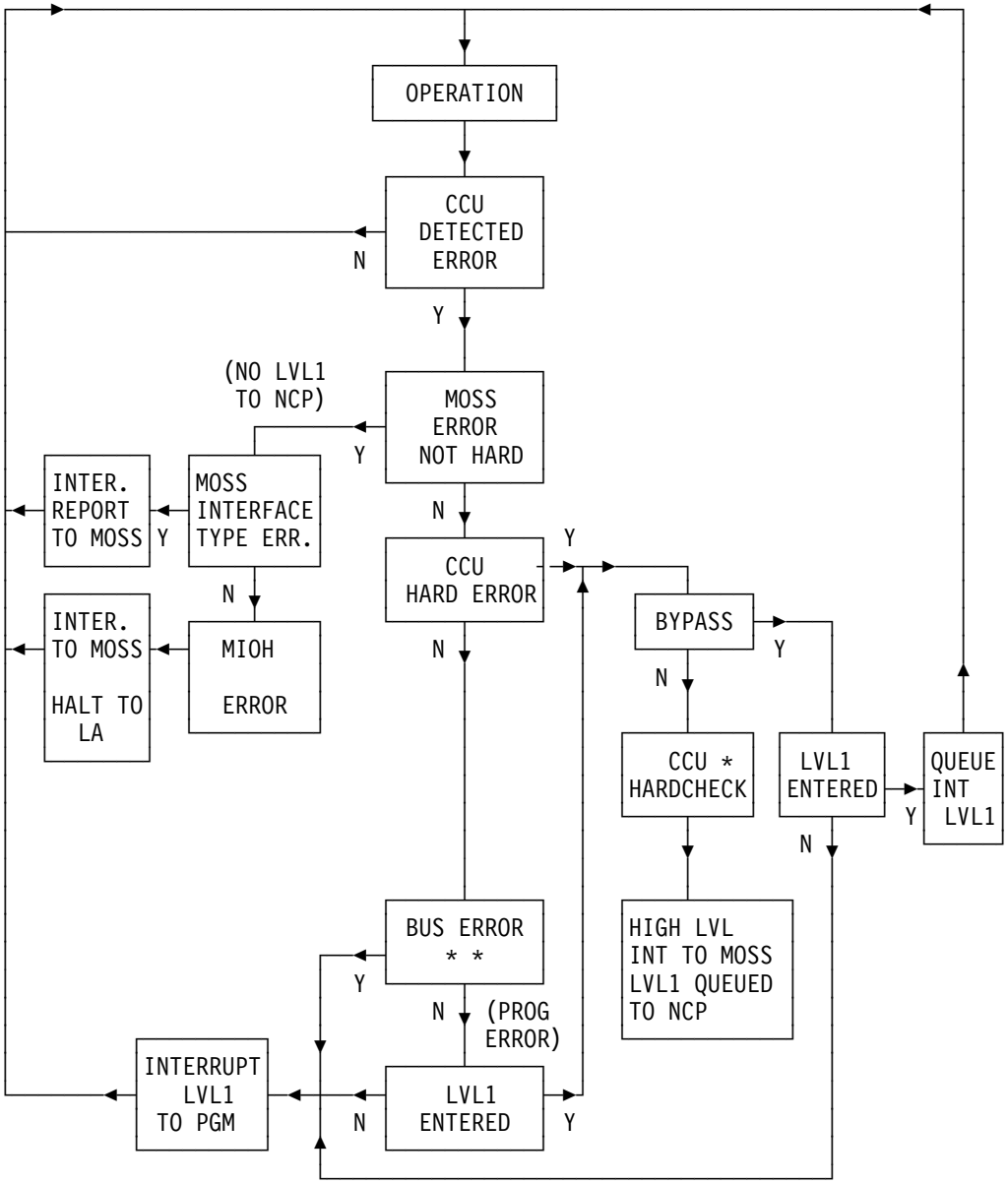
2. Program instructions and adapter operations (non-MOSS):

   These errors are reported to the program only.

Checking the Checkers

- All but 'ALU compare' checkers can be checked by the LSSD 'scan' path.
- The 'ALU compare' checker can be checked by using the output X'78' instruction.
- Additional checking can be performed using the data with bad parity available at the ALU output and resulting from the Output X'78' instruction, execution.

CCU Error Handling Summary



* Note: CCU hard check results in stopping the program, AIOs, and branch trace.

** Note: Bus error without adapter interface check stop mode.

CCU Error Detection

Hardware Errors

1. Control ROS parity error:

   Parity error detected on one of the CCU control word registers (latches receiving one ROS field).

2. MOSS data operant register (MDOR) parity error:

   Parity error during a read MDOR operation on the MDOR-to-MOSS bus.

3. MIOC parity error:

   Parity error during MOSS write operation.

4. Local storage parity error:

   Parity error detected on data bytes 0 or 1 of the local storage during a read operation.

   Possible parity error on byte X is not detected.

5. D1/D2 register parity errors (2 errors):

   Parity error detected in the IOC 1 or 2 D register after each register setting (except when set from adapter bus which results in putting the bus in parity check).

6. A/B bus parity error:

   Parity error detected on either the A bus or B bus during an ALU operation (other than 'degate' or 'pass' on the other bus).

7. Z register parity error:

   Parity error detected on any byte X 0 or 1 in the Z register except during input X'7X' instruction execution.

8. ALU compare error:

   Redundant ALU results are unequal (at any time).

9. POP parity error:

   Parity error detected in the pre-OP register (containing the prefetched instruction) before transferring its contents to the OP register.

10. SAR parity error:

    Parity error detected in the storage address register at any time.

For other parity errors, see “CCU Hard Errors” on page 2-42.

Note: At storage initialization time unrecoverable storage errors are inhibited and storage write operations are not prevented when ECC disable is set (see OUT X'74').

Handling: These errors are latched inside the CCU. A CCU hard check condition is detected, which stops the CCU, that is:

- Program stop
- AIO stop
- Hard stop

- MOSS direct operations are allowed. Indirect MOSS operations may be performed if the CCU is in bypass hardcheck mode.

A high level interrupt is sent to the MOSS.

An interrupt level 1 to the control program is queued but not executed unless in bypass check stop mode.

When the CCU is stopped the LSSD path is used by the MOSS to collect the error information from the CCU error latches through the 'scan out' line.

This error information can be made available to the operator by MOSS.

When these error latches are set by errors (not forced by diagnostics) they are unavailable to the control programs which reside in main storage.

After error information collection, MOSS may cause a re-IPL to take place.

Program Errors

1. Storage protect program execution error:

   Storage protect keys mismatch or read-only key violation during a program storage instruction.

2. Address exception program execution error:

   Program attempt to read or write uninstalled storage.

3. Storage protect instruction fetch error:

   Attempt to execute an instruction fetched from a storage area whose key did not match the program user key.

4. Address exception instruction fetch error:

   Attempt to execute an instruction fetched from an uninstalled storage location.

5. Level 5 I/O error:

   Attempt to perform an input/output instruction in program level 5.

6. Invalid Op-Code:

   Attempt to execute an instruction with an op-code that does not compare to any of the 53 valid op-codes, or input/output instruction to invalid external register addresses.

Handling: These errors result in an interrupt level 1 sent to the control program except if already in program level 1 (in this case a CCU hard check condition occurs).

Error information can be obtained by the control program using the input '7E' instruction (see “Input Instructions” on page 2-28).

However, storage protect/address exception errors are unrecoverable in program execution (load/store instruction) because, in some cases, the next instruction will be executed before the interrupt to program level 1.

For details on DMA storage protect, see Chapter 6, “High Performance Transmission Subsystem (HPTSS)” on page 6-1.

Adapter Interconnection Errors

1. IOC adapter bus parity error:

   Parity error detected when reading the IOC bus.

2. IOC time out error:

   Erroneous timing sequence on UC interface.

3. IOC adapter CCW error:

   Invalid channel control word coming from the adapter.

4. IOC storage protect error:

   Storage protect violation detected during an adapter-initiated operation (AIO) write.

5. IOC address exception error:

   Attempt to read or write storage not installed during an adapter-initiated operation.

Notes:

1. Parity and time out errors can be encountered with program user (IOH, IOHI) or with MOSS user (MIOH).
2. All errors can be encountered with AIOs.
3. In adapter interface check stop mode these bus errors are handled as hard errors.

Handling

1. With program user (IOH, IOHI):

   These errors result in an interrupt level 1 sent to the program, and a 'halt' signal is sent to the adapter. Error information can be obtained by the control program, using the input '7E' and input '76' instructions.

2. With MOSS user (MIOH):

   (MOSS IOCs OP ERROR)

   These errors result in a high level interrupt to MOSS and a 'halt' signal is sent to the adapter. No level 1 interrupt will be issued by the LAs in this case. Error information can be obtained by MOSS, using the input '76' instruction.

3. During program AIOs:

   These errors result in an interrupt level 1 to the control program and a 'halt' signal is sent to the adapter. No level 1 interrupt will be issued to the MOSS by the LAs.

   Error information can be obtained by the control program, using input '7E' and Input '76' instructions.

   The adapter address will be obtained by the program, using the input '75' instruction which allows sensing the CCW bits.

4. During MOSS AIOs:

   These errors during an adapter AIO operation for MOSS will result in a halt signal sent to the adapter. These AIOs are differentiated from the program AIOs by bit 1.0 of the CSCW which is equal to 1 for MOSS.

A high-level interrupt is sent to MOSS, if the error occurs after the CCW is transferred.

5. Adapter interface check stop mode:

   When the CCU is in adapter interface check stop mode, that is, when MOSS has sent the adapter interface check stop bit, any UC bus error encountered with any user will be handled like a hard error.

Note: Error detected during MOSS operations (MIOH) are not reported to the control program.

Error detected during control program operations (MOSS AIOs) are not reported to the MOSS.

Summary of Actions Taken During AIOs and PIOs

Event	Action In			
	AIO for Pgm	AIO for MOSS	IOH/IOHI	MIOH
AIO Stop (by MOSS)	Mask Ch Req *	Mask Ch Req *	Mask Ch Req *	Mask Ch Req *
SP/AE violation	Halt to AD LVL 1	Halt to AD HLIR to MOSS	LVL 1 (when I fetch)	Not available
Adr. Compare Stop	MASK Ch Req *	Mask Ch Req *	Mask Ch Req *	Not available
Adapt. Bus Error (WO AD bus check stop mode)	Halt to AD LVL 1	Halt to AD HLIR to MOSS	Halt to AD LVL 1	Halt to AD HLIR to MOSS
Hard Check	Halt to AD Mask Ch Req *	Halt to AD Mask Ch Req *	Halt to AD Mask Ch Req *	Halt to AD Mask Ch Req *

* "Mask Ch Req" means "Mask Channel Request" for AIOs, that is, AIO stop is set.

'MOSS Interconnection' Type Errors

1. MOSS interconnection parity error:
   - Parity error detected either on MOSS address bus or on MOSS data bus during a write operation.
   - Parity error detected on MOSS address bus during a read operation.
2. MOSS OP error:

   Moss initiates an indirect operation while the CCU busy bit is ON, meaning that CCU resources are already used for a previous MOSS indirect operation.
3. MOSS address exception (AE) error:

   MOSS attempted to read or write storage which is not installed.

Handling: These errors result in a high-level interrupt to MOSS (for MOSS OP error and MOSS AE error), or in a signal returned to MOSS through an interface line (for MOSS interface parity error).

Problem Isolation Procedure for 21x-to-41x or 31x-to-61x Model Upgrade

The following procedure helps the CE to isolate problems after a CCU upgrade from model 21x to 41x or model 31x to 61x.

For bus connection layout, see “Bus Data Flow” on page 3-27.

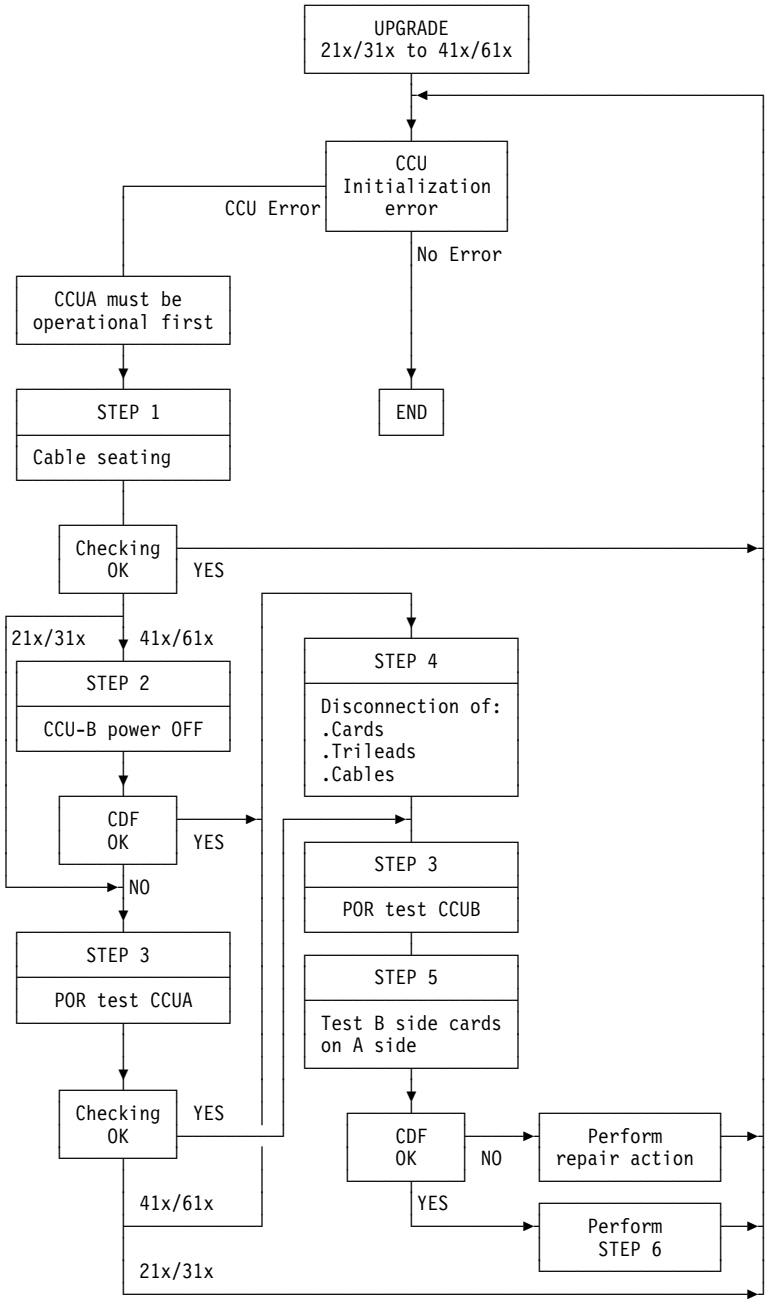


Figure 2-2. Problem Isolation Procedure for 21x-to-41x or 31x-to-61x Model Upgrade

STEP 1

The CDF messages are displayed:

CCUA INITIALIZATION ERROR
CCUB INITIALIZATION ERROR

Cable seating

Verify cable seating.

Check the label and the presence of each cable listed below:

Model 21x or 41x

- Trileads CCU board-SACL (see YZ033-1 and YZ034-2)
- Trileads CCU board-MOSS board (see YZ034-2 and YZ031)
- Flat cables SACU-MOSS board (see YZ031 and YZ032-2)
- Black cables PS1-SACL-CCU board (see YZ033-2 and YZ034-1)
- Black cables SACL-MAC card (see YZ033 and YZ731)
- Flat cables SACL (see YZ033)
- Flat cables SACU (see YZ032)
- Flat cables CCU board (see YZ034).

Model 31x or 61x

- Flat cables SACU2-MOSS board (see YZ031 and YZ032-2)
- Black cables PS1B-SACL2 (see YZ023 and YZ034-1)
- Flat cables SACU2 (see YZ022)

STEP 2

1. Set CP8 on the primary power box to the OFF position.
2. At the MOSS console call the POS (power services).
3. Select option C (create new configuration table) with answer Y (yes).
4. Press PF6, then 1 (display 3745 base frame).
5. Verify that PS ID 3 is suppressed from the table.

Next action is to run CDF upgrade. See Figure 2-2 on page 2-55.

STEP 3

Voltage Test Points

Verify the presence of all needed voltages on the following boards:

- SACU, SACL, CCU (see YZ333 or YZ323)
- MOSS (see YZ331).

POR test

Perform the POR test. Refer to 10-53 for POR layout.

At SCTL input:
With an analog scope, probe the POR SACL board (01B-A2 Z4D). It is necessary to probe the copper part of the back connector (2 wires) when it is correctly seated on the board.

The control panel must have been previously set to service mode 1 and function 0, then each POR action at the control panel will result in a power ON reset pulse to the CCUs.

- Inactive level : + 3 V (minimum level 2.4V)
- Active level : Ground (maximum level 0.8V)

+ 3 V developed from SCTL card

This signal is activated for 10 to 100 ms.

Note: A digital/analog voltmeter may be used for measurement but without the same accuracy.

Reset pulse problem:

Unplug connector 01B-A2/Z4 on SACL, then verify the POR activity with the scope (+ current voltage, 0 V).

- If it is still not correct:

  Exchange the PS1/cable.

- If it is correct continue:

For models 21x and 41x only: At SCTL output
Probe with an analog scope on SACL board pin Q0 A12 for CCU-B or F0 A12 for CCU-A.

- Inactive level : - 1 V
- Active level : - 2 V

If the POR is not correct, exchange the SCTL card. If it is still not correct, unplug trilead cable 01B-A2 P0 A1 and verify the POR.

- If correct, the suspected components are: trilead cables, CCU board, SACU board and the SACL board.
- If not correct, the suspected components are the SACU and SACL boards.

For models 31x and 61x only: At SCTLx output
Probe with an analog scope on SACL board pin S0 Y45 for CCU-B (or C0 Y45 for CCU-A).

- Inactive level : + 3 V (minimum level 2.4V)
- Active level : Ground (maximum level 0.8V)

- If it is not correct, exchange the SCTLx card.
- If it is still not correct suspect PUC, STOs, SACU2, SACL2.

STEP 4

If CCU-A fails with CCU-B powered Off:

Disconnection procedure:

1. Remove the CCU-B cards from the SAC cage. Run the CDF upgrade.
   - If correct, plug the cards back in one by one to find the bad card.
   - If not correct, continue.
2. Remove trilead cables on the SACL and MOSS boards. Run the CDF upgrade
   - If correct, suspect bad cables.
   - If not correct, continue.
3. Power the 3745 OFF. Exchange the MAC card. Power the 3745 ON and run CDF upgrade.
   - If correct, the MAC card was defective.
   - If not correct, a defective board can be suspected. Look for bent pins on the MOSS board, and the SACU, SACL boards (cable connectors and ZIF connectors), and CCU board.

STEP 5

CCU-B Card Test

Machine state is:

- Single CCU-A is working correctly (CDF + IPL).
- Remove the SCTL, STO, IOSW, DMSW cards from CCU-A.
- Remove the SCTL, STO, IOSW, DMSW cards from CCU-B and them instal in CCU-A locations.

Run the CDF upgrade with CCU-B cards installed in the CCU-A locations and CCU-B powered Off.

- If CDF upgrade is correct, cards now on CCU-A locations are not failing. Go to step 6 to continue.
- If CDF upgrade is not correct, continue with the "Repair Action" to isolate the failing card(s).

Repair Action

Using cards originally in CCU-A, replace SCTL and STO cards now in CCU-A locations. Run the CDF upgrade on A side.

- If not correct, isolate the failing card by swapping.
- If correct, and using cards originally in CCU-A, swap the IOSW and DMSW cards and run the CDF upgrade to isolate the failing card.

Run CCU-A diagnostics.

STEP 6

Machine state is:

- Single CCU-A is working correctly (CDF + IPL).
- B side cards tested on A side.
- Cables correctly seated and voltages correct on all boards.
- CCU POR tested correctly on the SACL board.

The suspected failing components on the B side are:

- TCM B side / CCU board (model 41x)
- PUC (model 61x)
- MOSS board
- SACU or SACL
- Cables (trileads, flat).

For model 41x only: Plug the flat cable between the MOSS and the IOSW B side on the A side (MOSS 01A-YE3 to SACU 01B-P0W3)***:*** Run the CDF upgrade to test it:

- If not correct, exchange the cable.
- If correct, continue.

Put the B side TCM on the A side and run CDF to test it:

- If not correct, exchange the TCM.
- If correct, continue.

Set CP8 ON. Disconnect all trilead cables on SACL board position N0 (cables between CCU-B and IOSW-B). Power the 3745 ON. Calling the POS function, perform a create and put PS3 UP.

Run CDF upgrade.

- If correct, the MOSS/CCU-B and MOSS/IOSW-B paths are checked. Parts to be suspected: trilead cables, SACL board, CCU-B board.
- If not correct, call the support.

Chapter 3. Buses and Bus Switching

The Buses and Bus Switching in 3745 Data Flow

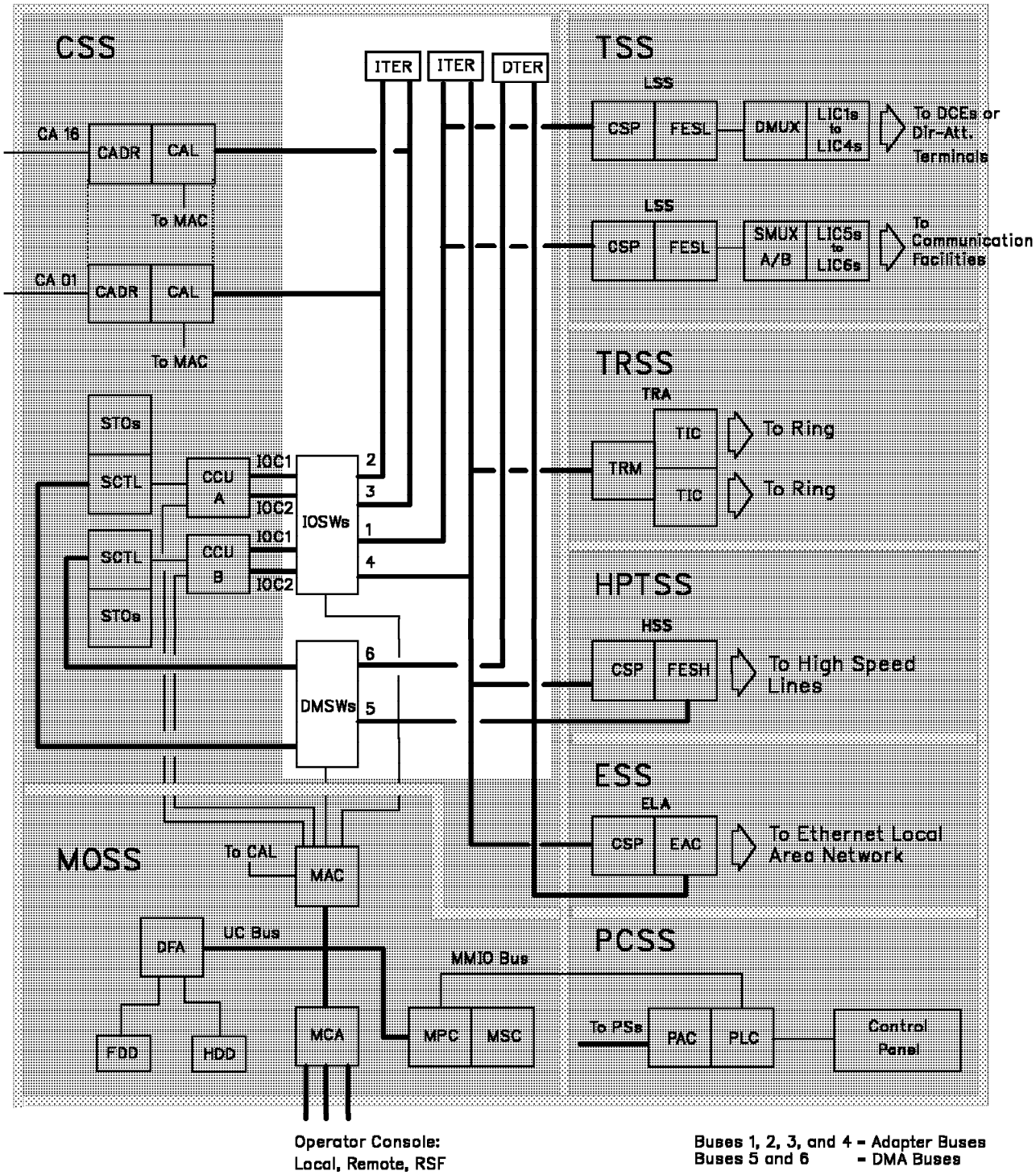


Figure 3-1. The Buses and Bus Switching in 3745 Data Flow. For models 21A-61A, DMA and IOC buses are connected to the CBC in the 3746-900. The MCA card is replaced by the MLA card which interfaces to the MPC card through the MMIO bus. This MLA card links the MOSS to the Service Processor through a LAN.

Generalities

Data, address, and control information exchanges take place between the work registers and adapters attached to the IOC buses through the switching logic.

The IOC logic operates differently depending on whether the program initiates an operation (PIO), or the adapter initiates it (AIO).
In both operations, the A (address) and D (data) registers of the data flow controlled by the IOC logic act as buffers between the CCU(s) and the adapters (CAs and LAs).

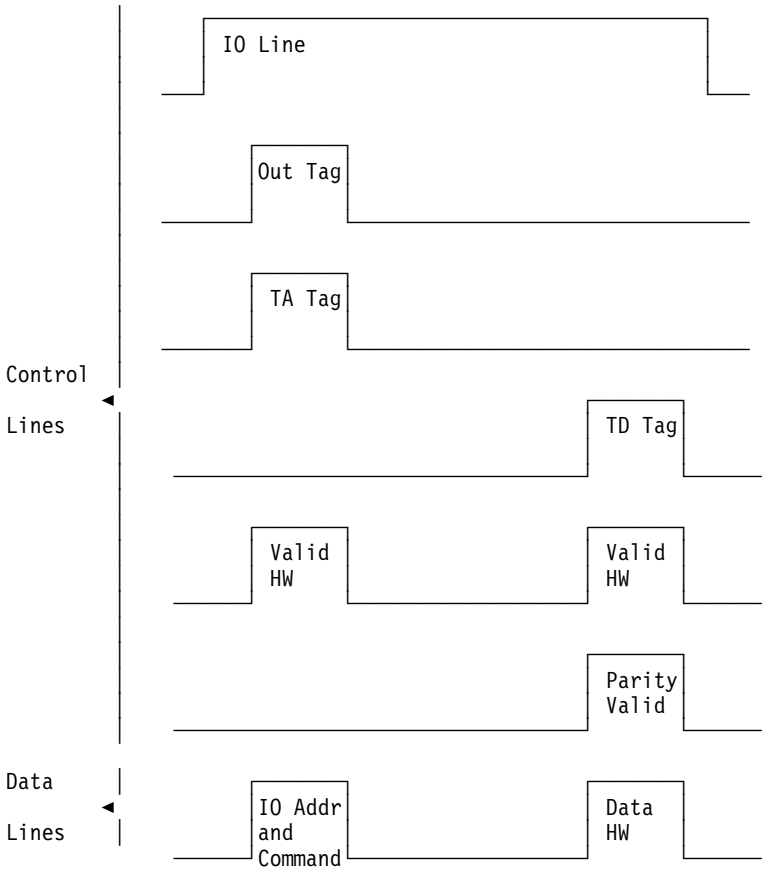
The IOC bus carries interrupt requests from the adapters (level 1, 2, and 3) when not busy with PIO or AIO operations.

This chapter is divided in two parts:

- "Bus Switch" on page 3-5, which gives information on the switching logic, and
- "Buses" on page 3-24, which gives information on the bus logic.

IOC Bus Protocol

Read PIO example



Bus Switch

Introduction

The bus switch, located between the CCU(s) and the adapter buses, allows connecting and switching adapter buses and DMA buses to one of the CCUs.

Four modes of operation are possible:

1. Single mode
2. Twin standby
3. Twin backup
4. Twin dual

Refer to the next pages for details.

The switch functions are split into two independent parts:

- Adapter bus switching to manage data from/to adapters (TSS, HPTSS, ESS, TRSS, and channels).
- DMA bus switching to manage data between HPTSS/ESS and SCTL cards.

The adapter bus switching function constitutes a basic part of the machine, even if the configuration is in single mode. This is due to the fact that it includes electrical signal level adaptation between IOCs and adapters.

The bus switch is controlled from the MOSS through a MAC card. A separate communication path exists between this MAC card and each CCU's bus switch.

Packaging

The bus switch is split into two identical parts, called switch-A and switch-B. Switch-A is associated to CCU-A, switch-B to CCU-B, if a twin machine.

Failure of one of the switches has the same impact as a failure of its associated CCU.

Each switch is composed of:

- one IOSW card
- one DMSW card
- one STER terminator card.

  Note that the two STER terminator cards are present even when only one CCU is installed.

See Figure 3-2 on page 3-6.

Data Flow

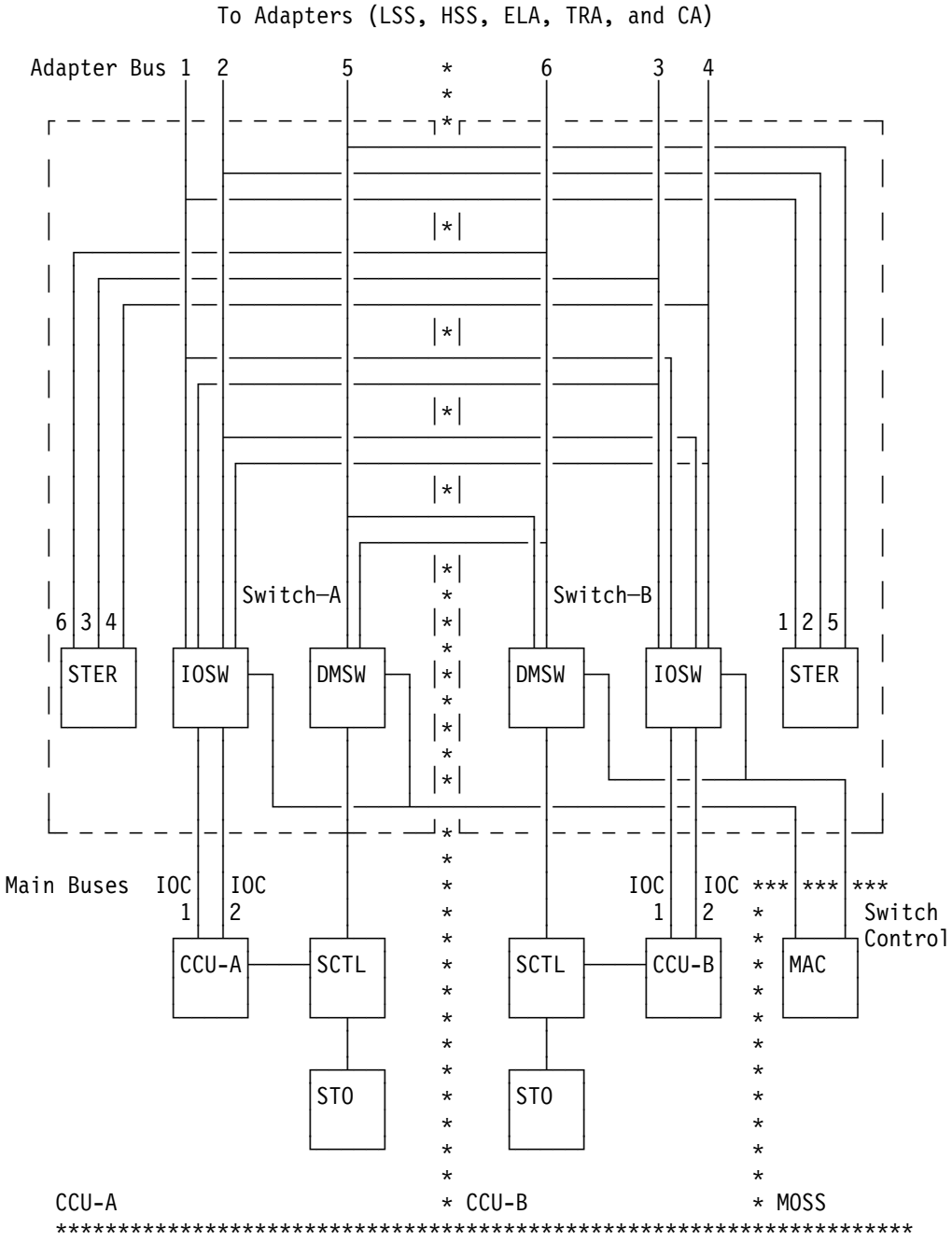


Figure 3-2. Bus Switch Data Flow

Generalities on Switching Operations

Bus switching allows the buses and adapters on the failing CCU to be switched to the running CCU (fallback operation).

Bus Groups

Buses are always switched by groups of three:

- Bus group 1: Adapter buses 1, 2, and DMA bus 5.
- Bus group 2: Adapter buses 3, 4, and DMA bus 6.

This function can only be used on configurations defined as Twin standby, or Twin backup.

Bus switching is also used to switch the buses and adapters back to the original CCU when it is running again (switchback operation).

If a PEP is generated, control must be passed to the EP part of the PEP to move its lines and ESCs, and then control must come back to the NCP.

Port swapping will not carry over from one CCU to another. If any port swapping has been done before the switchover, then MOSS will re-issue automatically the port swap commands.

Switches from NCP to EP (or vice-versa) that are made on a PEP system will not carry over. The access method will have to set the lines to the desired mode.

Adapter and DMA bus switching applies to twin configurations: twin-backup in fallback and twin stand-by. The switching can be automatically or normally activated by MOSS via its switch adapter based on customer-defined configuration options specifying a backup option, and the occurrence of a CCU hardcheck (logic, storage, SCTL/DMA).

Elementary switching commands (per bus) issued from MOSS include:

- Reset all adapters on the bus. This type of reset avoids having to re-IML adapters following a switching operation.
- Disconnect adapter bus from IOC, and companion DMA bus from SCTL.
- Connect adapter bus to IOC and companion DMA bus to SCTL.

MOSS Switching Scenarios

1. Twin Backup

   It is assumed that each CCU runs an NCP sysgened with the backup configuration. In the following examples, it is assumed that CCU-A is the CCU that is failing. The same logic is followed if CCU-B fails.

   a. Automatic fallback in case of CCU hardcheck:

      - Failure of CCU-A is detected via CCU hardcheck or CCU power drop. or some IPL checks (see Chapter 11, “IML and IPL” on page 11-1).
      - In case of hardcheck, re-IPL of CCU-A is attempted to avoid switching for transient errors. If the hardware checkout phase (Phase 1B) is successful, CCU-A is re-IPLed and no switching takes place. According to the option of DUMPLOAD, a dump is taken on disk and re-IPL takes place from disk.

        If unsuccessful, IPL Phase 1A starts, if successful there is no switchover, no new dump is taken, and re-IPL is performed.
      - If the re-IPL Phase 1A is not successful, adapters to be switched are logically reset. Switched CAs are disabled, following the ending status

presented by the channel monitoring, a fallback is performed, the CCU dump is kept on disk.

- Hosts/End-user sessions are de-activated by the hosts in both cases: switching or CCU-A re-IPL.
- Bus switching is activated by MOSS via switch adapter commands. Switched adapters (scanners) are re-initialized/enabled by MOSS.
- MOSS signals the NCP B to update its CDS and the port swaps previously attached to CCU-A.
- MOSS generates an ALERT to notify the network operator that the fallback process is started.
- Sessions are re-activated from the Host.

Note that the process of NCP abend does not lead to a fallback but the following is performed:

- MOSS runs IPL phase 1B, takes a CCU dump on disk according to the option DUMPLOAD, and performs an IPL up to IPL complete.
- If a second abend occurs then, no new CCU dump is taken on disk, IPL is performed up to IPL phase 4, the previous load module is assumed to be defective, a new NCP load module must be loaded from VTAM.

b. Manual Fallback

Manual fallback is allowed via a MOSS command. This is useful to install an MES on one CCU while the other one is running. Manual fallback operations are the same as for automatic fallback but triggering is manual. The switched-from CCU is stopped (CCU STOP function) before activating the switching operations. This also applies to the twin CCU in stand-by mode.

- The customer is responsible for ending active sessions to be switched.
- The switched-from CCU is stopped using the CCU STOP function.
- Switching proceeds as for automatic fallback.

c. Manual Switchback (after CCU-A repair)

- Switched resources are de-activated by the network operator.
- MOSS signals the NCP to update its AIT and to verify that resources to be switched are de-activated.

  If all resources are not deactivated the deactivation can be forced manually.
- Bus switching is activated by MOSS following a positive answer from the NCP.
- MOSS generates an alert to notify the network operator.
- CCU-A is automatically IPLed.
- Resources attached to NCP A are re-activated from the host.

2. Twin Standby

a. Automatic fallback (standby CCU not pre-loaded):
Same as twin backup configuration, except after switching, the switched-to CCU is IPLed.

b. Automatic fallback (standby CCU is pre-loaded):

   - Failure of CCU-A is detected via CCU hardcheck, control program abend or CCU power failure or some IPL checks.
   - Host/end-user sessions are deactivated by the hosts.
   - Bus switching is activated by the MOSS via switch adapter commands. Switched adapters are reinitialized/enabled by the MOSS.
   - The MOSS signals the NCP of CCU-B to update its CDS and port swaps.
   - The MOSS generates an alert to notify the network operator that the fallback is complete.
   - Sessions can be reactivated from the host.
   - The MOSS initiates a re-IPL of the failing CCU. Dumps and other problem determination data are collected.

c. Manual Fallback
   Manual activation of the standby CCU is allowed. This is similar to automatic operations except that triggering is manual. The switched-from CCU is stopped before activating the switching operations.

   - The customer is responsible for ending active sessions to be switched.
   - The switched-from CCU is stopped.
   - Switching proceeds as for automatic fallback.

3. Switchback

   A switchback operation can only be manual.

   Switchback can occur after the adapters of a failing CCU have been switched over and the failing CCU has been fixed.
   The following must be done:

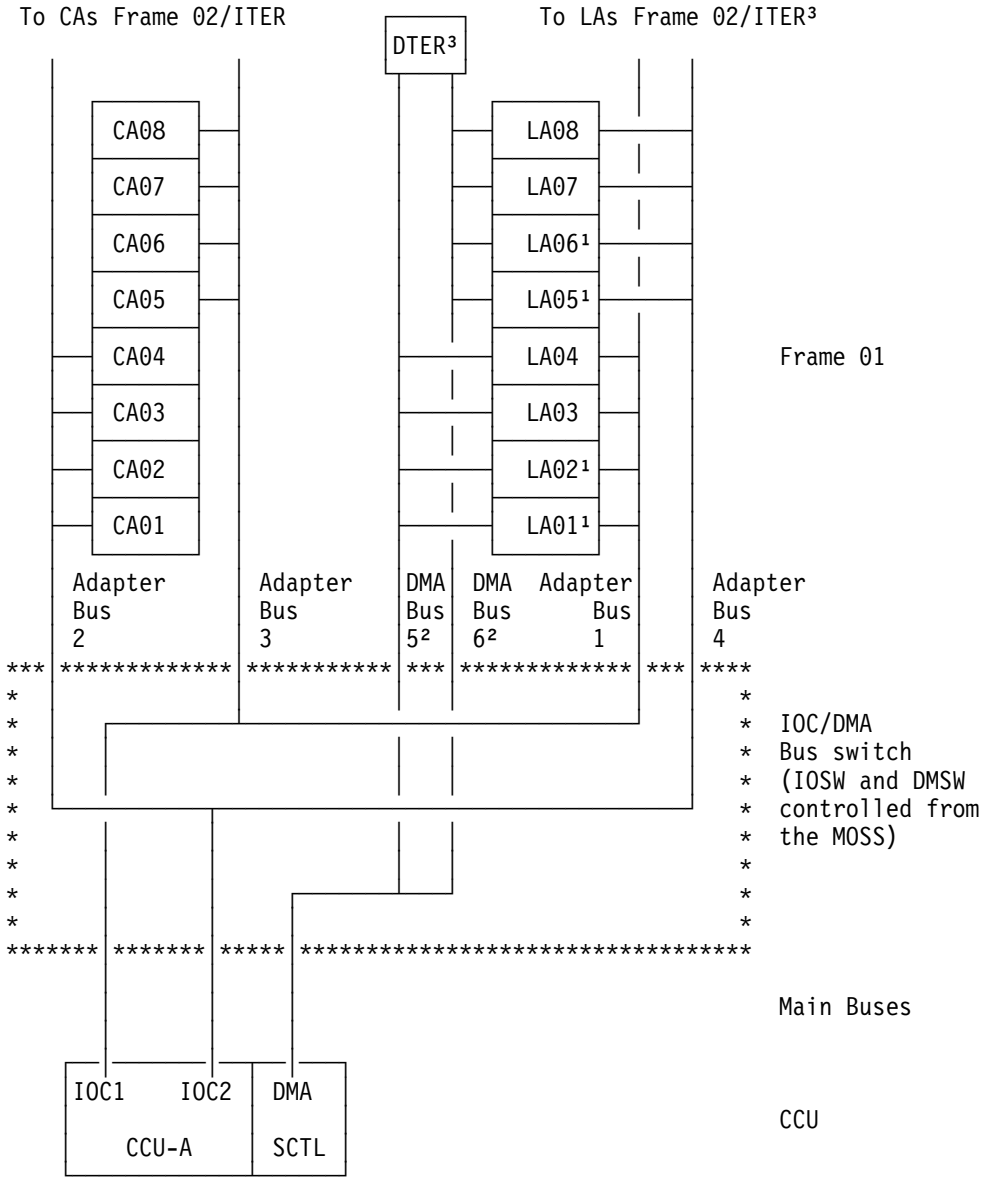
   - All the lines that were originally on the failing CCU must be deactivated by the host.
   - The new MOSS command must be issued.

   Any port swaps that were made while in fallback mode must be initiated by MOSS after the switchover is complete.

   Any switches of PEP lines from NCP to EP or vice versa must be re-established after the switchover.

Machine Mode of Operation

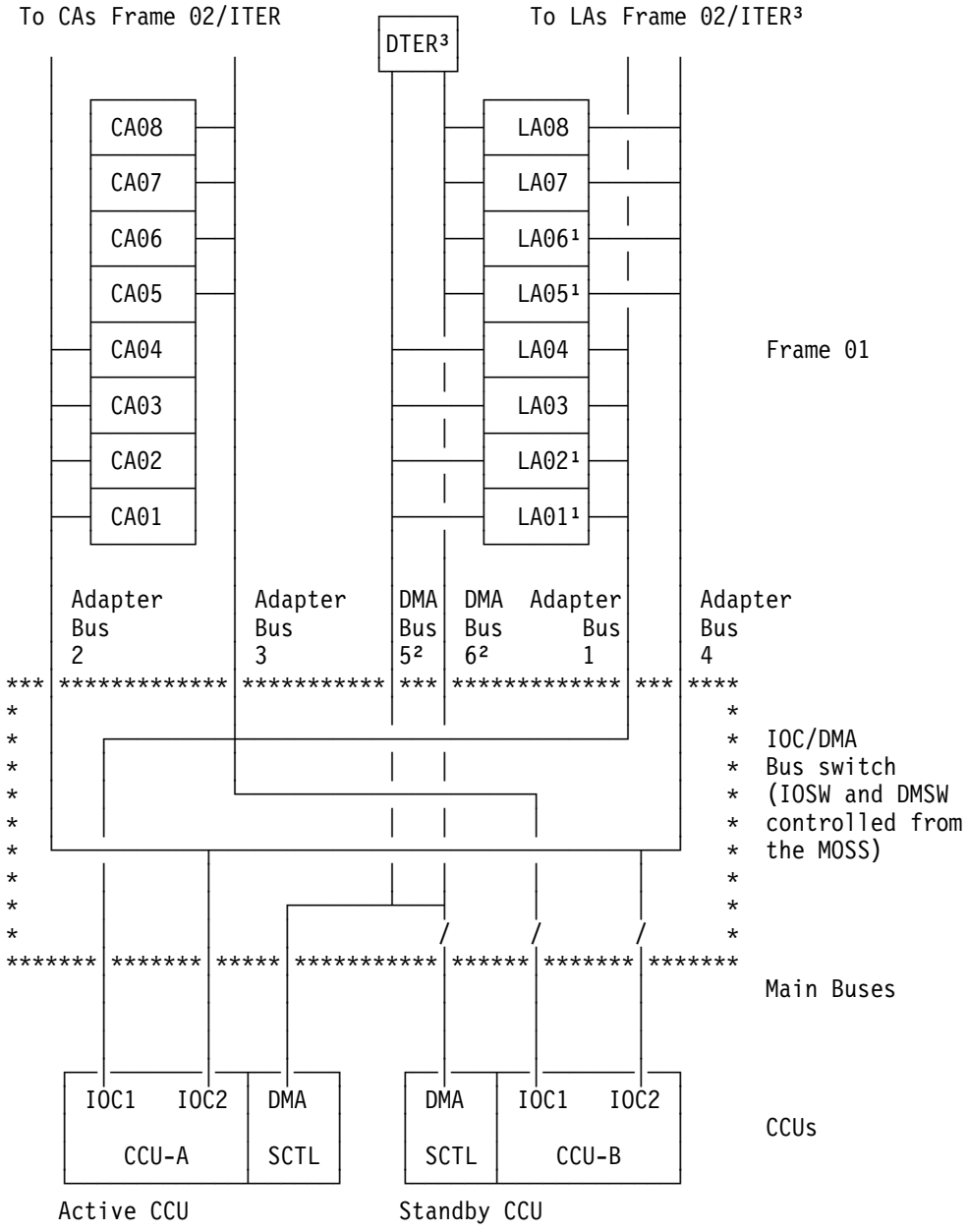
Single: A single CCU is installed. All IOC and DMA buses are connected to this CCU. See Figure 3-3.*:*



1 Can only be TRAs when the TSST board is installed
2 Buses 5 and 6 present for HPTSS/ESS only
3 DMA and adapter buses are connected to the CBC in the 3746-900 (if present) for models 21A-61A.

Figure 3-3. CCU Single Configuration

Twin Standby: Two CCUs are installed. One CCU is active, and the other is in standby, ready to take over if the active CCU fails. See Figure 3-4.
In hot standby mode the standby CCU is already preloaded with a copy of the control program. It is idle but ready to take over the the full configuration in case of a hardware failure of the active CCU. For more details, see the *Advanced Operations Guide*, SA33-0097.

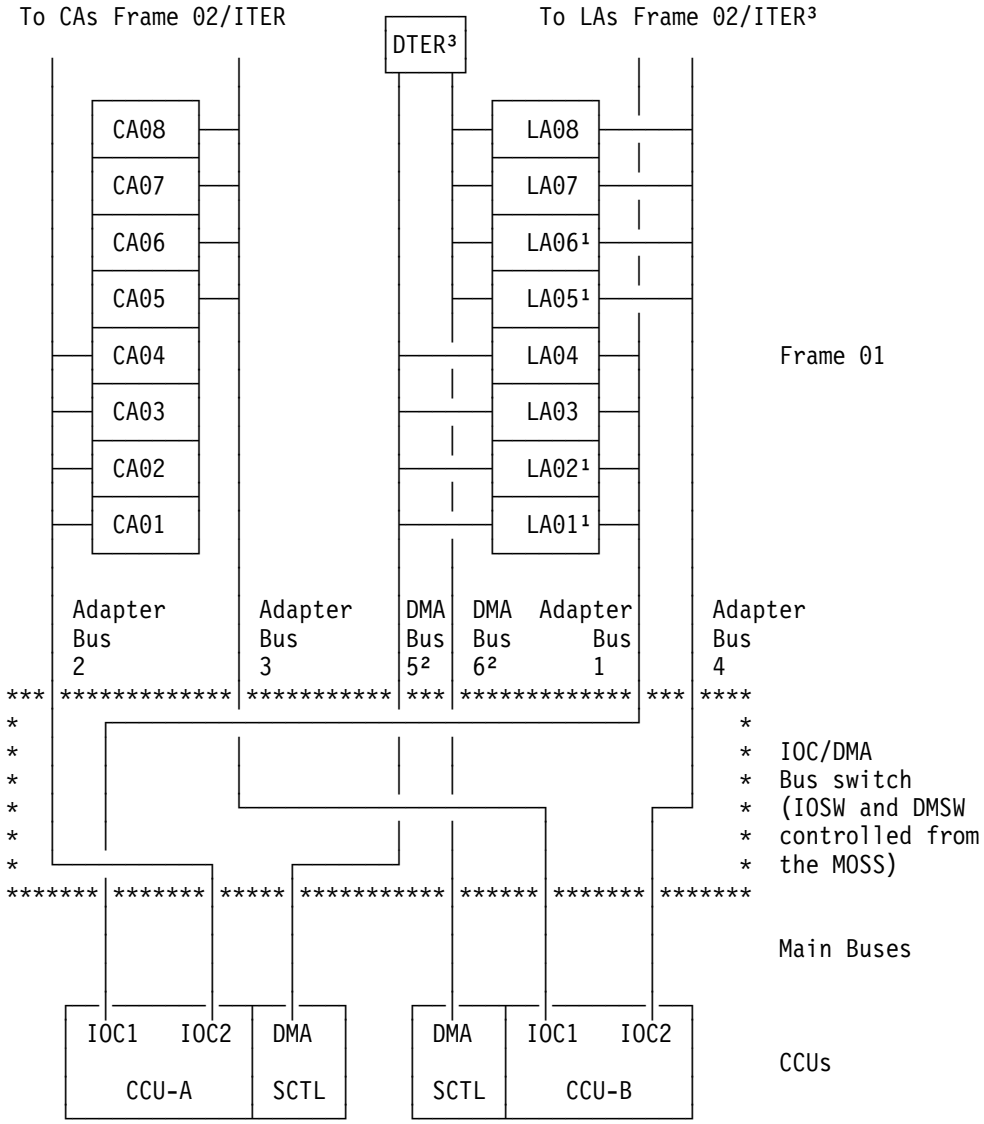


¹ Can only be TRAs when the TSST board is installed
² Buses 5 and 6 present for HPTSS/ESS only
³ DMA and adapter buses are connected to the CBC in the 3746-900 (if present) for models 21A-61A.

Figure 3-4. CCU Twin Standby Configuration

Twin Backup: Two CCUs are operational simultaneously, each controlling part of the network. See Figure 3-5. If one CCU fails, the other CCU takes over all lines controlled by the failing CCU, with a possible reduction of performances depending on NCP generation (fallback configuration). **Adapter buses 1 and 3 will be connected to IOC1 bus, adapter buses 2 and 4 will be connected to IOC2 bus.**

Twin Dual: Two CCUs are operational simultaneously, each controlling part of the network. See Figure 3-5. There is no provision for automatic bus switching (no fallback).***:***



¹ Can only be TRAs when the TSST board is installed
² Buses 5 and 6 present for HPTSS/ESS only
³ DMA and adapter buses are connected to the CBC in the 3746-900 (if present) for models 21A-61A.

Figure 3-5. CCU Twin Backup or Dual Configuration

Configuration

Four adapter buses: 1, 2, 3, and 4 are routed to adapter frames.

Each bus is dedicated to a type of adapter:

- Channel adapters are connected to adapter buses 2 and 3.
- Line adapters are connected to adapter buses 1 and 4.

Two DMA buses: 5 and 6 are routed inside base frame 01.
The HPTSS/ESS are connected to DMA buses 5 and 6, to transfer data directly to storage via the SCTL card, and to two adapter buses 1 and 4 respectively to achieve control operation.

Bus Connection

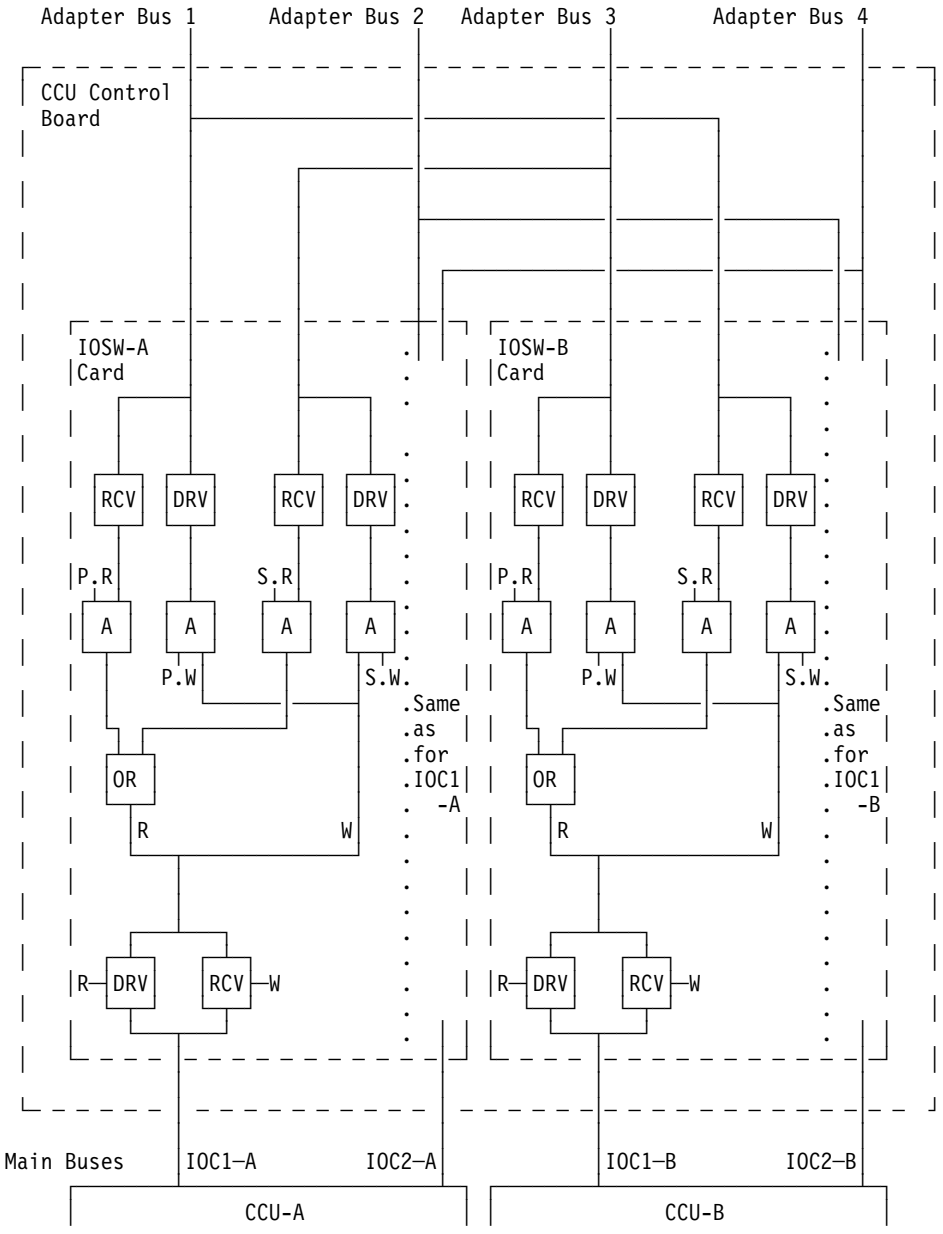
Mode of Operation	Adapter Bus Connection					
	5	6	1	2	3	4
Single	SCTL-A	SCTL-A	IOC1-A	IOC2-A	IOC1-A	IOC2-A
Twin Standby (CCU-A Active)	SCTL-A	SCTL-A	IOC1-A	IOC2-A	IOC1-A	IOC2-A
Twin Standby (CCU-B Active)	SCTL-B	SCTL-B	IOC1-B	IOC2-B	IOC1-B	IOC2-B
Twin Dual or Twin Backup (CCU-A and CCU-B Active)	SCTL-A	SCTL-B	IOC1-A	IOC2-A	IOC1-B	IOC2-B

SCTL-A = SCTL CCU-A
SCTL-B = SCTL CCU-B
IOC1-A = IOC1 CCU-A
IOC2-A = IOC2 CCU-A
IOC1-B = IOC1 CCU-B
IOC2-B = IOC2 CCU-B

Figure 3-6. Bus Connection

Switch Principles

IOC Bus Switch

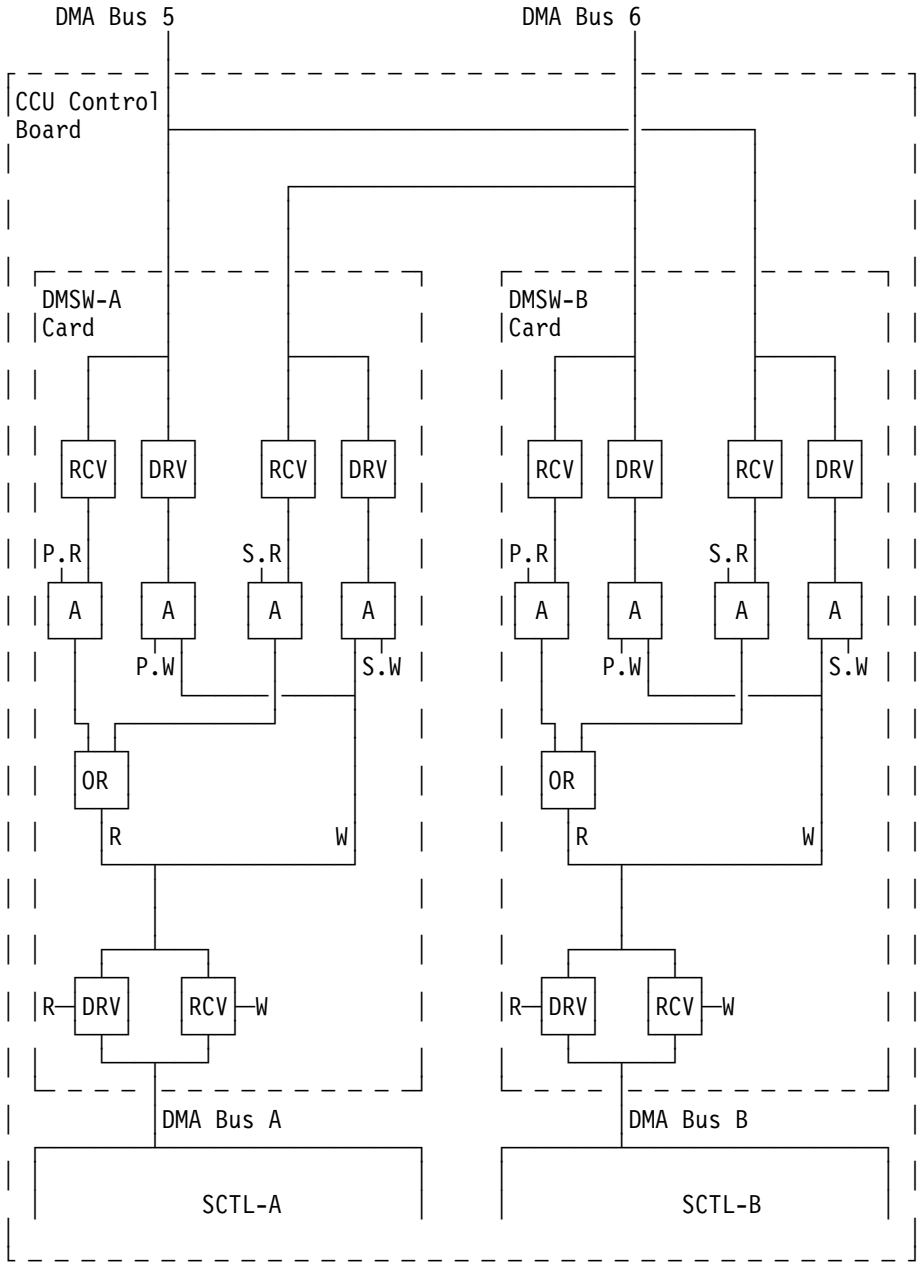


See the next two tables for details on bus connections.

DRV = Driver
RCV = Receiver
P = Connect primary bus
S = Connect Secondary bus
R = Read
W = Write

Figure 3-7. IOC Bus Switch Principles

DMA Bus Switch



See the next two tables for details on bus connections.

DRV	= Driver	S	= Connect Secondary bus
RCV	= Receiver	R	= Read
P	= Connect primary bus	W	= Write

Figure 3-8. DMA Bus Switch Principles

Each switch card has a two-bit configuration register, (bits P and S), called CONFSW and controlled by the MOSS through the MAC card.

According to the mode of operation, the contents of the CONFSW register are:

Mode of Operation	CONFSW A P S	CONFSW B P S
Single	1 1	
Twin Standby (CCU-A Active)	1 1	0 0
Twin Standby (CCU-B Active)	0 0	1 1
Twin Dual or Twin Backup (CCU-A or CCU-B Active)	1 0	1 0

Figure 3-9. Configuration Switch Register

Connected buses

Switch Card	Connected Buses	Twin Dual or Backup	Twin Standby[1] A Active or Single	Twin Standby[1] B Active
IOSW-A (IOC1)	IOC1 Primary	1	1	
	IOC1 Secondary		3	
IOSW-A (IOC2)	IOC2 Primary	2	2	
	IOC2 Secondary		4	
DMSW-A	DMA Primary	5	5	
	DMA Secondary		6	
IOSW-B (IOC1)	IOC1 Primary	3		3
	IOC1 Secondary			1
IOSW-B (IOC2)	IOC2 Primary	4		4
	IOC2 Secondary			2
DMSW-B	DMA Primary	6		6
	DMA Secondary			5

[1] = Can also be a fallback configuration from the twin backup mode.

Switch Control Mechanism

The MAC communicates with the MOSS engine through the MIOC bus. It accepts PIO operations for the following devices (identified at TC time):

- MAC itself
- IOC1 Switch in IOSW-A
- IOC2 Switch in IOSW-A
- DMA Switch in DMSW-A
- IOC1 Switch in IOSW-B
- IOC2 Switch in IOSW-B
- DMA Switch in DMSW-B

PIO operations related to MAC itself are either write PIOs or read PIOs. Among these PIOs, some relate to MAC internal registers which directly feed the Disconnect Switch-A and Disconnect Switch-B lines.

PIO operations related to Switch-A or Switch-B are write PIOs only.

For these operations, MAC transmits to the appropriate control bus the command byte received at TC time, concatenated with the data byte received at TD time (write command). A parity bit is generated for each byte.

This constitutes an 18-bit string shifted on the interconnection 'serial data in' line during the first phase of the transfer (Phase 1).

This phase is started once 'Request Line' has been raised by MAC and the switch device has answered by raising the 'Acknowledge Line'.

At the same time, the selected device returns a Phase 1 status to MAC on the 'Serial Data Out' line.

Phase 1 ends when 'Request Line' is dropped, and 'Acknowledge Line' is also dropped.

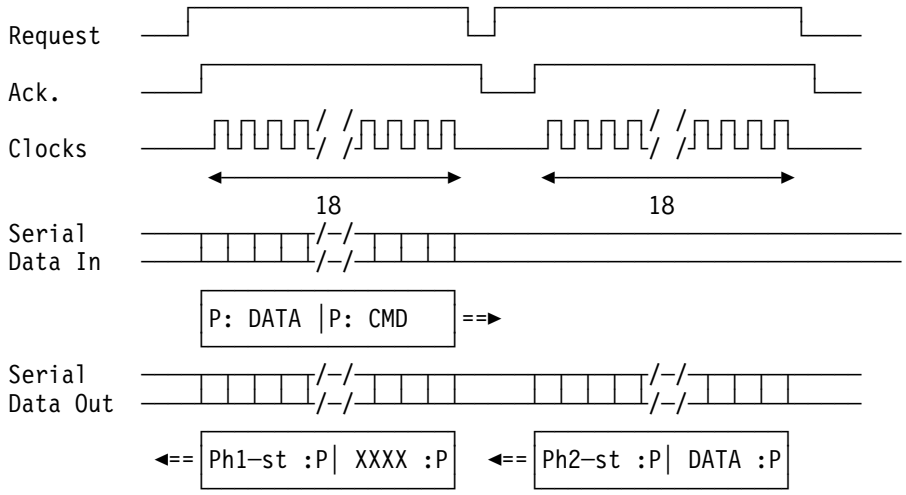
The second part of the transfer (Phase 2) consists in receiving data from the selected switch (read command), together with a Phase 2 status indicating whether the operation has been successfully executed.

This answer from the switch (data and status) constitutes another 18-bit string shifted back to MAC on the interface serial data out line.

Phase 2 uses the same request-acknowledge handshaking mechanism as Phase 1.

If the second phase is not entered within 5 microseconds after acknowledge has been dropped, the switch registers contents are not modified and the switch is ready to enter another Phase 1.

The following timing chart describes the interconnection lines involved in a switch command.

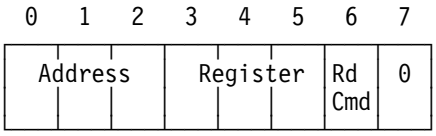


For a given control bus, the serial data in line is wrapped onto the serial data out line, as long as the Request line is inactive.

Switch Command

Command Byte

The command byte, as received by the switch from the MOSS through the MAC card, has the following format:



Device Address (bits 0 to 2)

- 010 : Switch-A IOC1
- 011 : Switch-B IOC1
- 100 : Switch-A IOC2
- 101 : Switch-B IOC2
- 110 : Switch-A DMA
- 111 : Switch-B DMA

Direct Register Address (bits 3 to 5)

- 000 : CONFSW register (read-only)
- 001 : NEWCONF register
- 010 : ACTCONF register
- 011 : BUSCLEAR register

- 100 : SUBCOM register
- 101 : TEMP register
- 110 : RDISC register
- 111 : CDISC register

Read Command (Rd Cd, bit 6)

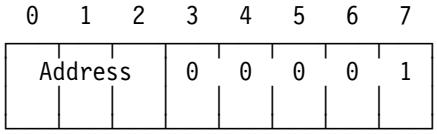
- This bit ON indicates that information is to be read from the switch and presented over the serial data out line during the second phase of the transfer.
- This bit OFF indicates that information provided over the serial data in line (data part of the 18-bit string of the first phase), is to be written into the selected switch register.

Read PIO (bit 7)

- This bit ON indicates a read PIO operation.
- This bit OFF indicates a write PIO operation.
- If a switch receives this bit ON, an invalid command bit will be returned in Phase 2 status, (see below).

Switch Status

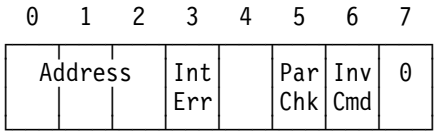
Phase 1 Status:
During Phase 1, the selected switch device has to return the following status:



The device address (bits 0 to 2) corresponds to the selected device.
Addressing is same as for “Command Byte” on page 3-18.

Bit 7 indicates Phase 1.

Phase 2 Status:
During Phase 2, the selected switch device has to return the following status:



The device address (bits 0 to 2) corresponds to the selected device.

Bit 3 (internal error) is set when a wrong behaviour has been detected in the five microsecond time-out counter. Once received by the MAC, this bit raises a Level 0 interrupt to the MPC.

Bit 4 is not used. It can be forced ON by diagnostic commands (Diag2 Register bit 5). Once received by the MAC, this bit raises a Level 0 interrupt to the MPC.

Bit 5 (MAC link parity error) indicates that a parity error has been detected by the switch on the link. Once received by the MAC, this bit raises a Level 0 interrupt to the MPC.

Bit 6 (MAC invalid command) indicates that the contents of the command byte received is incorrect:

- Incorrect device address
- Invalid write command in the CONFSW register
- Read PIO bit ON.

Once received by the MAC, this bit raises a Level O Interrupt to MPC.

Bit 7 OFF indicates Phase 2.
Bit 7 ON during Phase 2 raises a Level O interrupt to the MPC.

MOSS/Switch Interconnection

The MOSS controls each switch through the MAC card by a dedicated interconnection.

Each interconnection is housed in a separate flat cable.

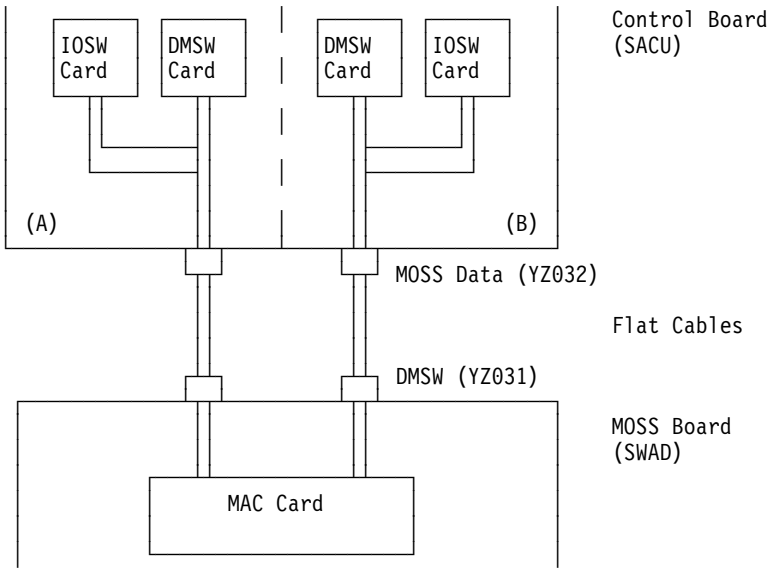


Figure 3-10. MOSS/Switch Interconnection

MOSS/Switch Signal Function

Signal Function	MAC	IOSW	DMSW
IOSW Control Bus			
Serial Data–In IOC	x	.	
Serial Data–Out IOC	.	x	
Shift 1 Clk IOC	x	.	
Shift 2 Clk IOC	x	.	
Request IOC1	x	.	
Request IOC2	x	.	
Acknowledge IOC	.	x	
DMSW Control Bus			
Serial Data–In DMA	x		.
Serial Data–Out DMA	.		x
Shift 1 Clk DMA	x		.
Shift 2 Clk DMA	x		.
Request DMA	x		.
Acknowledge DMA	.		x
Scan Int Bus 1 From Switch	.	x	
Scan Int Bus 4 From Switch	.	x	
Disconnect Switch	x	.	.
MOSS Inop to Switch	x	.	.

Legend:
x : Signal generated
. : Indicates where the signal is used

Figure 3-11. MOSS/Switch Signal Function

- There are two control buses between the MAC card and a given switch:
  - One is dedicated to the IOSW function
  - One is dedicated to the DMSW function

  Each control bus houses the six lines used in the logical protocol between the MAC card and the switch, (Serial Data-In, Serial Data-Out, Shift 1 Clock, Shift 2 Clock, Request, Acknowledge).
  In addition, the IOSW control bus includes two request lines, each dedicated to a given IOC bus.
- Scanner interrupts to MOSS lines are gated from scanner adapter buses 1 and 4 to MOSS.
- The Disconnect switch is activated from MOSS by the MAC card. Special care is taken by the MAC card before activating this line, two coherent MOSS commands must be received, using two different registers.
  The Disconnect switch physically disconnects the switch drivers from the adapters and the scanner interrupt lines from the MOSS.

  This line sets a latch inside switch, so as to keep the memory of the activation of this line in case of MAC link disconnection or MOSS becoming inoperative.

  It allows the MOSS to disconnect a switch even if the normal communication link is not operative, using Request/Acknowledge protocol.

It is error-free at power ON time, at power OFF and at MAC plugging/unplugging.

- MOSS inop line allows isolation of MAC/Switch interconnection and prevents any modification of the switch configuration.
  The polarity of this signal is such that it is active when the cable between MOSS and the switch is disconnected.

Switch CCU-Adapter Interconnection

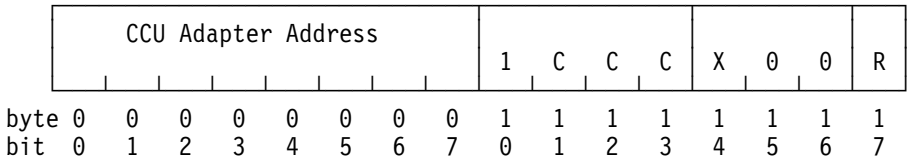
The CCU can access two CCU adapters located in each switch (one per IOC bus) through the following PIOs:

- Read/reset error register
- Read/write data register
- Read/write data register

The CCU adapter has no interrupt capability.

The CCU adapter has no cycle steal capability.

The format is the following:



- The CCU adapter address (byte 0) has to match the contents of the CCU-A ADDR register which is loaded at machine IPL time by the MOSS code.

  According to the machine addressing structure, the following codes are used:

  – Hex '40' for Switch CCU adapter on IOC1
  – Hex 'C0' for Switch CCU adapter on IOC2

- Byte 1 bit 0 = 1
- Byte 1 bits 1-3 (CCC):

  – 000 = Reset/read error register
  – 111 = Write/read data register

- Byte 1 bit 4 (X) can have any value.
- Byte 1 bits 5-6 = 00
- Byte 1 bit 7 (R) indicates a read PIO.

IOC Bus Errors: IOSW error register logs errors detected on IOC and adapter buses. See following error register format.
IOSW does not raise any interrupt when it detects an error.

When the CCU detects an abnormal condition on IOC bus it reads the IOSW error register in order to make a correlation between IOSW detected errors, CCU detected errors, and adapter detected errors.

The detection is made on on each bus, IOC buses 1 and 2, and adapter buses 1, 2, 3, and 4.
When a type of error is detected in IOSW the error register contents is locked.

Error Register Format (SWA error register)

- Byte 0 bits 0-7 : 00
- Byte 1 bit 0 : Inbound parity check (main bus to CCU)
- Byte 1 bit 1 : Outbound parity check (main bus from CCU)
- Byte 1 bit 2 : Inbound parity check (primary bus from adapters)
- Byte 1 bit 3 : Inbound parity check (secondary bus from adapters)
- Byte 1 bit 4 : HALT received during a PIO sent to the CCU adapter
- Byte 1 bit 5 : Invalid CCU adapter command
- Byte 1 bit 6 : Outbound parity check (primary bus to adapters)
- Byte 1 bit 7 : Outbound parity check (secondary bus to adapters)

MOSS can access the CCU adapter resources through commands sent over the MAC link.

POR on Switch

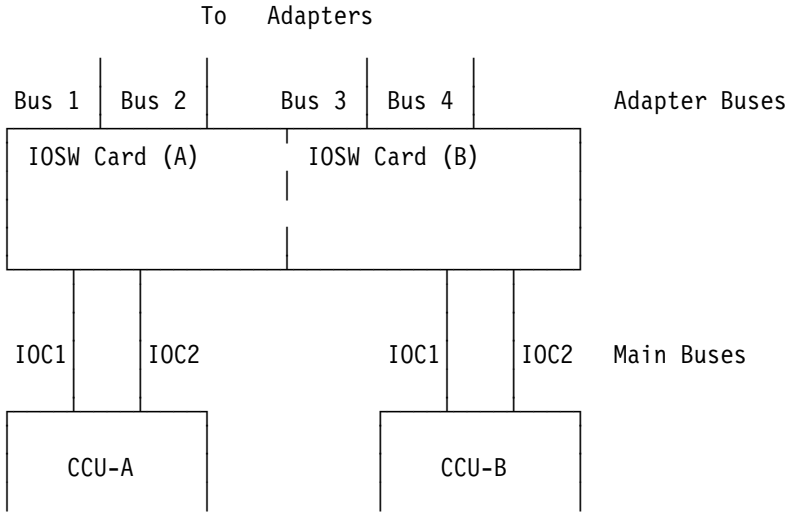
During the POR the CCU/switch adapter and switch error register on the IOSW cards are reset.

Buses

Two types of bus connect the adapters to the CCU/SCTL(s) through the bus switches:

1. IOC buses: These buses connect the CCU(s) to the adapters.
2. DMA Buses: These buses connect the SCTL cards to the high-speed adapters. See “DMA Buses” on page 3-37.

IOC-Buses



Each CCU has two identical IOC main buses, IOC1 and IOC2. IOC1 and IOC2 connect the CCU(s) to the IOSW card(s).

Four adapter buses 1, 2, 3, and 4 are routed from the IOSW card to adapter frames.

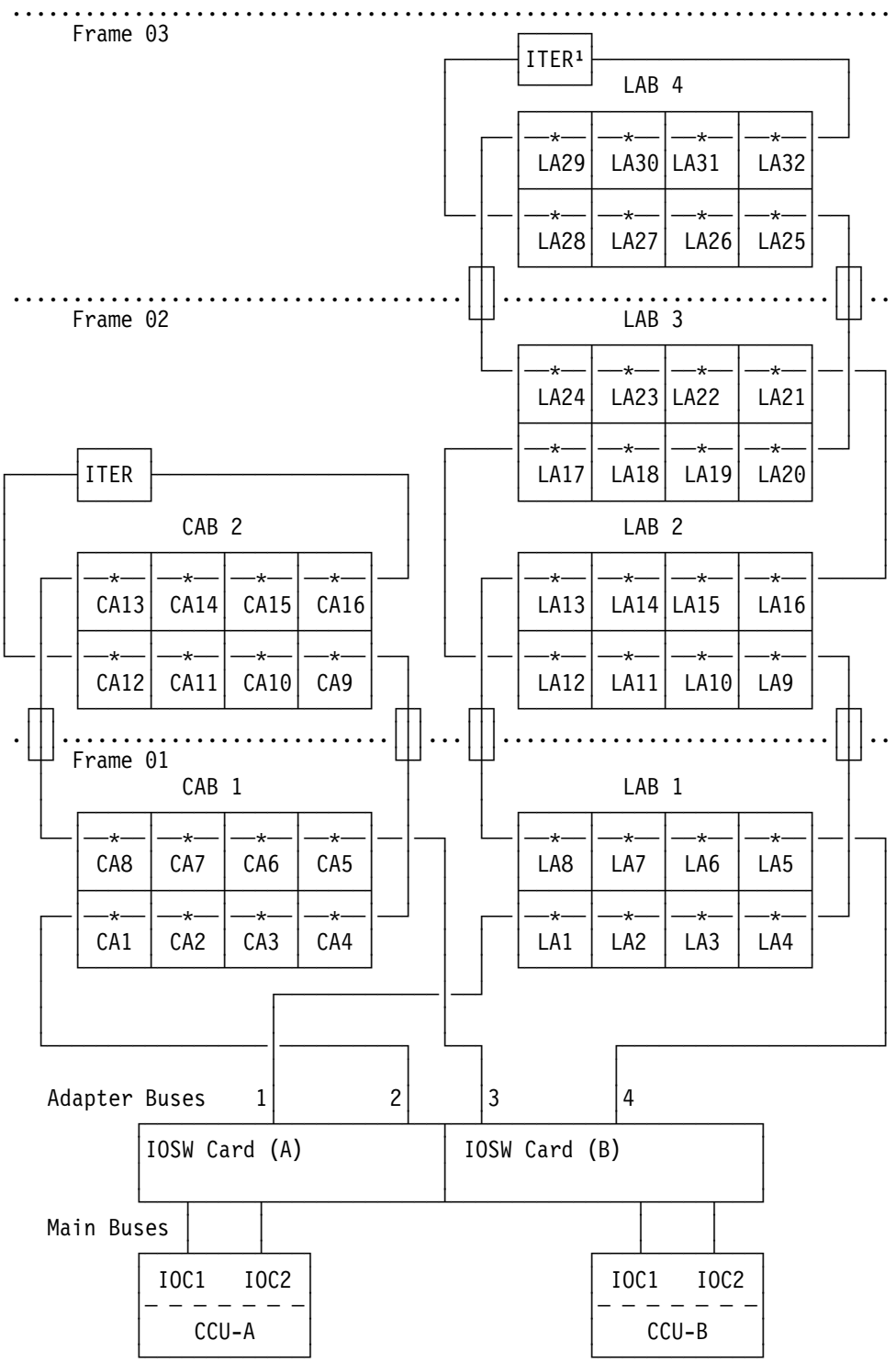
Each adapter bus is dedicated to a specific type of adapter:

- Channel adapters (CA) are connected to adapter buses 2 and 3.
- Line adapters (LA) are connected to adapter buses 1 and 4.

See Figure 3-12 on page 3-25.

See pages YZ032 and YZ033 for bus locations on SACU/L boards.

CCU-Bus Layout



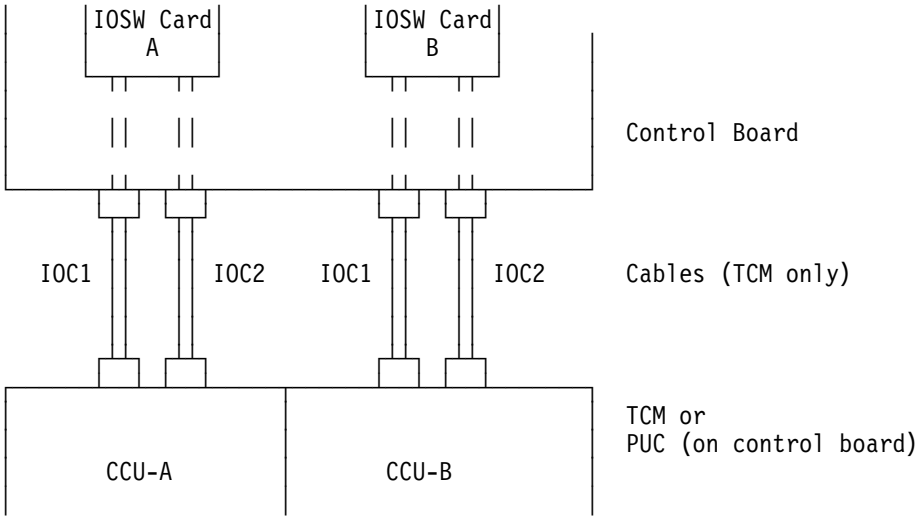
1 Buses are connected to the CBC in the 3746-900 for models 21A-61A.

Figure 3-12. CCU-Bus Layout

CCU-Bus Interconnection

CCU(s) IOSW Card Interconnection

Each interconnection consist of 18 bidirectional lines, (two data bytes plus two parity bits) and 16 tag and control lines.
For details on line function, see Figure 3-13 on page 3-33.



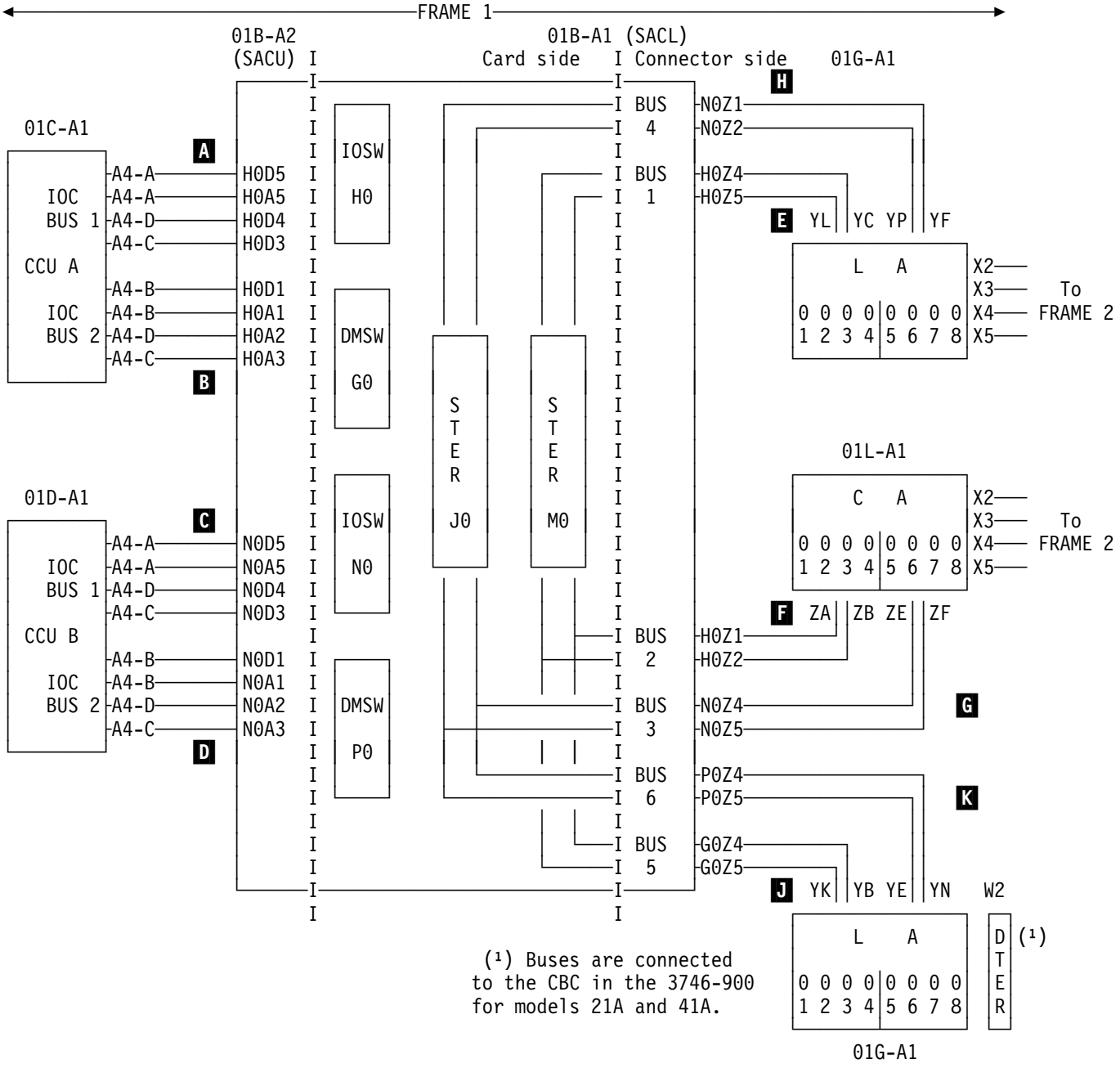
IOSW Card/Adapters Interconnection

For details on line function, see Figure 3-13 on page 3-33.
For 1, 2, 3, and 4 adapter buses interconnection with IOC1 and IOC2 buses, see "Bus Connection" on page 3-13.

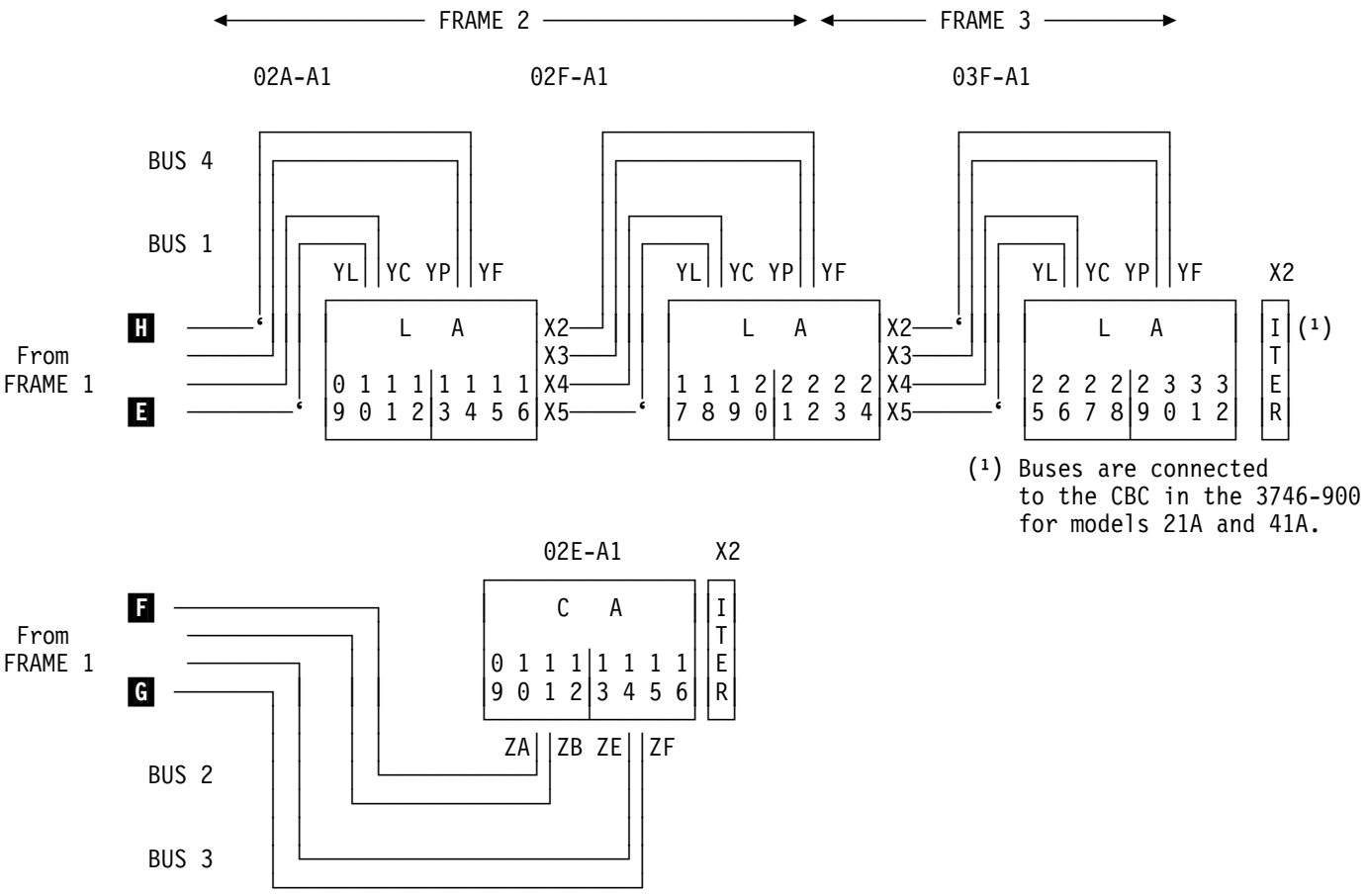
For details on bus layout, see Figure 3-12 on page 3-25.

Bus Data Flow

Models 210, 21A, 410, or 41A (Part 1 of 2)

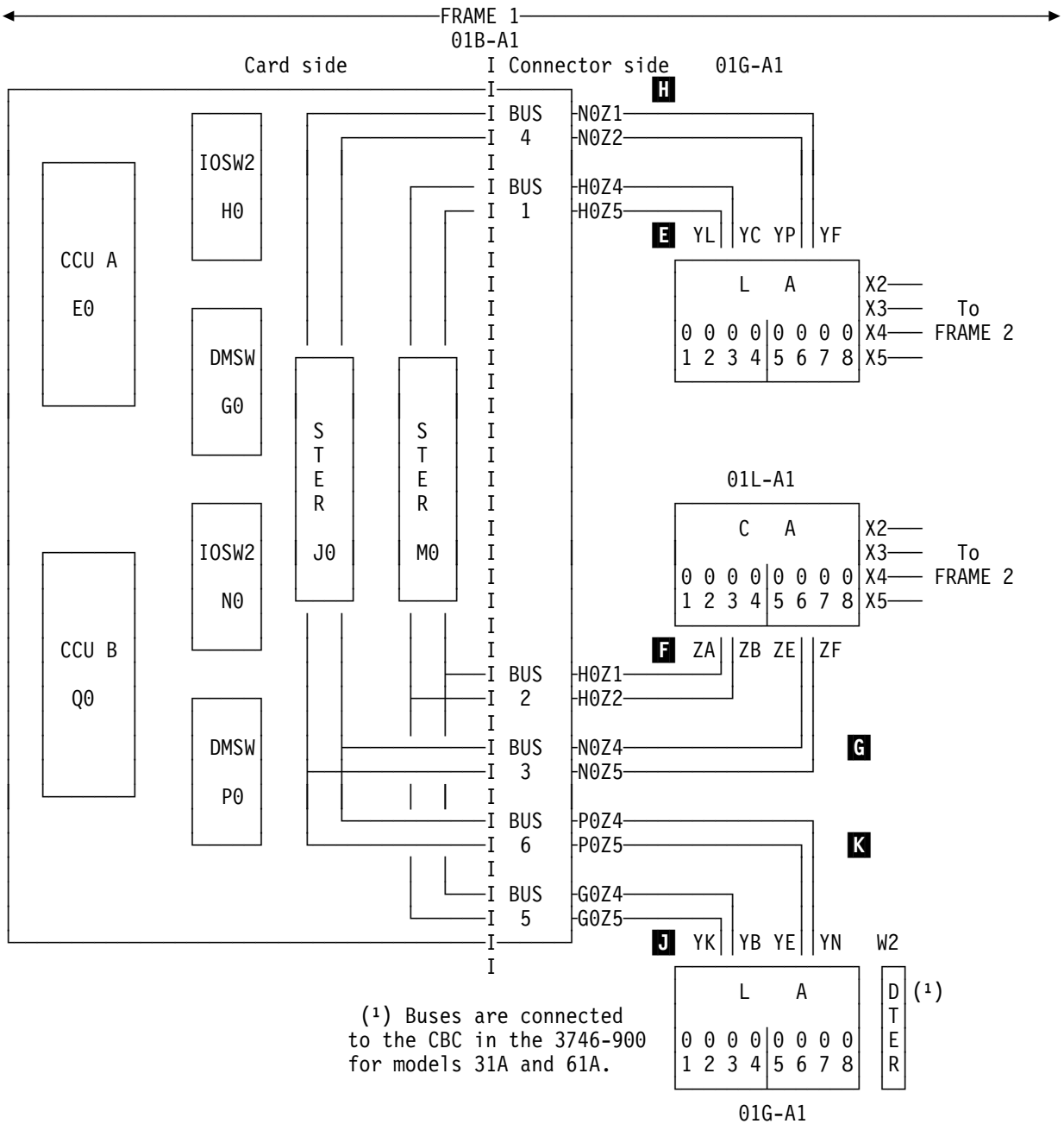


Models 210, 21A, 410, or 41A (Part 2 of 2)

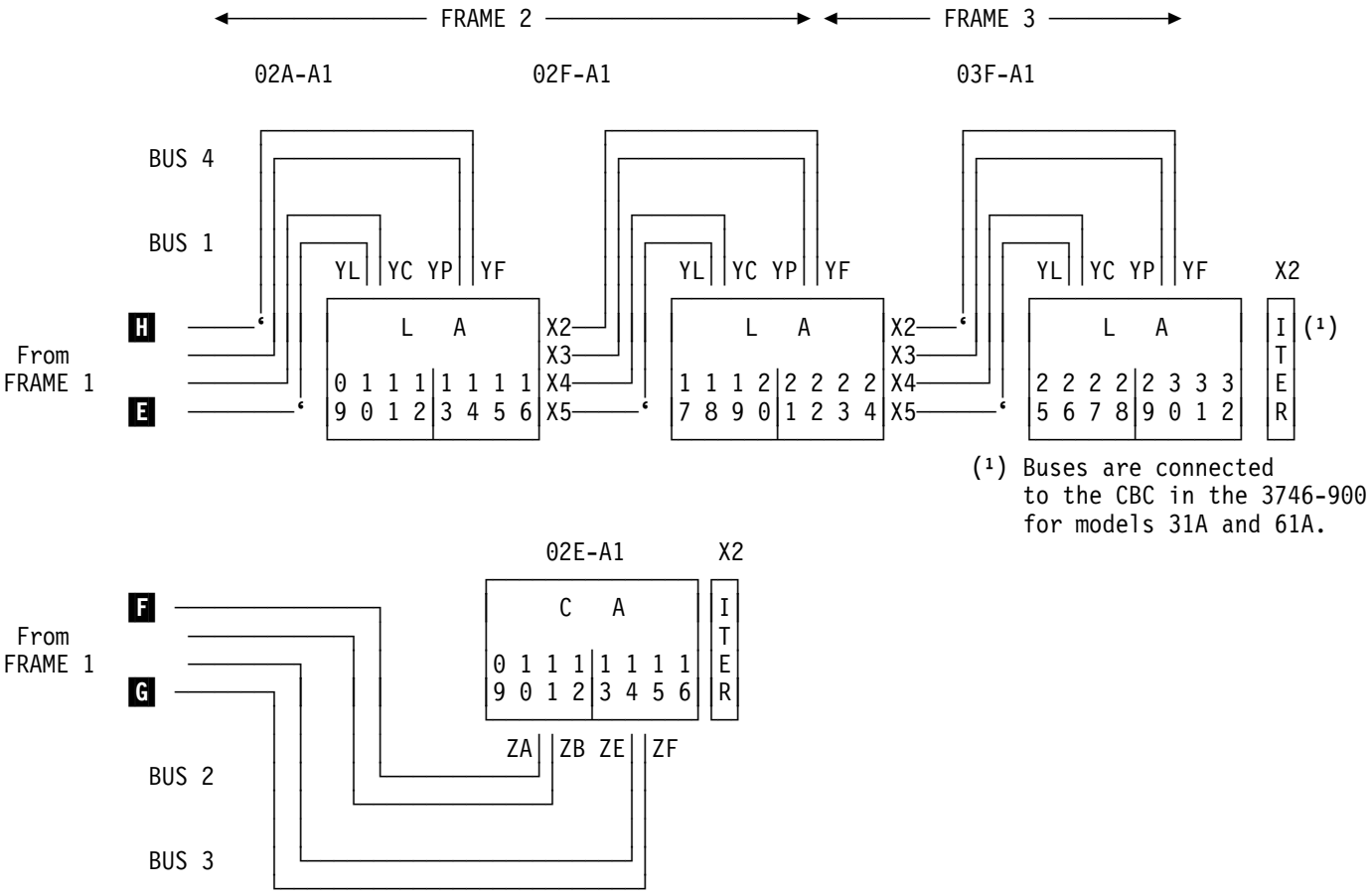


.

Models 310, 31A, 610, or 61A (Part 1 of 2)



Models 310, 31A, 610, or 61A (Part 2 of 2)



IO Cable Group	Name	From To
A (models 210, 21A, 410, or 41A only)	IOC 1 Data	01C-A1A4-A 01B-A2H0D5
	IOC 1 Data	01C-A1A4-A 01B-A2H0A5
	IOC 1 Tag In	01C-A1A4-D 01B-A2H0D4
	IOC 1 Tag Out	01C-A1A4-C 01B-A2H0D3
B (models 210, 21A, 410, or 41A only)	IOC 2 Data	01C-A1A4-B 01B-A2H0D1
	IOC 2 Data	01C-A1A4-B 01B-A2H0A1
	IOC 2 Tag In	01C-A1A4-D 01B-A2H0A2
	IOC 2 Tag Out	01C-A1A4-C 01B-A2H0A3
C (model 410 or 41A only)	IOC 1 Data	01D-A1A4-A 01B-A2N0D5
	IOC 1 Data	01D-A1A4-A 01B-A2N0A5
	IOC 1 Tag In	01D-A1A4-D 01B-A2N0D4
	IOC 1 Tag Out	01D-A1A4-C 01B-A2N0D3
D (model 410 or 41A only)	IOC 2 Data	01D-A1A4-B 01B-A2N0D1
	IOC 2 Data	01D-A1A4-B 01B-A2N0A1
	IOC 2 Tag In	01D-A1A4-D 01B-A2N0A2
	IOC 2 Tag Out	01D-A1A4-C 01B-A2N0A3
E	BUS 1 Tag	01B-A1H0Z4 01G-A1YC
	BUS 1 Data	01B-A1H0Z5 01G-A1YL
		If no LA board in frame 2: ITER 01G-A1X2
		If LA board in frame 2:
	BUS 1 Tag	01G-A1X4 02A-A1YC
	BUS 1 Data	01G-A1X5 02A-A1YL
		If no 2nd LA board in frame 2: ITER 02A-A1X2
		If 2nd LA board in frame 2:
	BUS 1 Tag	02A-A1X4 02F-A1YC
	BUS 1 Data	02A-A1X5 02F-A1YL
		If no frame 3: ITER 02A-A1X2
		If frame 3:
	BUS 1 Tag	02F-A1X4 03F-A1YC
	BUS 1 Data	02F-A1X5 03F-A1YL
		ITER 03F-A1X2
F	BUS 2 Tag	01B-A1H0Z1 01L-A1ZA
	BUS 2 Data	01B-A1H0Z2 01L-A1ZB
		If no CA board in frame 2: ITER 01L-A1X2
		If CA board in frame 2:
	BUS 2 Tag	01L-A1X4 02E-A1ZA
	BUS 2 Data	01L-A1X5 02E-A1ZB
		ITER 02E-A1X2

IO Cable Group	Name	From To
G	BUS 3 Tag	01B-A1N0Z4 01L-A1ZE
	BUS 3 Data	01B-A1N0Z5 01L-A1ZF
		If no CA board in frame 2: ITER 01L-A1X2
		If CA board in frame 2:
	BUS 3 Tag	01L-A1X2 02E-A1ZE
	BUS 3 Data	01L-A1X3 02E-A1ZF
		ITER 02E-A1X2
H	BUS 4 Tag	01B-A1N0Z1 01G-A1YF
	BUS 4 Data	01B-A1N0Z2 01G-A1YP
		If no LA board in frame 2: ITER 01G-A1X2
		If LA board in frame 2:
	BUS 4 Tag	01G-A1X2 02A-A1YF
	BUS 4 Data	01G-A1X3 02A-A1YP
		If no 2nd LA board in frame 2: ITER 02A-A1X2
		If 2nd LA board in frame 2:
	BUS 4 Tag	02A-A1X2 02F-A1YF
	BUS 4 Data	02A-A1X3 02F-A1YP
		If no frame 3: ITER 02A-A1X2
		If frame 3:
	BUS 4 Tag	02F-A1X2 03F-A1YF
	BUS 4 Data	02F-A1X3 03F-A1YP
		ITER 03F-A1X2
J	BUS 5 Tag	01B-A1G0Z4 01G-A1YB
	BUS 5 Data	01B-A1G0Z5 01G-A1YK
		ITER 01G-A1W2
K	BUS 6 Tag	01B-A1P0Z4 01G-A1YN
	BUS 6 Data	01B-A1P0Z5 01G-A1YE
		ITER 01G-A1W2

CCU-Bus Line Function

Line Function	Abbr	CCU	IOSW	CA	LA
Address/Command Tag (1)	TA	x	R	.	.
Data Tag (1)	TD	x	R	.	.
Interrupt Req. Removed (1)	IRR	.	R	x	x
CS Req. High (1)	CSRH	.	R		x
CS Req. Low (1)	CSRL	.	R	x	
CS Grant High (1)	CSGH	x	R		.
CS Grant Low (1)	CSGL	x	R	.	
Input/Output (1)	I/O	x	R	.	.
Halt (1)	HLT	x	R	.	.
Out (1)	R/W	x	R	.	.
Valid Byte (1)	VB	.	R	x	x
Valid Halfword (1)	VH	.	R	x	x
End of Chain (1)	EOC	.	R	x	x
Modifier (1)	M	.	R	x	x
Parity Valid (1)	PV	.	R	x	x
CA IPL Detect (1)	CAIPL	.	R	x	
Reset Tag (See Note 1)	RST		R	.	.
Data Byte 0 (9) OUT	DB0	x	R	.	.
IN	DB0	.	R	x	x
Data Byte 1 (9) OUT	DB1	x	R	.	.
IN	DB1	.	R	x	x
Scan Int (See Note 2)	SCI		R		x

Legend:
(): The contents of the parentheses indicate the number of wires in line function
x : Signal generated
R : Signal redriven. IOSW card is transparent to all these signals. However, in some cases, the I/O tag may be delayed at switching time.
. : Indicates where the signal arrives

Notes:
1. Reset line is activated directly from the MOSS.
2. Sent directly to MOSS (MAC card) from the IOSW card.

Figure 3-13. CCU-Bus Line Function

The following is a short description of each of the lines in the summary table above.

Address/Command Tag (TA): The 'TA' line is activated by the CCU to indicate that the adapter address is in data byte 0 and the command is in data byte 1.

Data Tag (TD): The 'TD' line is activated by the CCU to indicate that the data bus contains write data or that the CCU is ready to receive read data while the 'I/O' line is active.***:*** When the 'I/O' line is not active, the 'TD' line is activated by the CCU to indicate that it is permissible to change the state of any interrupt request on the data bus.

Interrupt Request Removed (IRR): The 'IRR' line is activated by any adapter that has removed its interrupt request from the data bus.
Each adapter should activate 'IRR' in response to the 'I/O' line being activated and, of course, remove its interrupt request from the data bus.***:*** Each adapter should allow 'IRR' to change to the inactive level when the 'I/O' line is inactive.

When all the adapters have allowed 'IRR' to drop, this common 'IRR' line going inactive indicates to the CCU that all adapters have placed their interrupt requests, if any, on the data bus and the CCU may now sample for interrupts.

Cycle Steal Request High (CSRH): A scanner activates 'CSRH' whenever it wishes to start an AIO operation.***:*** The scanner keeps 'CSRH' active until it receives 'CSGH' (Cycle Steal Grant High).

Cycle Steal Request Low (CSRL): A channel adapter activates CSRL whenever it wishes to start an AIO operation.***:*** The channel adapter keeps 'CSRL' active until it receives 'CSGL' (Cycle Steal Grant Low).

Cycle Steal Grant High (CSGH): The CCU activates 'CSGH' in response to 'CSRH' for the purpose of selecting a scanner for an AIO operation, and receiving a 'CSCW' from the selected scanner.
'CSGH' will be deactivated by the CCU when 'valid halfword' is received from the scanner.

Cycle Steal Grant Low (CSGL): The CCU activates 'CSGL' in response to 'CSRL' for the purpose of selecting a channel adapter for an AIO operation, and receiving a 'CSCW' from the selected channel adapter.
'CSGL' will be deactivated by the CCU when 'valid halfword' is received from the channel adapter.

Input/Output (I/O): The 'I/O' line is activated by the CCU to indicate either that an I/O operation is about to start on the IOC bus, or that one is in progress.***:*** For any I/O operation, 'I/O' is the first line activated and the last one deactivated.

When the 'I/O' line is active, all adapters should remove any interrupt requests on the data bus until the I/O is deactivated.

Halt (HLT): The CCU activates the 'halt' line to indicate to the selected adapter that the CCU has detected an error condition associated with the current operation. The CCU will activate the 'halt' line after 'TA', 'CSGH', or 'CSGL' has been deactivated. The CCU will deactivate the 'halt' line when it deactivates the 'I/O' line. The selected adapter will terminate the current operation and set a check bit active in its status register.

Out (R/W): The CCU activates the 'out' line, while the 'I/O' line is active, to indicate that the direction of information on the data bus is outbound from the CCU. The CCU deactivates the 'Out' line to indicate that the direction of information on the data bus is inbound to the CCU.

Valid Byte (VB): A selected adapter will activate the 'valid byte' line during an AIO operation to indicate a byte transfer instead of a halfword transfer. The valid byte of information will be data bus byte 1.

Valid Halfword (VH): In some places the term 'valid' is used in place of 'valid halfword'. A selected adapter will activate the 'valid halfword' line in response to the activation of the 'TA', 'TD', 'CSGH', or 'CSGL' line from the CCU.
'Valid halfword' line active indicates that the adapter has either placed information on the data bus or has received information from the data bus. It also indicates that the CCU may deactivate its control line.

All adapters will activate 'valid halfword' when the CCU deactivates the 'I/O' line, and deactivate 'valid halfword' when the CCU activates the 'I/O' line.

The CCU will proceed with an IO operation after all adapters have deactivated 'valid halfword'. A selected adapter will activate the 'end of chain' line instead of 'valid halfword' for the last halfword transfer of an AIO operation.

End of Chain (EOC) 'End of chain' active indicates that the AIO operation should be concluded and that the adapter has either placed information on the data bus or has received information from the data bus.

Modifier (M): A selected adapter will activate the 'modifier' line with 'valid byte' line for the last byte transfer of a AIO operation.***:*** 'Modifier' line active at this time indicates that the AIO operation should be concluded.

Parity Valid (PV): A selected adapter will activate 'parity valid' to indicate to the CCU that it wishes to have parity checking of data inbound to the CCU.***:*** If 'parity valid' is active and bad parity is detected by the CCU, the CCU will activate the 'halt' line.

If 'parity valid' is deactivated and bad parity is detected by the CCU, the parity is corrected, the data is stored, and a status bit is set.

CA IPL Detect (CAIPL): A CA adapter will activate this line when it detects a "WRITE IPL" command on the host interface. When the CCU receives this signal it will raise a Level 1 interrupt to MOSS.

Reset (RST): The MOSS may activate the 'reset' line at any time to initialize all adapters. This initialization will cause all adapters to immediately terminate current operations, go to a ready state, and prepare to respond to PIO commands.

Data bus bytes 0 and 1: The data bus is halfword wide with 18 bidirectional lines. Each of the two bytes (0 and 1) contains 8 bits plus a parity bit (0-7,P).***:*** Information is transferred between the CCU and the adapters in either direction when the 'I/O' line is active.

Four bits of the bus are used for an additional function when the 'I/O' line is deactivated, as follows:

- Byte 0 bit 1 = LAs Lvl 2 interrupt req to CCU.
- Byte 0 bit 5 = CAs Lvl 1 interrupt req to CCU.
- Byte 1 bit 0 = CAs Lvl 3 interrupt req to CCU.
- Byte 1 bit 5 = LAs Lvl 1 interrupt req to CCU.

The adapters activate their interrupt requests to the CCU using these paths, but only when the 'I/O' line is inactive.
The CCU will sample the data bus for interrupts after activating the 'TD' line, while the 'I/O' line is inactive.

Scanner Interrupt (Scan Int): Interrupt level 4 generated by the line adapter to the MOSS (MPC).

Physical Interconnection

The physical interconnection is made by flat cables between boards, and board wiring.

See Figure 3-12 on page 3-25

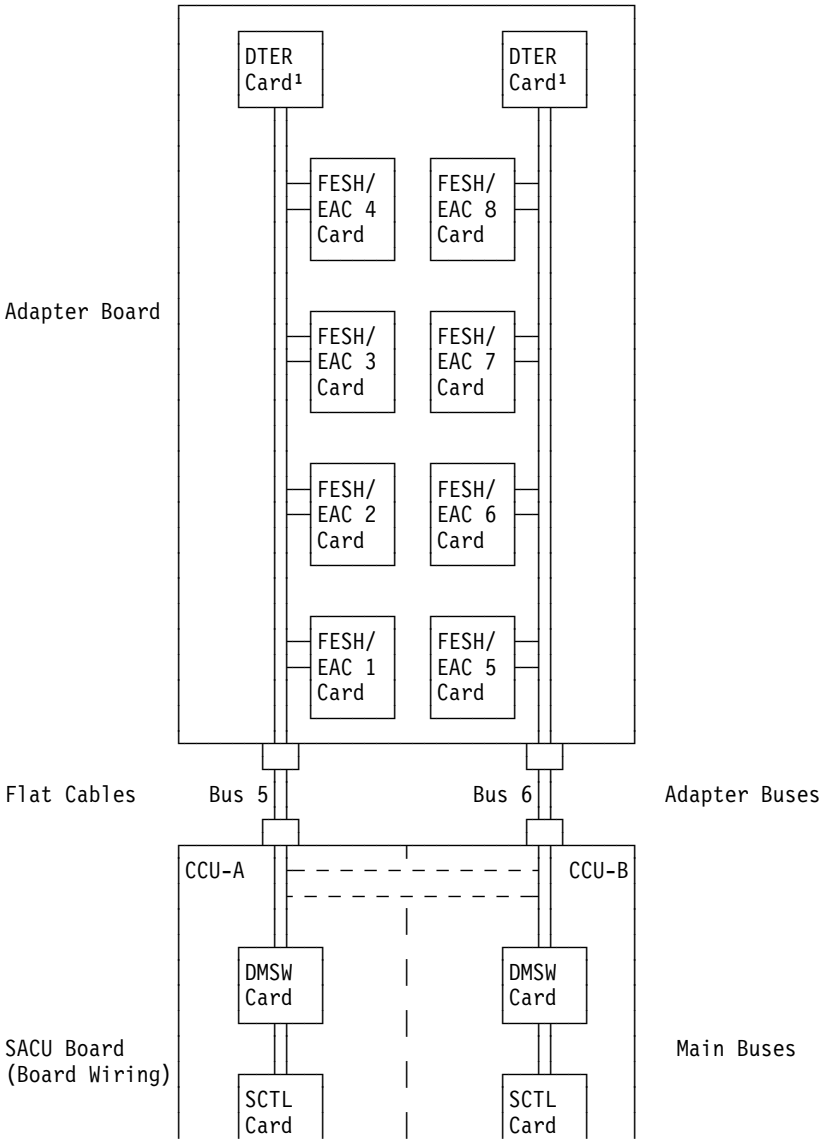
DMA Buses

These buses are used to transfer data from CCU storage to the high speed adapters (FESH card) and Ethernet LAN adapter (EAC card).

Two identical DMA buses, 5 and 6, are routed from the DMSW card to the FESH/EAC cards located in the first adapter board of the base frame 01.

See Figure 3-14 for details.

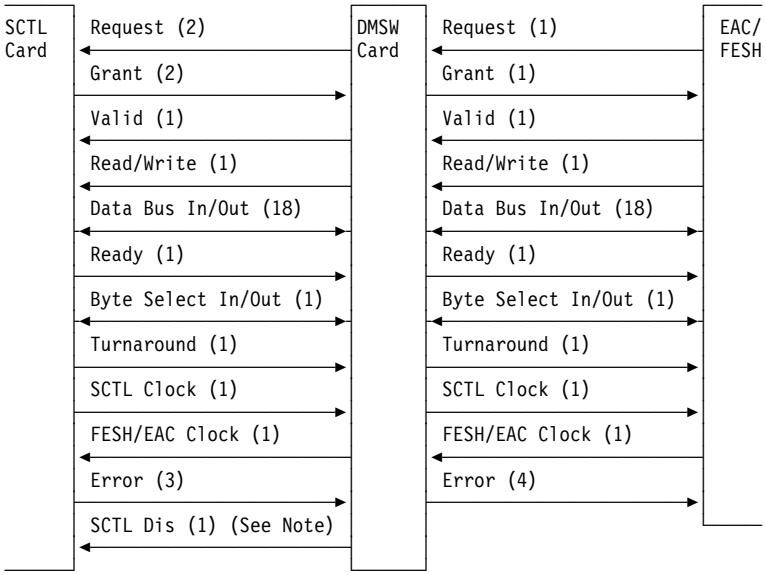
Physical Interconnection



¹ Buses are connected to the CBC in the 3746-900 for models 21A-61A.

Figure 3-14. DMA Bus Physical Interconnection

Interconnection Layout



(): The figure in the parentheses indicates the number of wires in the line function
Note: SCTL Disable line is activated from the MOSS and is used at switching time.

Figure 3-15. DMA Bus Interconnection Layout

DMA-to-SCTL Bus Line Function

Line Function	SCTL	DMSW
Request (2) (See Note 1)	.	x
Grant (2) (See Note 1)	x	.
Valid (1)	.	x
Read/Write (1)	.	x
Data Bus (18) Out	x	.
In	.	x
Ready (1)	x	.
Byte Select (1) Out	x	.
In	.	x
Turnaround (1)	x	.
SCTL Clock (1)	x	.
FESH/EAC Clock (1)	.	x
Error (3)	x	.
SCTL Dis (1) (See Note 2)	.	x

Legend:
(): Figure in the parentheses indicates the number of wires in the line function
x : Signal from
Note:
1. One Request line for each bus, 5 and 6. One Grant line for each bus, 5 and 6.
2. SCTL Disable line is activated from the MOSS and is used at switching time.

Figure 3-16. DMA Bus Line Function

DMA-to-FESH/EAC Bus Line Function

Line Function	DMSW	EAC/ FESH
Request (1)	.	x
Grant (1)	x	.
Valid (1)	.	x
Read/Write (1)	.	x
Data Bus (18) Out	x	.
In	.	x
Ready (1)	x	.
Byte Select (1) Out	x	.
In	.	x
Turnaround (1)	x	.
SCTL Clock (1)	x	.
FESH/EAC Clock (1)	.	x
Error (4)	x	.

Legend:
(): The figure in parentheses indicates the number of wires in the line function.
the number of wires in the line function.
x : Signal from
. : Indicates where the signal arrives

Figure 3-17. DMA Bus Line Function

The following is a short description of each of the lines in the preceding summary tables.

Request: Each request indicates that a FESH/EAC requests a DMA service (such as a Write or Read data transfer). Write means that storage will be written. Read means that storage data will be sent to the adapter.***:*** The two requests correspond to the two DMA buses connected to a DMSW card (one request per DMA bus).

Grant: Each grant indicates an answer to a request.
The two grant signals correspond to the two DMA buses connected to a DMSW card (one grant per DMA bus).

Valid: Indicates that the grant has been taken into account by the adapter and that the DMA data transfer can start.

Read/Write: Indicates the direction of the DMA data transfer.

Data bus: 18 bidirectional lines. Used to transfer the CCU address and burst length from the selected adapter, and to support the data transfers.

Ready: It is an envelope of the actual data transfer, (if the ready bit is ON there is a data transfer).

Byte Select: One bidirectional line. Indicates that only one byte is transferred in the last halfword data transfer.

Turnaround: Indicates a read data transfer.

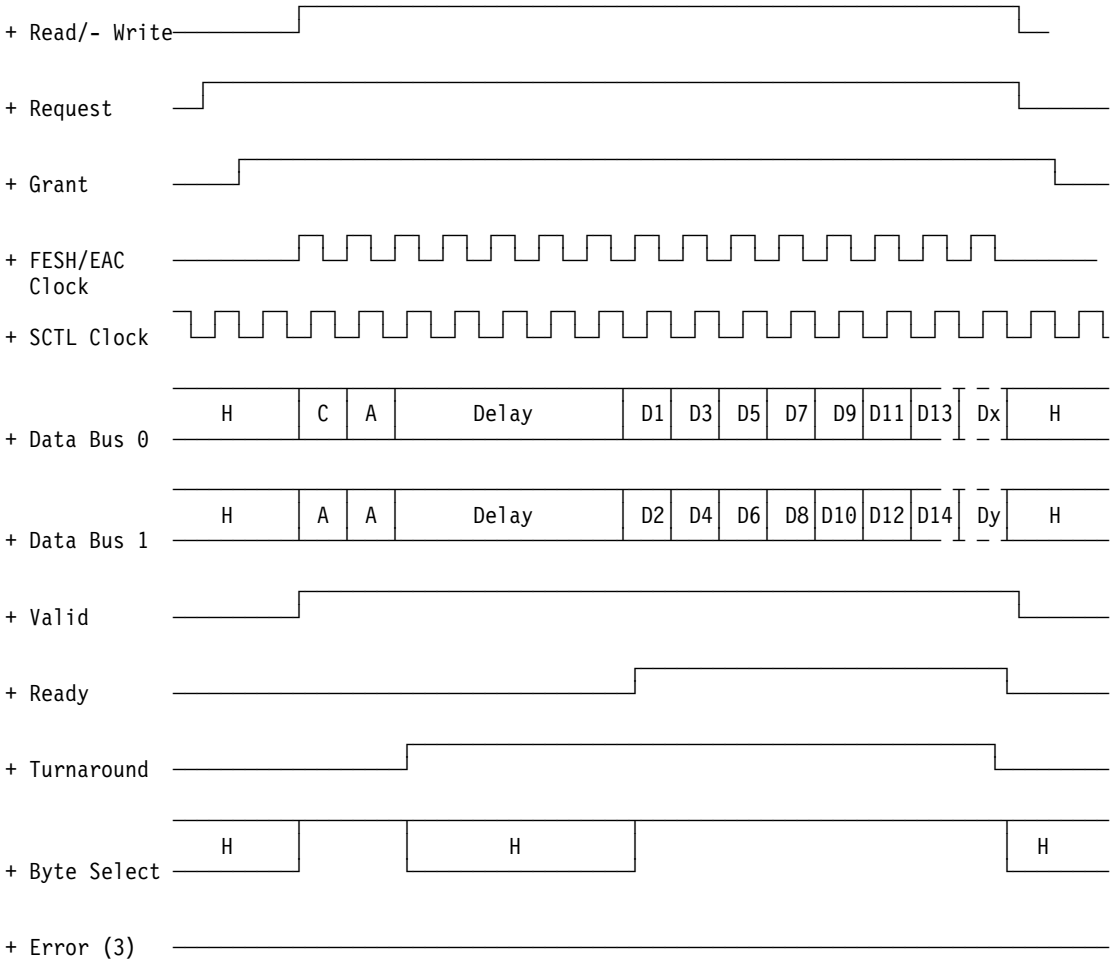
SCTL Clock: Synchronizes the DMA bus operations.

FESH/EAC Clock: It consists in the SCTL clock gated by the valid tag in the FESH/EAC.

Errors: Used to report errors to the adapter. When the DMSW card detects an error, it can modify the errors lines to the adapters.***:*** See Chapter 6, “High Performance Transmission Subsystem (HPTSS)” on page 6-1 for details.

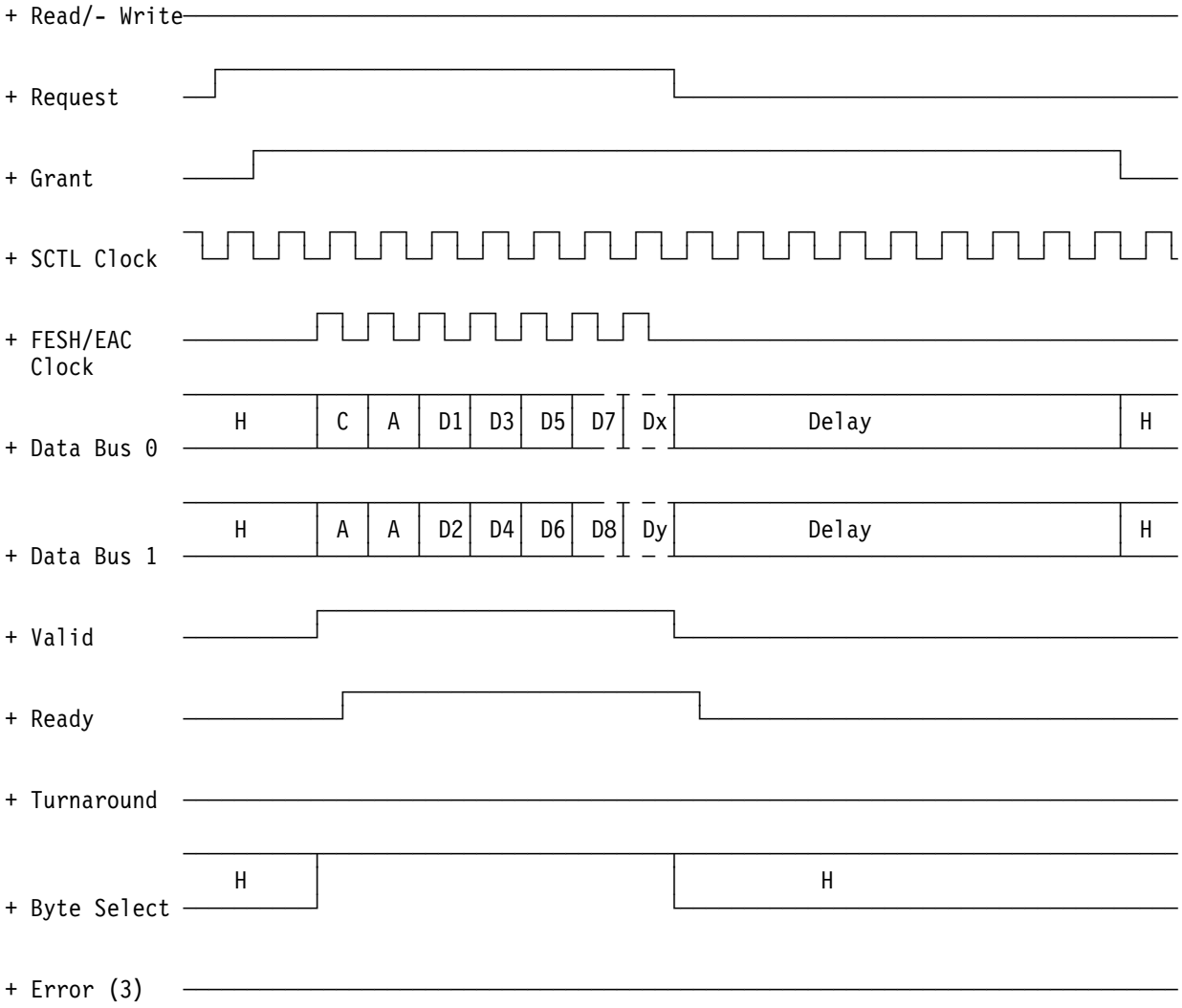
SCTL Disable: Informs SCTL that a switch configuration change will occur. SCTL must terminate the current burst transfer, but not grant another request.***:***

DMA Bus During Read Operation:



A = Address
C = Count
D = Data
H = High-impedance driver 3 states
Delay = Delay to transfer data from storage

DMA Bus During Write Operation:



A = Address
C = Count
D = Data
H = High-impedance driver 3 states
Delay = Delay to transfer data to storage

PIO Operation

PIO Operation Sequence

A PIO operation to control a channel or an LA operation may be started either by the control program in the CCU, or by the microcode in the MOSS.

PIO Initiated by the CCU

During such an operation two halfwords (address, command, and data) are exchanged with a selected adapter.

A PIO operation has four steps:

1. IOH or IOHI instruction decode
2. IOC initialization
3. Adapter addressing and selection
4. Data transfer:

   Write = from CCU
   Read = to CCU

At step 1:

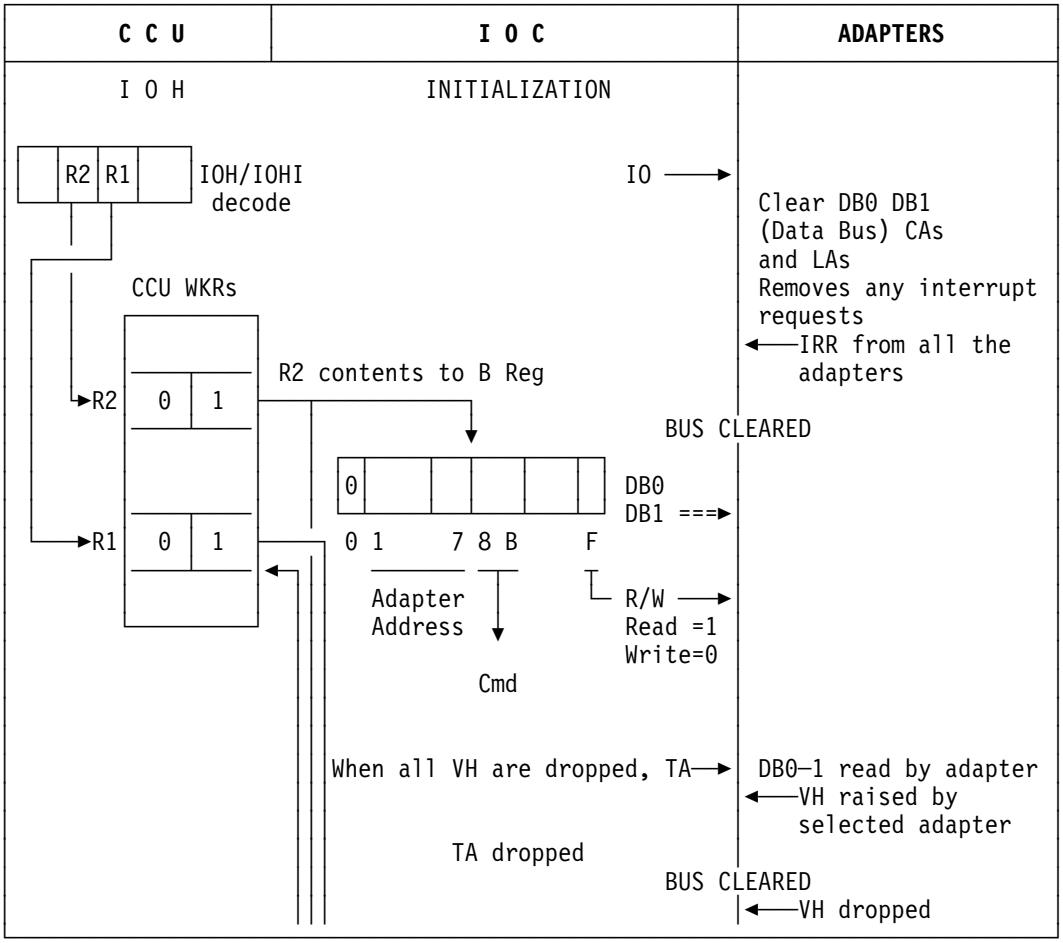
- Instruction code 50 = IOH with R1 and R2.
- Instruction code 70 = IOHI with R1 and the second halfword of the instruction whose contents go into the D register.

PIO Initiated by the MOSS

MIOH/MIOHI instructions are equivalent to IOH/IOHI instructions except that:

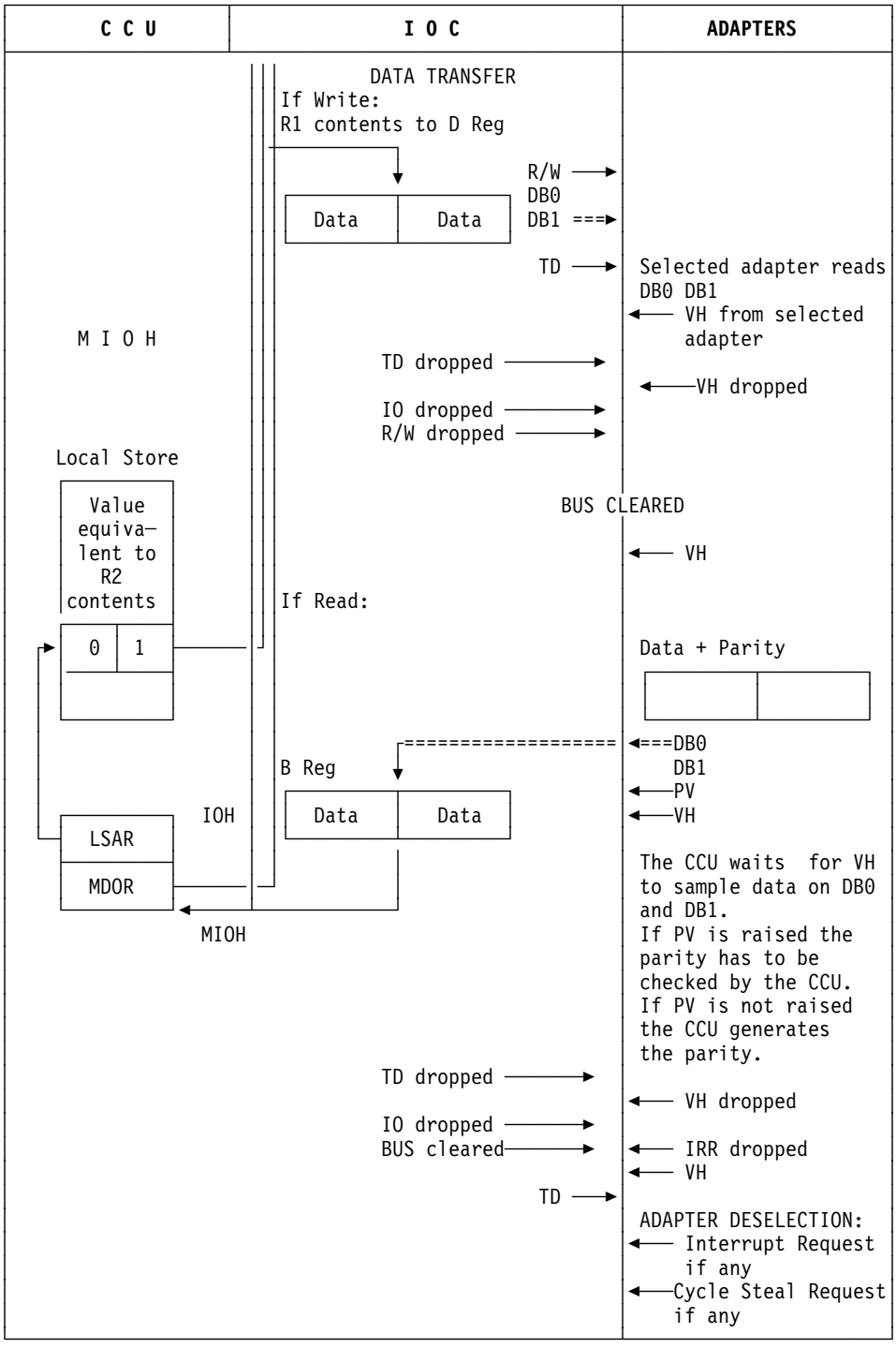
1. The MOSS initiates the operation.
2. R2 contents are found at the LS address given by the LSAR at TA time.
3. The MDOR receives or sends at data TD time instead of R1.

PIO Operation Sequence (Initialization)

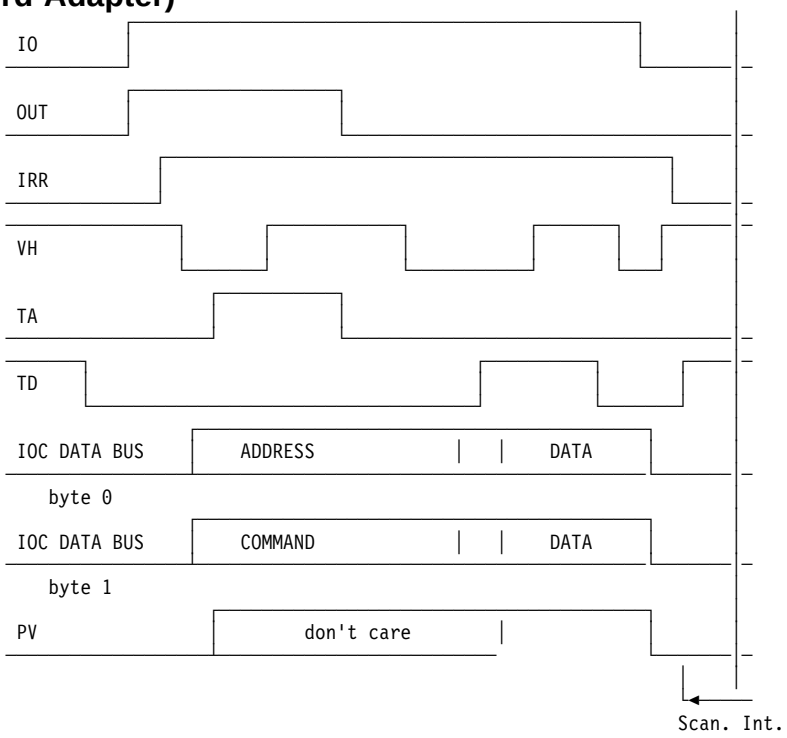


R2 = address field
R1 = data field

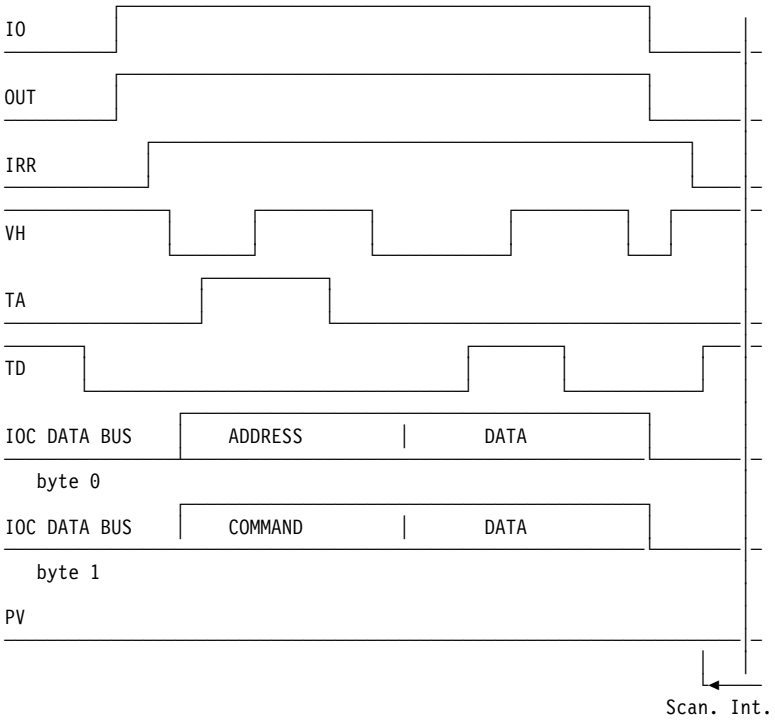
PIO operation sequence (Data Transfer):



PIO Read (Halfword Adapter)



PIO Write (Halfword Adapter)



Note: Line explanation is given starting on page 3-33.

AIO Operation

AIO Operation (Cycle Stealing)

During such an operation, several units of data are exchanged between CCU and adapter storage without CP intervention. The maximum burst of data transferred is 256 bytes.

A selected LA provides the storage addresses at which the data bytes are to be stored. For this purpose, a pointer is shared by all LAs cycle steal control word (CSCW).
This information is first placed in the adapter registers by the control program, using the IOH/IOHI instructions in PIO mode.

A selected channel adapter uses its dedicated pointer which was first loaded by the control program.

AIO Operation Sequence (Initialization):

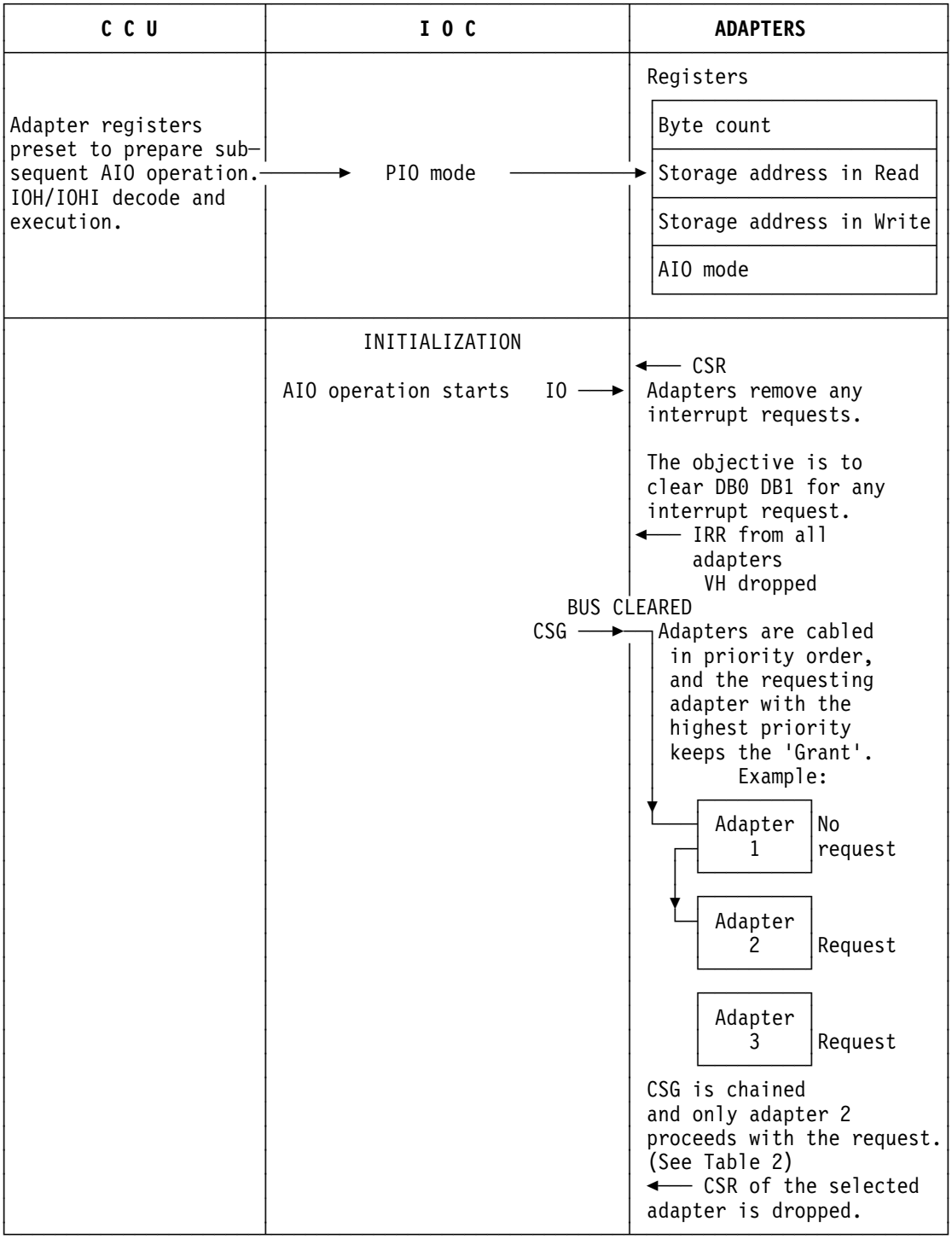


Table 1

AIO Operation Sequence (CSCW Transfer):

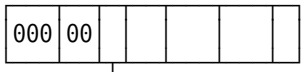
C C U	I O C	ADAPTERS
	CYCLE STEAL CONTROL WORD TRANSFER (CSCW)	
		DB0 ◄=== DB1 ◄—— VH ◄—— PV if LA AIO If CA AIO, PV may be OFF but the parity must be correct and the CCU checks it.
	Is parity correct ? Yes No = HALT ——►	
	D register contains CSCW  0 2 34 67 8 A B E F CA = 0 LA = 1 Type of operation 1 = only byte 1 in this control word is valid. 0 = both bytes of this control word are valid. Pointer LS register number only for CA. If LA, pointer register contains the address bytes X, 0, and 1 which are loaded to SAR.	
	CSG dropped	VH dropped (See Tables 3-1 and 3-2)

Table 2

AIO Operation Sequence for CA (Storage Address Transfer):

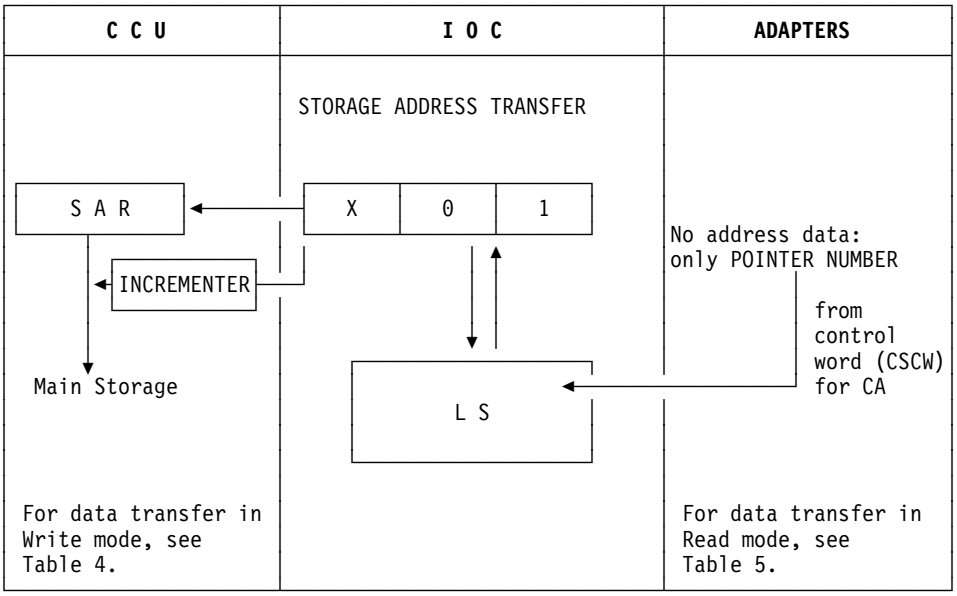


Table 3-1

AIO Operation Sequence for LA (Storage Address Transfer):

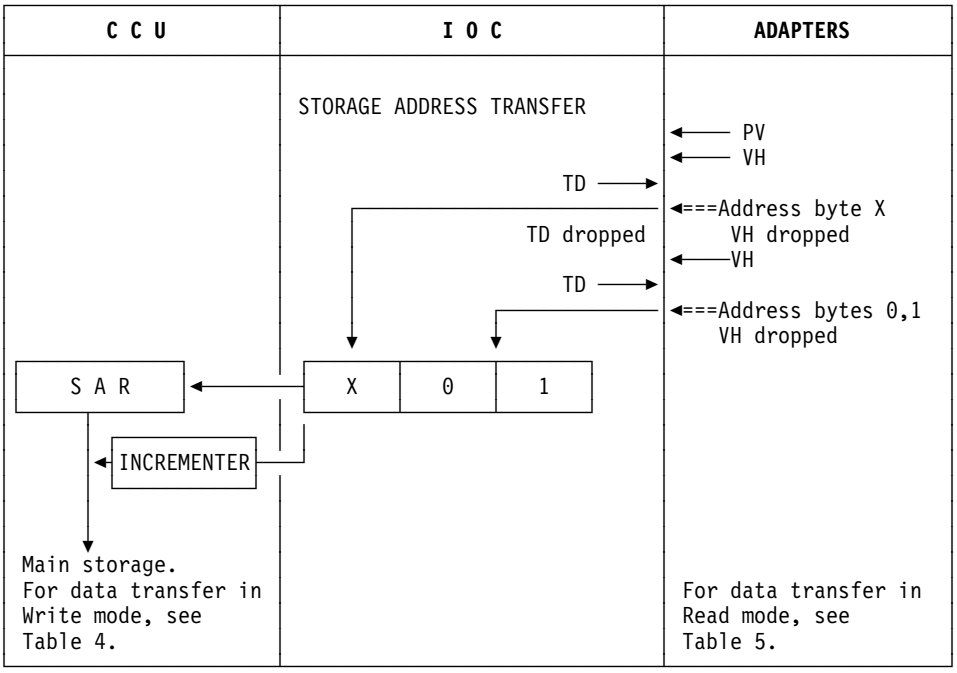


Table 3-2

AIO Operation Sequence (Data Transfer in Write):

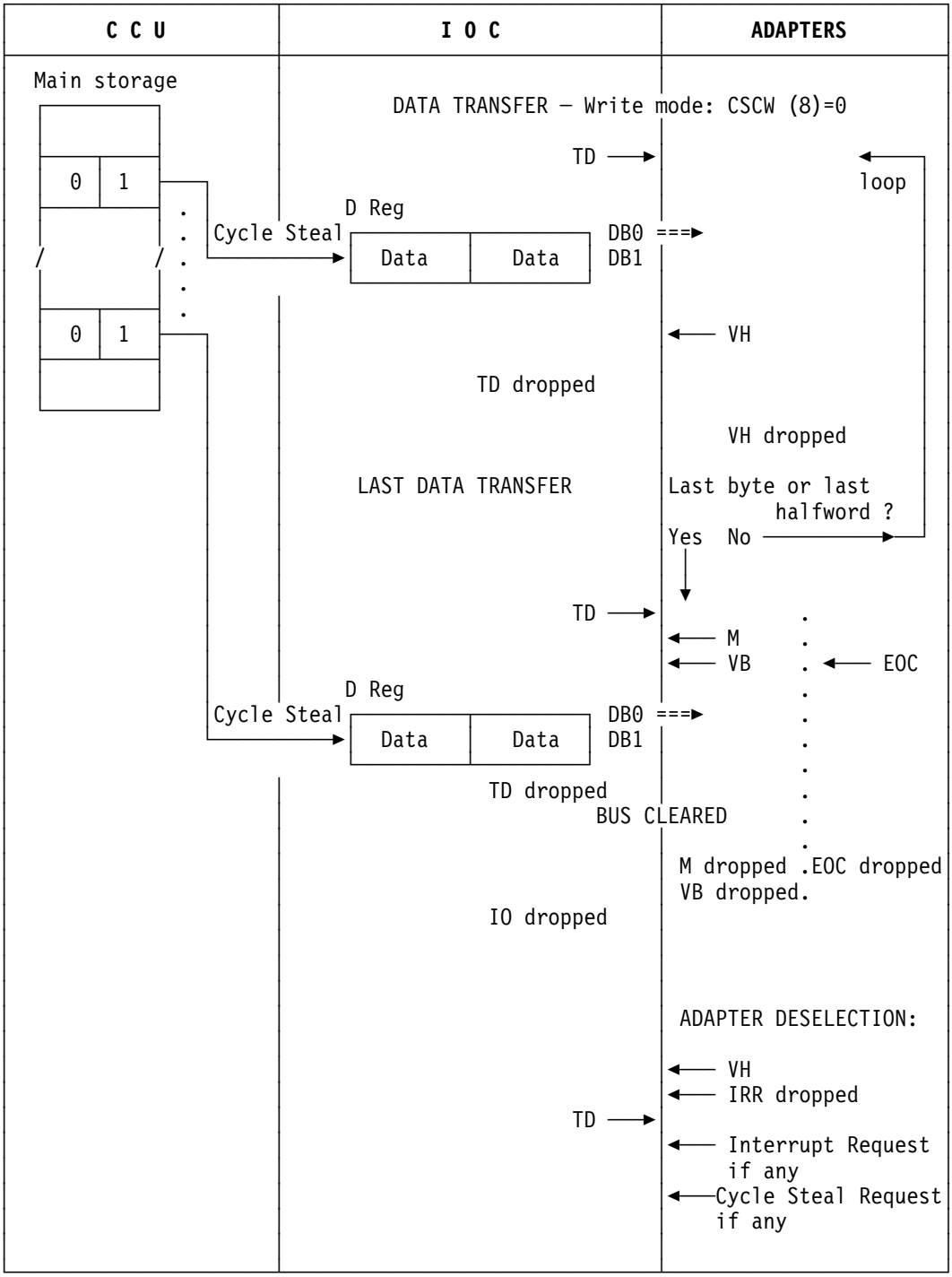


Table 4

AIO Operation Sequence (Data Transfer in Read):

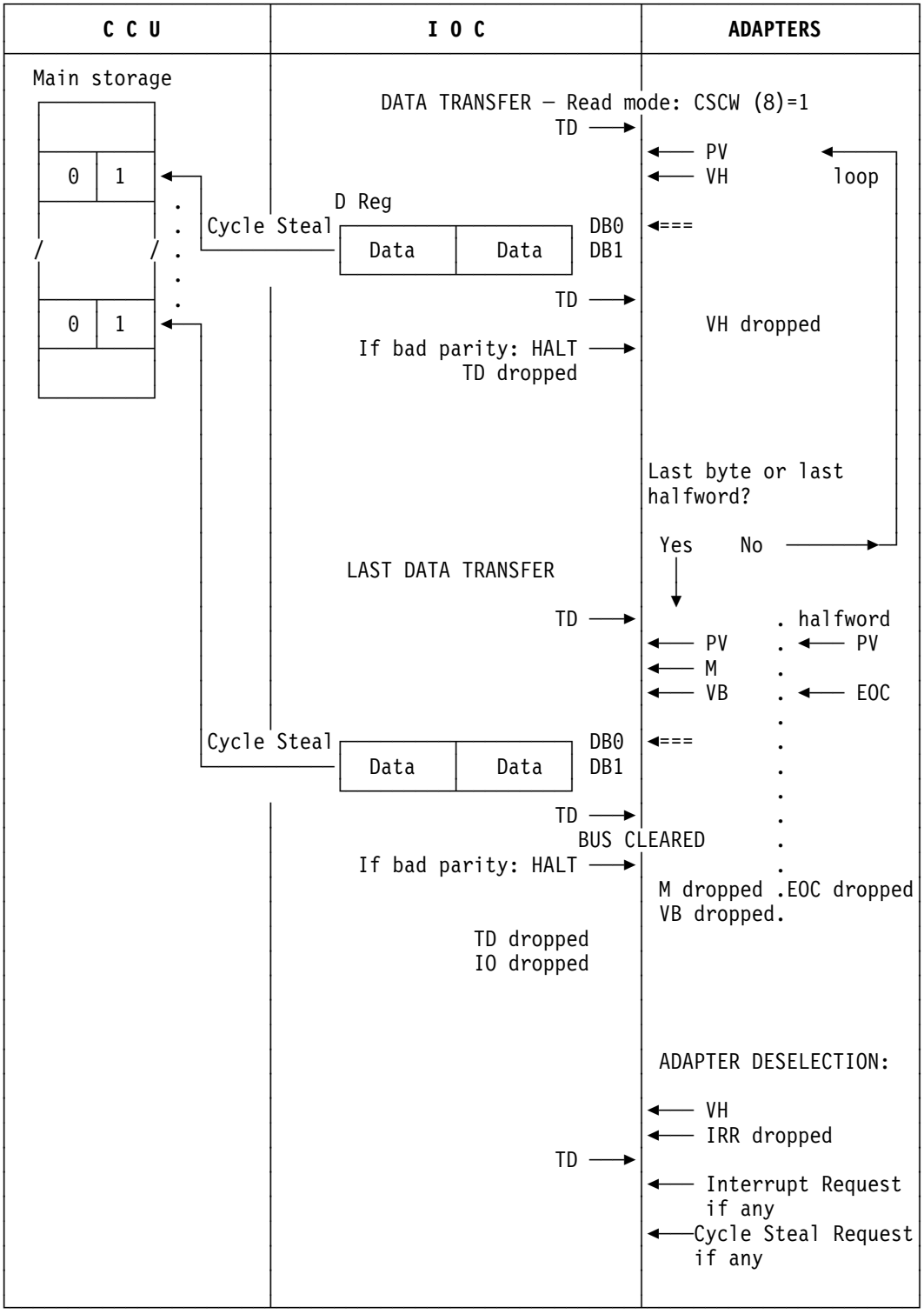
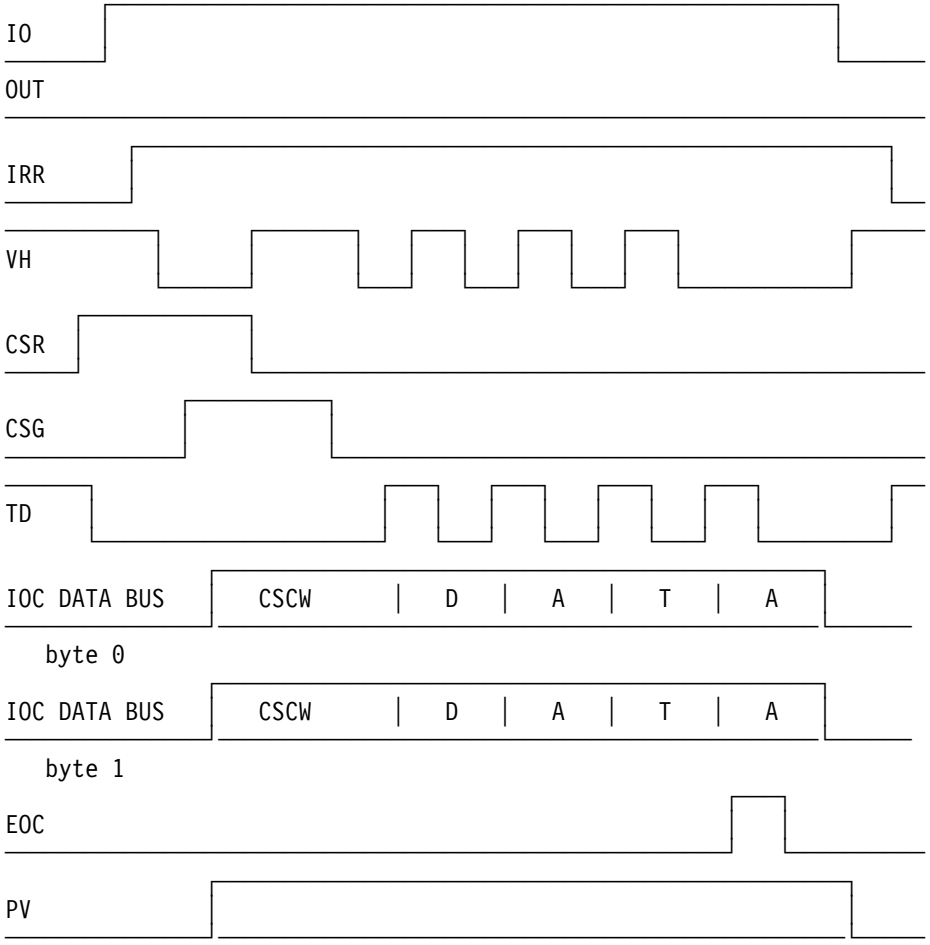


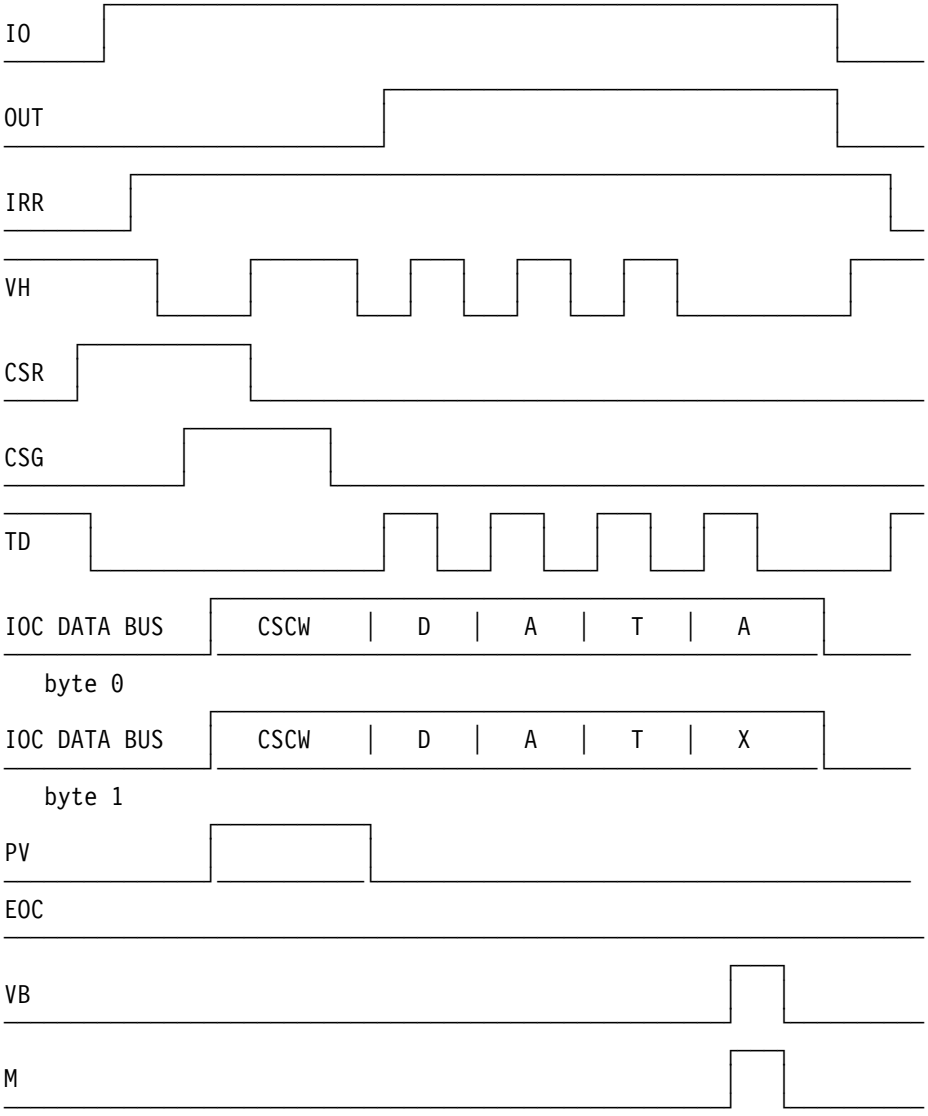
Table 5

AIO CA Read Indirect Operation (8-byte Transfer)



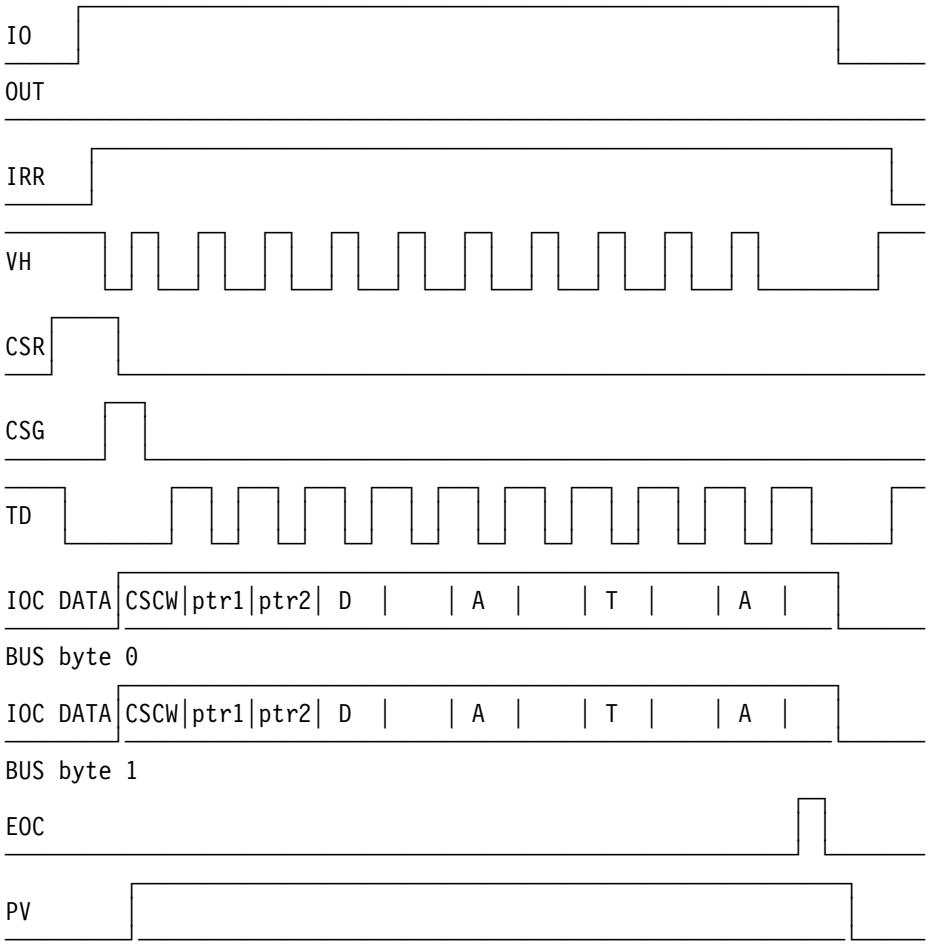
Note: The last data (byte) is in bytes 0 and 1 (same data in bytes 0 and 1 during the inbound operation (VB+M tag).

AIO CA Write Indirect Operation (7-byte Transfer)



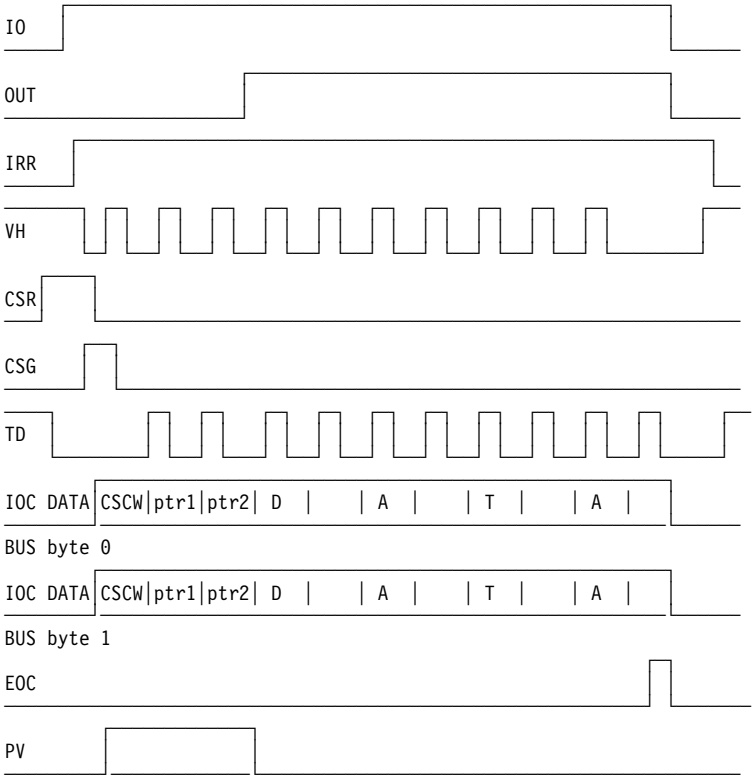
Note: The last data (byte) is in byte 0 during the outbound operation (VB+M tag).

AIO Direct/Indirect LA/TRA Read (16-byte Transfer)

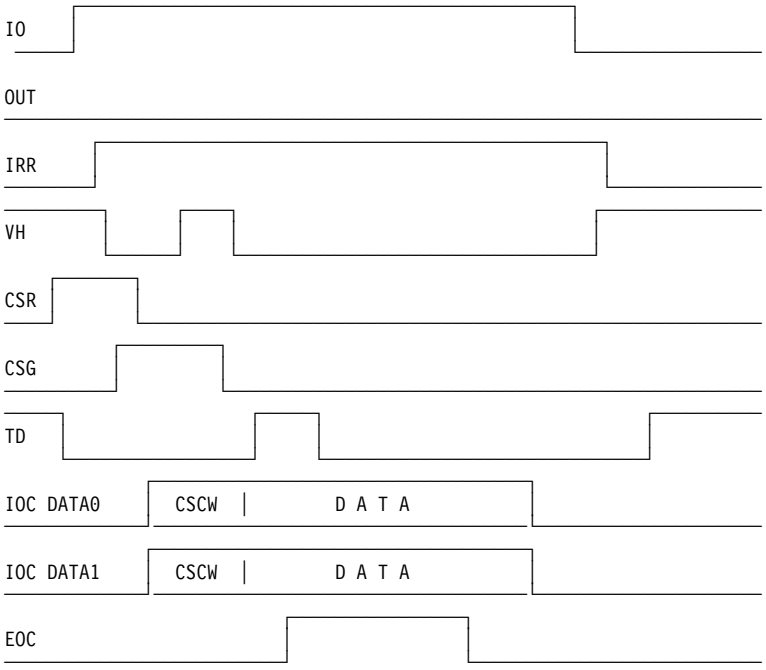


Note: The last data (byte) is in byte 1 during the read operation (VB+M tag).

AIO Direct/Indirect LA/TRA Write (16-byte Transfer)



AIO TRA Read Direct Operation (2-byte Transfer)



3746-900/3745 Attachment

From an attachement point of view, the CBC is a 3745 line adapter which is attached to IOC and DMA buses.

The CBC is connected to:

- The IOC bus from the last TSS board of the last adapter frame
- The DMA bus from the TSS board of the base frame.

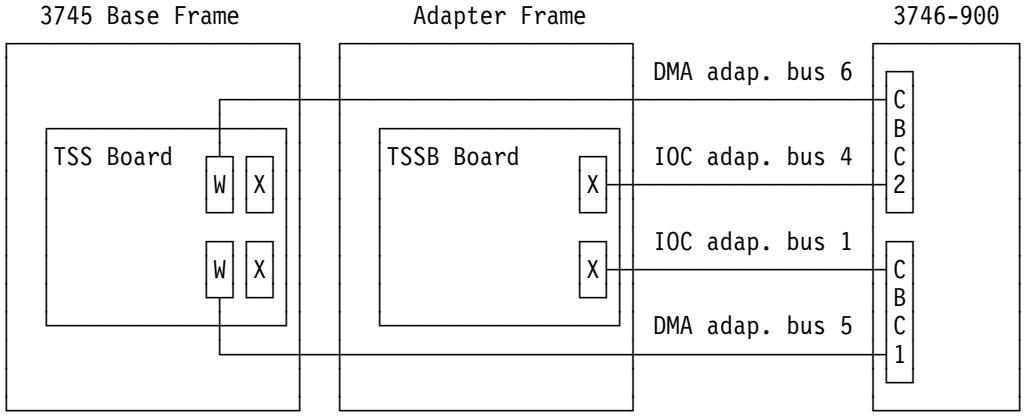


Figure 3-18. 3746 Model 900 Attachment to 3745

If the CBC2 is not installed in the 3746-900, the DMA adapter bus 6 and the IOC adapter bus 4 are connected to a terminator card located 3746-900 07R-A1.

DICO Cards

When a 3746-900 is installed, DICO cards are installed on the LAB1 board positions X and W. The IOC and DMA buses are connected to these DICO cards.

Adapter Addressing

Logical Adapter Address

A logical address is composed of:

- Type address
- Adapter group
- Slot

The address is valid at IOH/MIOH command time, in PIO mode. This command is generated by the control program or the MOSS.

- The type address defines the kind of adapter (LA, CA, or Switch) addressed by the control program, at TA time (and TD time for the CA) of the IOH.
- The adapter group defines the group of two adapters (LA or CA) on one IOC bus (IOC1 or IOC2), contained in the 3745.
- The slot gives the position of the adapter in the adapter group on one IOC bus.

Physical Address Wiring

The logical address sent on the IOC bus at TA time is compared by each adapter with its proper physical address.

- The type address part is provided by the logic of the adapter card.
- The slot and the adapter group part, (the bit of lowest weight), are imbedded in the printed circuit of the board.
- The adapter group part, (the remaining bit(s) of higher weight), is provided by the board but each board has to be personalized by a wired address.

The physical address of each adapter is provided by the following:

- WU is the IOC bus connection: IOC1 (WU = 0) or IOC2 (WU = 1)
- WS is the slot wire: Position 0 or 1 in the group
- WG1, WG2, WG3 are the group address wires.

Group Addresses per Board

LABs and CABs contain four groups of adapters. They get their physical addresses from the board printed circuit.

Using the WU and WG1 wires previously defined, the following table gives the wiring rule:

Group	WU	WG1
1	0	0
2	0	1
3	1	0
4	1	1

Wired Board Address

CAB: As there are only two CABs per machine, one wire is enough to identify the boards:

- WG2 = 0 is CAB 1, LTC1 jumper card installed on CAB 1.
- WG2 = 1 is CAB 2, LTC2 jumper card installed on CAB 2.

LAB: As there are four LABs per machine, two wires are needed to identify the four boards. The following table gives the wiring rule:

LAB	WG2	WG3
1	0	0
2	0	1
3	1	0
4	1	1

LAB board addressing is made by a jumper card on B position of the TSSB board as follow:

- Jumper card in B2 position for LAB 1
- Jumper card in B3 position for LAB 2
- Jumper card in B4 position for LAB 3
- Jumper card in B5 position for LAB 4

Bus Switch Addressing

The bus switch is like an adapter divided in two logical parts, switch A and switch B.

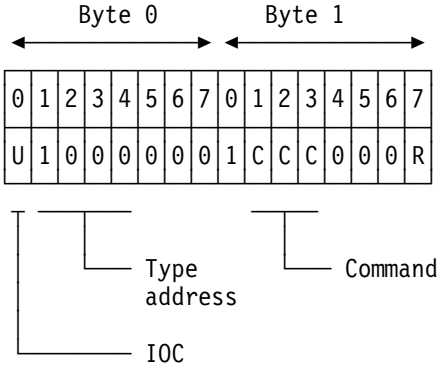
Each CCU has access only to its dedicated part and has to be able to address it to read the error buffer or to perform diagnostics.

The address has a special type address and a unique group address.
The IOH at TA time indicates the switch address:

- Byte 0, bit 0 is the switch side: 0 = IOC1
  1 = IOC2
- Byte 0, bits 1-4 is the type address: Code = 1 0 0 0 (fixed for switch)
  Byte 0, bit 5-7 are not used.
- Byte 1, bits 1-3 is the command code.
  - Reset/read error register: CCC=000
  - Write/read data register: CCC=111

  Byte 1, bit 4 indicates the origin: 0 = Control program
  1 = MOSS
  This bit is not checked by the switch hardware.
- Byte 1, bits 5-6 is the switch address : Code = 0 0
- Byte 1, bit 7 indicates read PIO:
  - 0 = Write/Reset
  - 1 = Read

IOC bus at TA time



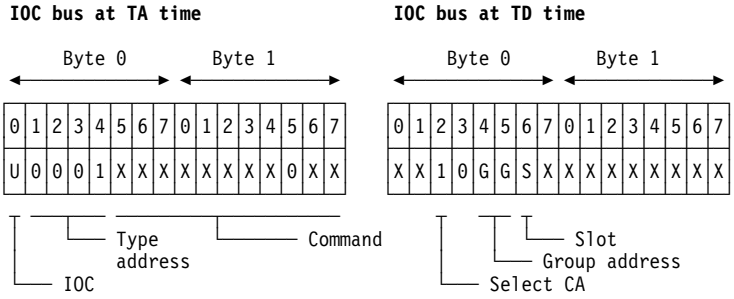
CA Addressing

PIO Mode

The number of CAs to address is sixteen. A maximum of eight CAs can be attached on the same IOC bus.
The IOH OUT '07' is the only one which selects a CA. The definition of the IOH/MIOH bit pattern is:

- Byte 0, bit 0 of TA time is the IOC connection:
  0 = IOC1
  1 = IOC2
- Byte 0, bits 1-4 is the type address: Code = 0 0 0 1 for all CAs
- Byte 0, bits 5-7 and byte 1, bits 0-7 is the
  command code = 0 0 0 0 1 1 1 x 0 x x
- Byte 1, bit 4 indicates the origin :
  0 = Control program (IOH)
  1 = MOSS (MIOH)
- The remaining part of the address is contained in the TD field. Only the MIOH command '07' is able to select a channel adapter with the following convention:
  – Byte 0, bit 2 is equal to 1 to select a CA indicated by byte 0, bits 4 to 6.
  – Byte 0, bits 4 and 5 is the group address:
    0 0 = CA Group 1
    0 1 = CA Group 2
    1 0 = CA Group 3
    1 1 = CA Group 4
  – Byte 0, bit 6 is the slot address:
    0 = Slot 1
    1 = Slot 2

Note: In case of TPS, the B interface uses the slots of the following CA, part of the same CA group. The address of the CA replaced by the B interface is lost.



		GG = 00		GG = 01		GG = 10		GG = 11	
		S=0	S=1	S=0	S=1	S=0	S=1	S=0	S=1
IOC2 U = 1	Adapter Bus 2	CA 01	CA 02	CA 03	CA 04	CA 09	CA 10	CA 11	CA 12
IOC1 U = 0	Adapter Bus 3	CA 05	CA 06	CA 07	CA 08	CA 13	CA 14	CA 15	CA 16

Channel Adapter Addresses:

			IOC bus at TA time Byte 0								**Byte 1**								**IOC bus at TD time** Byte 0							
CAB	**IOC**	**CA**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
			U	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**G**	**G**	**S**	**0**
1	2	01	1	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		0	0	0	
		02	1	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		0	0	1	
		03	1	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		0	1	0	
		04	1	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		0	1	1	
	1	05	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		0	0	0	
		06	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		0	0	1	
		07	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		0	1	0	
		08	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		0	1	1	
2	2	09	1	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		1	0	0	
		10	1	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		1	0	1	
		11	1	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		1	1	0	
		12	1	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		1	1	1	
	1	13	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		1	0	0	
		14	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		1	0	1	
		15	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		1	1	0	
		16	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			1		1	1	1	

MOSS Screen CA Address Display: As an example, address 8806 for CA 4A displayed on the MOSS screen is composed as follows:***:***

```
8 8 0 6
└┴─└┴─
  │  │
  │  v
  │  xxxx 011x = Byte 0 at TD Time,
  │              . Bits 4-5 (GG) = 01 and
  │              . Bit 6 (S) = 1
  │
  v
  1000 1xxx = Byte 0 at TA Time,
              . Bit 0 (U) = 1 and
              . Bits 1-4 (Type Address) = 0001
```

Line Adapter Addressing (LSS, HSS, and ELA)

PIO Mode

The number of line adapters to address is 32 LSS, or 28 LSS and four TRAs (with TSST board installed).

Eight high-speed or Ethernet lines can be installed in the system at line adapter addresses: LA 1, LA 2, LA 3, LA 4, LA 5, LA 6, LA 7, and LA 8. See Figure 3-12 on page 3-25.

The HSS or ELA are addressed like the LSS.

The LA address is defined at TA time of the IOH.
The line addresses for this LA are given at TD time.

The LA address is given at TA time of the IOH.

- Byte 0, bit 0 is the IOC connection:
  0 = IOC1
  1 = IOC2
- Byte 0, bits 1-4 is the type address and slot indicator.
  Three type addresses, 0 0 1 0, 0 1 0 0, and 0 1 1 0 are recognized by the line adapters.

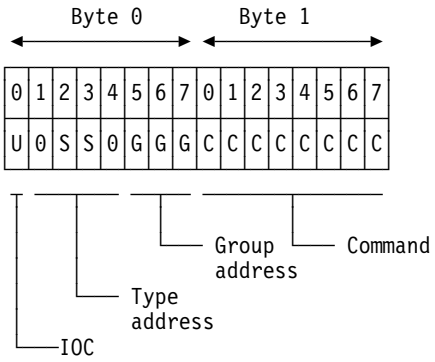
  The type address 0 1 1 0 has the meaning of command broadcast to all LAs.

  Bits 2 and 3 also have a meaning for the slot identification:

  Bits 2-3 = 01 indicates the slot 1 in a group address of one IOC bus.
  Bits 2-3 = 10 indicates the slot 2 in a group address of one IOC bus.
  Bits 2-3 = 11 broadcast to all LAs.
- Byte 0, bits 5-7 is the group address. The Group Address identifies a pair of scanners. There are eight group addresses per IOC.

  0 0 0 = Group address 1 1 0 0 = Group address 5
  0 0 1 = Group address 2 1 0 1 = Group address 6
  0 1 0 = Group address 3 1 1 0 = Group address 7
  0 1 1 = Group address 4 1 1 1 = Group address 8

IOC bus at TA time



		G=000 SS=01	G=000 SS=10	G=001 SS=01	G=001 SS=10	G=010 SS=01	G=010 SS=10	G=011 SS=01	G=011 SS=10	G=100 SS=01	G=100 SS=10	G=101 SS=01	G=101 SS=10	G=110 SS=01	G=110 SS=10	G=111 SS=01	G=111 SS=10
IOC1 U=0	Adapter Bus 1	LA 01	LA 02	LA 03	LA 04	LA 09	LA 10	LA 11	LA 12	LA 17	LA 18	LA 19	LA 20	LA 25	LA 26	LA 27	LA 28
IOC2 U=1	Adapter Bus 4	LA 05	LA 06	LA 07	LA 08	LA 13	LA 14	LA 15	LA 16	LA 21	LA 22	LA 23	LA 24	LA 29	LA 30	LA 31	LA 32

IOC bus at TA time
Byte 0

LAB	IOC	LA	0	1	2	3	4	5	6	7	Hex
			U	0	S	S	0	G	G	G	
1	1	01	0	0	0	1	0	0	0	0	10
		02	0	0	1	0	0	0	0	0	20
		03	0	0	0	1	0	0	0	1	11
		04	0	0	1	0	0	0	0	1	21
	2	05	1	0	0	1	0	0	0	0	90
		06	1	0	1	0	0	0	0	0	A0
		07	1	0	0	1	0	0	0	1	91
		08	1	0	1	0	0	0	0	1	A1
2	1	09	0	0	0	1	0	0	1	0	12
		10	0	0	1	0	0	0	1	0	22
		11	0	0	0	1	0	0	1	1	13
		12	0	0	1	0	0	0	1	1	23
	2	13	1	0	0	1	0	0	1	0	92
		14	1	0	1	0	0	0	1	0	A2
		15	1	0	0	1	0	0	1	1	93
		16	1	0	1	0	0	0	1	1	A3

IOC bus at TA time
Byte 0

LAB	IOC	LA	0	1	2	3	4	5	6	7	Hex
			U	0	S	S	0	G	G	G	
3	1	17	0	0	0	1	0	1	0	0	14
		18	0	0	1	0	0	1	0	0	24
		19	0	0	0	1	0	1	0	1	15
		20	0	0	1	0	0	1	0	1	25
	2	21	1	0	0	1	0	1	0	0	94
		22	1	0	1	0	0	1	0	0	A4
		23	1	0	0	1	0	1	0	1	95
		24	1	0	1	0	0	1	0	1	A5
4	1	25	0	0	0	1	0	1	1	0	16
		26	0	0	1	0	0	1	1	0	26
		27	0	0	0	1	0	1	1	1	17
		28	0	0	1	0	0	1	1	1	27
	2	29	1	0	0	1	0	1	1	0	96
		30	1	0	1	0	0	1	1	0	A6
		31	1	0	0	1	0	1	1	1	97
		32	1	0	1	0	0	1	1	1	A7

The line adapter addresses and the group addresses for LAB 3 and LAB 4 are obtained by setting byte 0, bit 5 to 1.

MOSS Screen LA Address Display: As an example, address A1 for LA 8 displayed on the MOSS screen is composed as follows:***:***

```
A 1
─┬─
 │
 v
1010 0001 = Byte 0 at TA Time,
            . Bit 0 (U) = 1,
            . Bits 2-3 (SS) = 10, and
            . Bits 5-7 (GGG) = 001
```

3746 Model 900 Adapter Addressing (CBC, PRC)

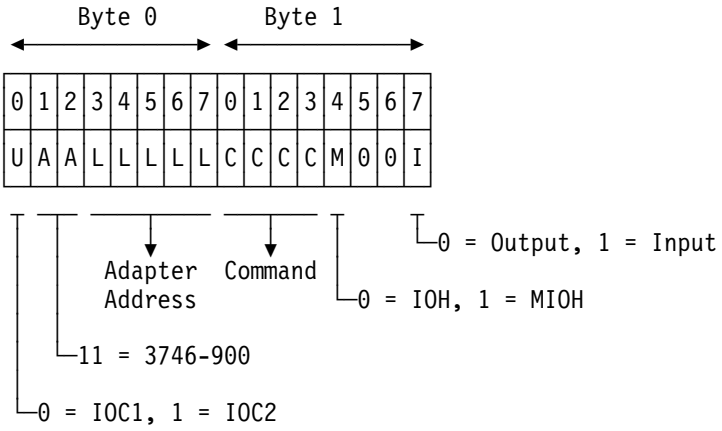
PIO Mode

The number of adapters to address is 11 processors (PRC) and two controller bus couplers (CBC).

The address is defined at TA time of the IOH.

- Byte 0, bit 0 is the IOC connection:
  0 = IOC1
  1 = IOC2
- Byte 0, bits 1-2 = 11, instruction for 3746-900.
- Byte 0, bits 3-7 indicates the adapter address.

IOC bus at TA time



How 3746-900 Adapters Are Addressed

Two cases:

1. For models 21A and 31A (one CCU-A only):
   - Through IOC1, the CCU-A addresses in the 3746-900:
     The CBSP (X'62)
     The PRCs (X'63' to X'6C')
     The CBC1 (X'7E')
2. For models 41A and 61A (two CCUs)
   - Through IOC1, the CCU-A addresses in the 3746-900:
     The CBSP (X'62)
     The TRP of CBTRP (X'63)
     The PRCs (X'64' to X'6C')
     The CBC1 (X'7E')
   - Through IOC2, the CCU-B addresses in the 3746-900:
     The CBSP (X'E2)
     The TRP of CBTRP (X'E3)
     The PRCs (X'E4' to X'EC')
     The CBC2 (X'FF')

IOC1 addressing

3746-900 Enclosure Location	Type of Adap.	0	1	2	3	4	5	6	7	Hex
		U	A	A	L	L	L	L	L	
07G-A1 F	CBSP	0	1	1	0	0	0	1	0	62
07G-A1 H	PRC[1]	0	1	1	0	0	0	1	1	63
07G-A1 K	PRC	0	1	1	0	0	1	0	0	64
07G-A1 M	PRC	0	1	1	0	0	1	0	1	65
07G-A1 P	PRC	0	1	1	0	0	1	1	0	66
07E-A1 D	PRC	0	1	1	0	0	1	1	1	67
07E-A1 F	PRC	0	1	1	0	1	0	0	0	68
07E-A1 H	PRC	0	1	1	0	1	0	0	1	69
07E-A1 K	PRC	0	1	1	0	1	0	1	0	6A
07E-A1 M	PRC	0	1	1	0	1	0	1	1	6B
07E-A1 P	PRC	0	1	1	0	1	1	0	0	6C
07N-A1 E	CBC1	0	1	1	1	1	1	1	0	7E

IOC2 Addressing

3746-900 Enclosure Location	Type of Adap.	0	1	2	3	4	5	6	7	Hex
		U	A	A	L	L	L	L	L	
07G-A1 F	CBSP	1	1	1	0	0	0	1	0	E2
07G-A1 H	TRP	1	1	1	0	0	0	1	1	E3
07G-A1 K	PRC	1	1	1	0	0	1	0	0	E4
07G-A1 M	PRC	1	1	1	0	0	1	0	1	E5
07G-A1 P	PRC	1	1	1	0	0	1	1	0	E6
07E-A1 D	PRC	1	1	1	0	0	1	1	1	E7
07E-A1 F	PRC	1	1	1	0	1	0	0	0	E8
07E-A1 H	PRC	1	1	1	0	1	0	0	1	E9
07E-A1 K	PRC	1	1	1	0	1	0	1	0	EA
07E-A1 M	PRC	1	1	1	0	1	0	1	1	EB
07E-A1 P	PRC	1	1	1	0	1	1	0	0	EC
07N-A1 G	CBC2	1	1	1	1	1	1	1	1	FF

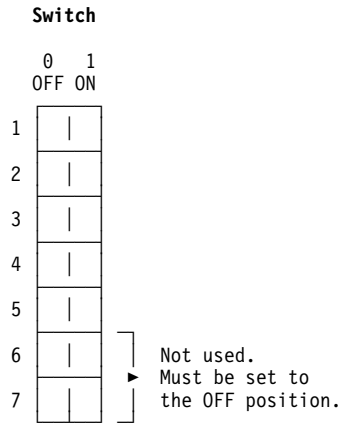
[1] When two CCUs (model 41A or 61A) a TRP (of CBTRA) replaces the PRC on IOC1.

For more details on 3746-900 see, *3746 Model 900 Hardware Maintenance Reference,* online documentation.

LIC Board Addressing

The LIC board address is set with a seven-position switch located on A1 position of the LIC board.

For location, see page YZ038 or YZ039.



Frame	Board	Switch 1	2	3	4	5	6	7
01	01P-B2	0	0	0	0	0	0	0
	01P-B1	1	0	0	0	0	0	0
	01M-B2	0	1	0	0	0	0	0
	01M-B1	1	1	0	0	0	0	0
04	04D-B2	0	0	0	1	0	0	0
	04D-B1	1	0	0	1	0	0	0
	04G-B2	0	1	0	1	0	0	0
	04G-B1	1	1	0	1	0	0	0
	04B-B2	0	0	1	1	0	0	0
	04B-B1	1	0	1	1	0	0	0
	04E-B2	0	1	1	1	0	0	0
	04E-B1	1	1	1	1	0	0	0
05	05D-B2	0	0	0	0	1	0	0
	05D-B1	1	0	0	0	1	0	0
	05G-B2	0	1	0	0	1	0	0
	05G-B1	1	1	0	0	1	0	0
	05B-B2	0	0	1	0	1	0	0
	05B-B1	1	0	1	0	1	0	0
	05E-B2	0	1	1	0	1	0	0
	05E-B1	1	1	1	0	1	0	0
06	06D-B2	0	0	0	1	1	0	0
	06D-B1	1	0	0	1	1	0	0
	06G-B2	0	1	0	1	1	0	0
	06G-B1	1	1	0	1	1	0	0
	06B-B2	0	0	1	1	1	0	0
	06B-B1	1	0	1	1	1	0	0
	06E-B2	0	1	1	1	1	0	0
	06E-B1	1	1	1	1	1	0	0

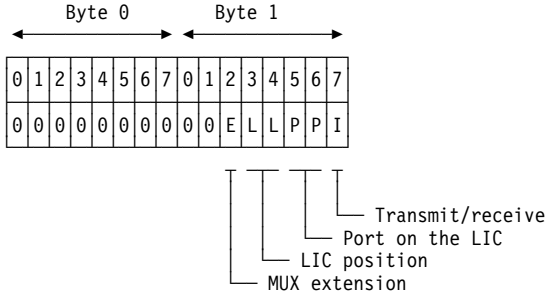
Figure 3-19. LIC Board Addressing Switch Position

Line Addressing

The line address used by the control program is composed of the LA address, previously defined, and of the LIC/PORT address given at TD time of the IOH using byte 1, bits 2 to 7:

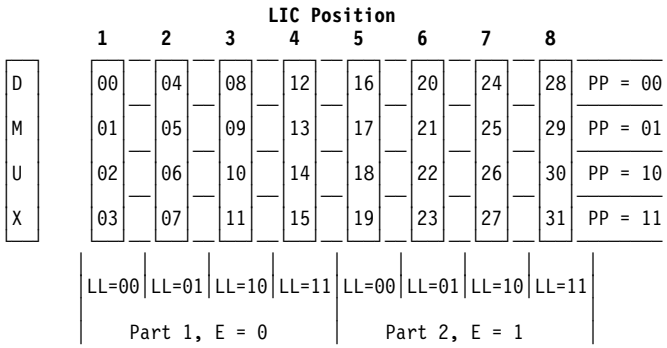
LIC1 LIC3 LIC4A and LIC4B Addressing

IOC bus at TD time



- Byte 1, bit 2 identifies the part 1 or 2 in the LIC board (MUX extension).
  - Bit 2 = 0: the scanner controls the part 1 in the LIC board
  - Bit 2 = 1: the scanner controls the part 2 in the LIC board.
- Byte 1, bits 3-4 indicates the LIC position in the part 1 or 2.
  - 00 = First LIC in part 1 or 2
  - 01 = Second LIC in part 1 or 2
  - 10 = Third LIC in part 1 or 2
  - 11 = Fourth LIC in part 1 or 2
- Byte 1, bits 5-6 indicates the port of the LIC.
  - 00 = First port
  - 01 = Second port
  - 10 = Third port
  - 11 = Fourth port

  LIC Type 1 and LIC Type 4A have four ports.
  LIC type 3 and LIC type 4B have only one port.
- Byte 1, bit 7 indicates the transmit or receive address.
  - When bit 7 = 1: receive address.
  - When bit 7 = 0: transmit address.



TSS Line Addressing for LICs 1-4

During Transmit Operation

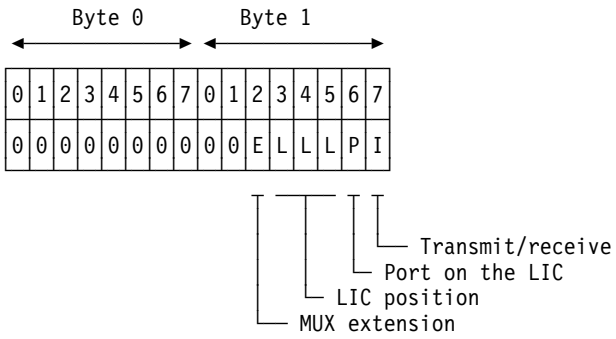
Line	Byte 1								Hex
	0	0	E	L	L	P	P	I	
00	0	0	0	0	0	0	0	0	00
01	0	0	0	0	0	0	1	0	02
02	0	0	0	0	0	1	0	0	04
03	0	0	0	0	0	1	1	0	06
04	0	0	0	0	1	0	0	0	08
05	0	0	0	0	1	0	1	0	0A
06	0	0	0	0	1	1	0	0	0C
07	0	0	0	0	1	1	1	0	0E
08	0	0	0	1	0	0	0	0	10
09	0	0	0	1	0	0	1	0	12
10	0	0	0	1	0	1	0	0	14
11	0	0	0	1	0	1	1	0	16
12	0	0	0	1	1	0	0	0	18
13	0	0	0	1	1	0	1	0	1A
14	0	0	0	1	1	1	0	0	1C
15	0	0	0	1	1	1	1	0	1E
16	0	0	1	0	0	0	0	0	20
17	0	0	1	0	0	0	1	0	22
18	0	0	1	0	0	1	0	0	24
19	0	0	1	0	0	1	1	0	26
20	0	0	1	0	1	0	0	0	28
21	0	0	1	0	1	0	1	0	2A
22	0	0	1	0	1	1	0	0	2C
23	0	0	1	0	1	1	1	0	2E
24	0	0	1	1	0	0	0	0	30
25	0	0	1	1	0	0	1	0	32
26	0	0	1	1	0	1	0	0	34
27	0	0	1	1	0	1	1	0	36
28	0	0	1	1	1	0	0	0	38
29	0	0	1	1	1	0	1	0	3A
30	0	0	1	1	1	1	0	0	3C
31	0	0	1	1	1	1	1	0	3E

During Receive Operation

Line	Byte 1								Hex
	0	0	E	L	L	P	P	I	
00	0	0	0	0	0	0	0	1	01
01	0	0	0	0	0	0	1	1	03
02	0	0	0	0	0	1	0	1	05
03	0	0	0	0	0	1	1	1	07
04	0	0	0	0	1	0	0	1	09
05	0	0	0	0	1	0	1	1	0C
06	0	0	0	0	1	1	0	1	0D
07	0	0	0	0	1	1	1	1	0F
08	0	0	0	1	0	0	0	1	11
09	0	0	0	1	0	0	1	1	13
10	0	0	0	1	0	1	0	1	15
11	0	0	0	1	0	1	1	1	17
12	0	0	0	1	1	0	0	1	19
13	0	0	0	1	1	0	1	1	1B
14	0	0	0	1	1	1	0	1	1D
15	0	0	0	1	1	1	1	1	1F
16	0	0	1	0	0	0	0	1	21
17	0	0	1	0	0	0	1	1	23
18	0	0	1	0	0	1	0	1	25
19	0	0	1	0	0	1	1	1	27
20	0	0	1	0	1	0	0	1	29
21	0	0	1	0	1	0	1	1	2B
22	0	0	1	0	1	1	0	1	2B
23	0	0	1	0	1	1	1	1	2F
24	0	0	1	1	0	0	0	1	31
25	0	0	1	1	0	0	1	1	33
26	0	0	1	1	0	1	0	1	35
27	0	0	1	1	0	1	1	1	37
28	0	0	1	1	1	0	0	1	39
29	0	0	1	1	1	0	1	1	3B
30	0	0	1	1	1	1	0	1	3D
31	0	0	1	1	1	1	1	1	3F

LIC5 and LIC6 Addressing

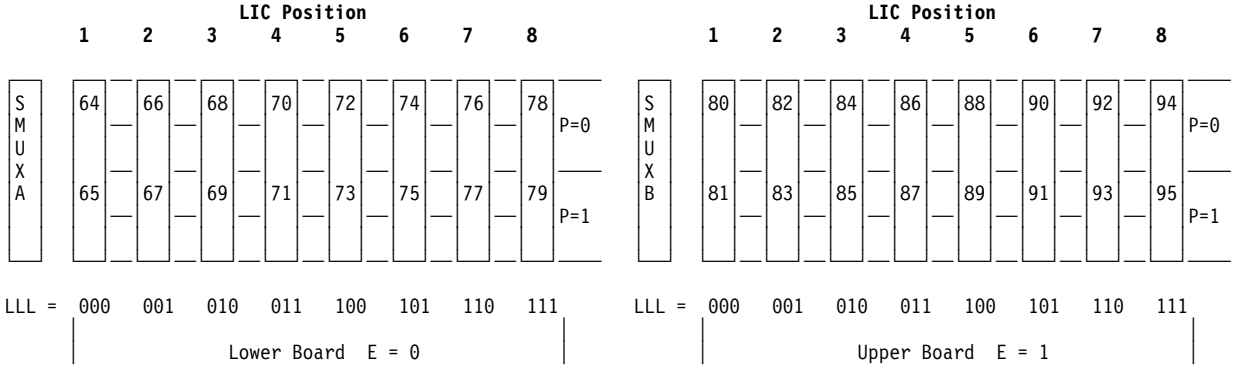
IOC bus at TD time



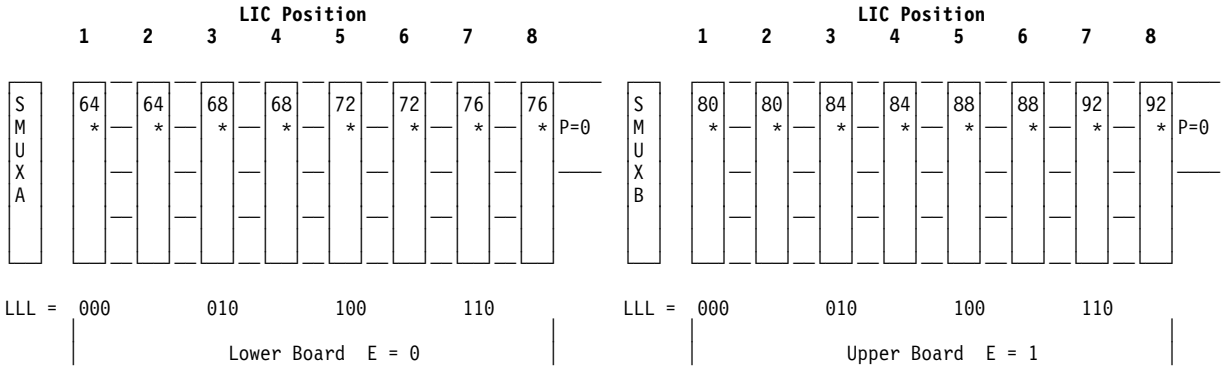
- Byte 1, bit 2 identifies the LIC board in the LIC unit.
  - Bit 2 = 0: the scanner controls the lower board in the LIC unit.
  - Bit 2 = 1: the scanner controls the upper board in the LIC unit.
- Byte 1, bits 3-5 indicate the LIC position in the LIC board.
  - 000 = LIC position 1
  - 001 = LIC position 2
  - 010 = LIC position 3
  - 011 = LIC position 4
  - 100 = LIC position 5
  - 101 = LIC position 6
  - 110 = LIC position 7
  - 111 = LIC position 8
- Byte 1, bit 6 indicates the port of the LIC.
  - 0 = First port
  - 1 = Second port

  LIC type 5 has two ports.
  LIC type 6 has only one port.
- Byte 1, bit 7 indicates the transmit or receive address.
  - When bit 7 = 1: receive address.
  - When bit 7 = 0: transmit address.

Port Position for LIC Type 5 and LIC Type 6 at 9.6 and 19.2 kbps:



Port Position for LIC Type 6 at 56 kbps:



* = The LIC cassette can be plugged in either an odd position, or in the even position next to it on the LIC board.

For plugging restrictions refer to “LIC6, Plugging Limitations” on page 4-13.

Note: LIC type 5 and LIC type 6 are installed starting from line address 064 on LIC unit 01M.

TSS Line Addressing for LICs 5-6

During Transmit Operation

Line	Byte 1 0	0	E	L	L	L	P	I	Hex
64	0	0	0	0	0	0	0	0	00
65	0	0	0	0	0	0	1	0	02
66	0	0	0	0	0	1	0	0	04
67	0	0	0	0	0	1	1	0	06
68	0	0	0	0	1	0	0	0	08
69	0	0	0	0	1	0	1	0	0A
70	0	0	0	0	1	1	0	0	0C
71	0	0	0	0	1	1	1	0	0E
72	0	0	0	1	0	0	0	0	10
73	0	0	0	1	0	0	1	0	12
74	0	0	0	1	0	1	0	0	14
75	0	0	0	1	0	1	1	0	16
76	0	0	0	1	1	0	0	0	18
77	0	0	0	1	1	0	1	0	1A
78	0	0	0	1	1	1	0	0	1C
79	0	0	0	1	1	1	1	0	1E
80	0	0	1	0	0	0	0	0	20
81	0	0	1	0	0	0	1	0	22
82	0	0	1	0	0	1	0	0	24
83	0	0	1	0	0	1	1	0	26
84	0	0	1	0	1	0	0	0	28
85	0	0	1	0	1	0	1	0	2A
86	0	0	1	0	1	1	0	0	2C
87	0	0	1	0	1	1	1	0	2E
88	0	0	1	1	0	0	0	0	30
89	0	0	1	1	0	0	1	0	32
90	0	0	1	1	0	1	0	0	34
91	0	0	1	1	0	1	1	0	36
92	0	0	1	1	1	0	0	0	38
93	0	0	1	1	1	0	1	0	3A
94	0	0	1	1	1	1	0	0	3C
95	0	0	1	1	1	1	1	0	3E

During Receive Operation

Line	Byte 1 0	0	E	L	L	L	P	I	Hex
64	0	0	0	0	0	0	0	1	01
65	0	0	0	0	0	0	1	1	03
66	0	0	0	0	0	1	0	1	05
67	0	0	0	0	0	1	1	1	07
68	0	0	0	0	1	0	0	1	09
69	0	0	0	0	1	0	1	1	0C
70	0	0	0	0	1	1	0	1	0D
71	0	0	0	0	1	1	1	1	0F
72	0	0	0	1	0	0	0	1	11
73	0	0	0	1	0	0	1	1	13
74	0	0	0	1	0	1	0	1	15
75	0	0	0	1	0	1	1	1	17
76	0	0	0	1	1	0	0	1	19
77	0	0	0	1	1	0	1	1	1B
78	0	0	0	1	1	1	0	1	1D
79	0	0	0	1	1	1	1	1	1F
80	0	0	1	0	0	0	0	1	21
81	0	0	1	0	0	0	1	1	23
82	0	0	1	0	0	1	0	1	25
83	0	0	1	0	0	1	1	1	27
84	0	0	1	0	1	0	0	1	29
85	0	0	1	0	1	0	1	1	2B
86	0	0	1	0	1	1	0	1	2B
87	0	0	1	0	1	1	1	1	2F
88	0	0	1	1	0	0	0	1	31
89	0	0	1	1	0	0	1	1	33
90	0	0	1	1	0	1	0	1	35
91	0	0	1	1	0	1	1	1	37
92	0	0	1	1	1	0	0	1	39
93	0	0	1	1	1	0	1	1	3B
94	0	0	1	1	1	1	0	1	3D
95	0	0	1	1	1	1	1	1	3F

HPTSS Line Addressing

Up to two lines can be addressed for each HPTSS, but only one is active at a time.

Byte 1 bit 6 selects the port:

- 0 = port 1
- 1 = port 2

Line numbers 1024 through 1039 are dedicated for HPTSS use.

For TSSB Board

TSSB Board 01G-A1 EAC Card Position	Port	Line Address Decimal	Line Address Hex	Tailgate Position*
F	Port 1	1024	400	1 J2
F	Port 2	1025	401	1 J1
H	Port 1	1026	402	2 J2
H	Port 2	1027	403	2 J1
K	Port 1	1028	404	3 J2
K	Port 2	1029	405	3 J1
M	Port 1	1030	406	4 J2
M	Port 2	1031	407	4 J1
P	Port 1	1032	408	5 J2
P	Port 2	1033	409	5 J1
R	Port 1	1034	40A	6 J2
R	Port 2	1035	40B	6 J1
T	Port 1	1036	40C	7 J2
T	Port 2	1037	40D	7 J1
V	Port 1	1038	40E	8 J2
V	Port 2	1039	40F	8 J1

* = See page YZ044 for connector location

For TSST Board

TSST Board 01G-A1 EAC Card Position	Port	Line Address Decimal	Line Address Hex	Tailgate Position*
H	Port 1	1028	404	5 J2
H	Port 2	1029	405	5 J1
K	Port 1	1030	406	6 J2
K	Port 2	1031	407	6 J1
T	Port 1	1036	40C	7 J2
T	Port 2	1037	40D	7 J1
V	Port 1	1038	40E	8 J2
V	Port 2	1039	40F	8 J1

* = See page YZ044 for connector location

ESS Line Addressing

Up to two lines can be addressed for each ESS.

Byte 1 bit 6 selects the port:

- 0 = port 1
- 1 = port 2

Line numbers 1056 through 1071 are dedicated for ESS use.

For TSSB Board

TSSB Board 01G-A1 EAC Card Position	Port	Line Address Decimal	Hex	Tailgate Position*
F	Port 1	1056	420	1 J2
F	Port 2	1057	421	1 J1
H	Port 1	1058	422	2 J2
H	Port 2	1059	423	2 J1
K	Port 1	1060	424	3 J2
K	Port 2	1061	425	3 J1
M	Port 1	1062	426	4 J2
M	Port 2	1063	427	4 J1
P	Port 1	1064	428	5 J2
P	Port 2	1065	429	5 J1
R	Port 1	1066	42A	6 J2
R	Port 2	1067	42B	6 J1
T	Port 1	1068	42C	7 J2
T	Port 2	1069	42D	7 J1
V	Port 1	1070	42E	8 J2
V	Port 2	1071	42F	8 J1

* = See page YZ044 for connector location

For TSST Board

TSST Board 01G-A1 EAC Card Position	Port	Line Address Decimal	Hex	Tailgate Position*
H	Port 1	1060	424	5 J2
H	Port 2	1061	425	5 J1
K	Port 1	1062	426	6 J2
K	Port 2	1063	427	6 J1
T	Port 1	1068	42C	7 J2
T	Port 2	1069	42D	7 J1
V	Port 1	1070	42E	8 J2
V	Port 2	1071	42F	8 J1

* = See page YZ044 for connector location

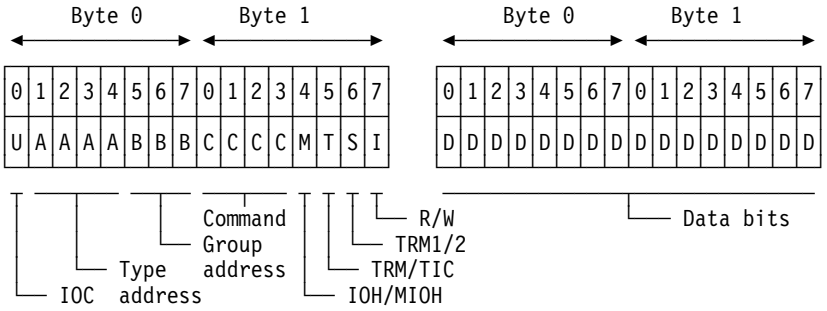
Token-Ring Adapter (TRA) Addressing

Four TRMs can be installed on the 3745. They have the positions of the line adapters 01, 02, 05, and 06.

They are addressed at TA time of the IOH.
The TRM address is included in the TA halfword of the IOH.

- Byte 0, bit 0 is the IOC connection.
- Byte 0, bits 1-4 is the type address and is equal to 1 0 0 1.
- Byte 0, bits 5-7 is the group address. This group address is unique and always set to 0 0 0.
- Byte 1, bit 4 indicates the origin: 0 = Control program
  1 = MOSS
- Byte 1, bit 5 indicates whether a TRM or a TIC is addressed:
  - Bit 5 = 0 indicates a command to a TIC.
  - Bit 5 = 1 indicates a command to a TRM.
- Byte 1, bit 6 is the slot address: 0 = Slot 1
  1 = Slot 2

IOC bus at TA time **IOC bus at TD time**



IOC bus at TA time

IOC	TRM	LA Pos	Byte 0								Byte 1							
			0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
			U	A	A	A	A	B	B	B	C	C	C	C	M	T	S	I
1	1	1	0	1	0	0	1	0	0	0			0	0		1	0	
	2	2	0	1	0	0	1	0	0	0			0	0		1	1	
2	3	5	1	1	0	0	1	0	0	0			0	0		1	0	
	4	6	1	1	0	0	1	0	0	0			0	0		1	1	

Token-Ring Line Addressing

Four token-ring adapters can be installed on the base frame and have the addresses of the line adapters: LA 1, LA 2, LA 5, and LA 6. See Figure 3-12 on page 3-25. They are addressed at TA time of the IOH One TRM controls 2 TICs. Byte 1, bits 2 and 3 from the command are used to identify one of the TICs.

- If bits 2 and 3 = 0 0, TIC 1 is addressed.
- If bits 2 and 3 = 0 1, TIC 2 is addressed.

The TIC is addressed when byte 1, bit 5 = 0.

Token-Ring Address

IOC bus at TA time

			Byte 0								Byte 1							
IOC	**TRM**	**TIC**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
			U	**A**	**A**	**A**	**A**	**B**	**B**	**B**	**C**	**C**	**C**	**C**	**M**	**T**	**S**	**I**
1	1	1	0	1	0	0	1	0	0	0			0	0		0	0	
		2	0	1	0	0	1	0	0	0			0	1		0	0	
	2	3	0	1	0	0	1	0	0	0			0	0		0	1	
		4	0	1	0	0	1	0	0	0			0	1		0	1	
2	3	5	1	1	0	0	1	0	0	0			0	0		0	0	
		6	1	1	0	0	1	0	0	0			0	1		0	0	
	4	7	1	1	0	0	1	0	0	0			0	0		0	1	
		8	1	1	0	0	1	0	0	0			0	1		0	1	

Line numbers 1088 through 1095 are dedicated for TRSS use.

TSST Board 01G-A1 TRA Card Position	TIC	Line Address Decimal	Line Address Hex	Tailgate Position*
B	1	1088	440	1 J1
C	2	1089	441	1 J2
E	1	1090	442	2 J1
F	2	1091	443	2 J2
M	1	1092	444	3 J1
N	2	1093	445	3 J2
Q	1	1094	446	4 J1
R	2	1095	447	4 J2

* = See page YZ044 for connector location

Note: More token-ring connections can be provided through the 3746-900. Refer to the *3746-900 Hardware Maintenance Reference* (online documentation) for details.

Bypass Card

Bypass cards are used on each IOC and DMA buses for bus serial lines strapping.

Two types of bypass cards:

1. BPC1 or BPC2 is a passive bypass card (jumper card).
2. ABP1 or ABP2 is an active bypass card (need of +8.5 V supplied by the CBSP and CBTRP in the 3746-900).

Bypass Card Plugging Rules

- ABP1 is installed in the first odd CSP position following the last adapter installed.
- ABP2 is installed in the first odd FES (FESH/FESL/EAC) position following the last adapter installed.
- BPC1 is installed in all CSP positions following the last adapter installed.
- BPC1 is installed in all FES (FESH/FESL/EAC) positions in the LAB1 (base frame) following the last adapter installed.
- BPC2 is installed in all TRM positions in a TSST board.

Note: BPC1 or BPC2 are needed for continuity of daisy chain, even if there is a missing adapter on the adapter busses. Following scenario (next pages) illustrates this.

Bypass Mechanism for LAs

This procedure is valid only for 3745 Models 210-610 and for models 21A-61A if no 3746 Model 900 is installed.

Adapter Plugging Rules

1. If the PS feeding two LAs is ON:
   a. Never remove the odd LA or replace it by a BPC card if an LA is plugged in the even position.
   b. You can remove the even LA but you must replace it by a BPC card if an LA is plugged in the odd position.
2. If one PS feeding two LAs is OFF:
   a. You can remove one or both LAs without plugging in any BPC card.
   b. If BPC cards are plugged in both positions, you can power OFF the next PS but not the preceding PS.
      If not, never power OFF the next or the preceding PS.
   c. Never run the IOC diagnostics (routines IA09, 10 and JA09, and 10 will fail).
3. If two consecutive PSs feeding four LAs are OFF:
   a. BPC cards and only BPC cards must be plugged in the first two LA positions of the string.
   b. No LA or BPC cards are needed in the next two positions of the string.
   c. If BPC cards are plugged in the four positions, you can power OFF the next PS.
      If not, never power OFF the next or the preceding PS.
   d. Never run the IOC diagnostics (routines IA09, 10 and JA09, and 10 will fail).
4. If several non-consecutive PSs are OFF:
   a. You can remove all the cards powered OFF without plugging any BPC card in.
   b. For each PS OFF, apply the same restrictions as for one PS OFF.

Note: LA cards are not hot pluggable.

Cycle Steal Grant (CSG) Theory for TSS/HPTSS/ESS/TRSS

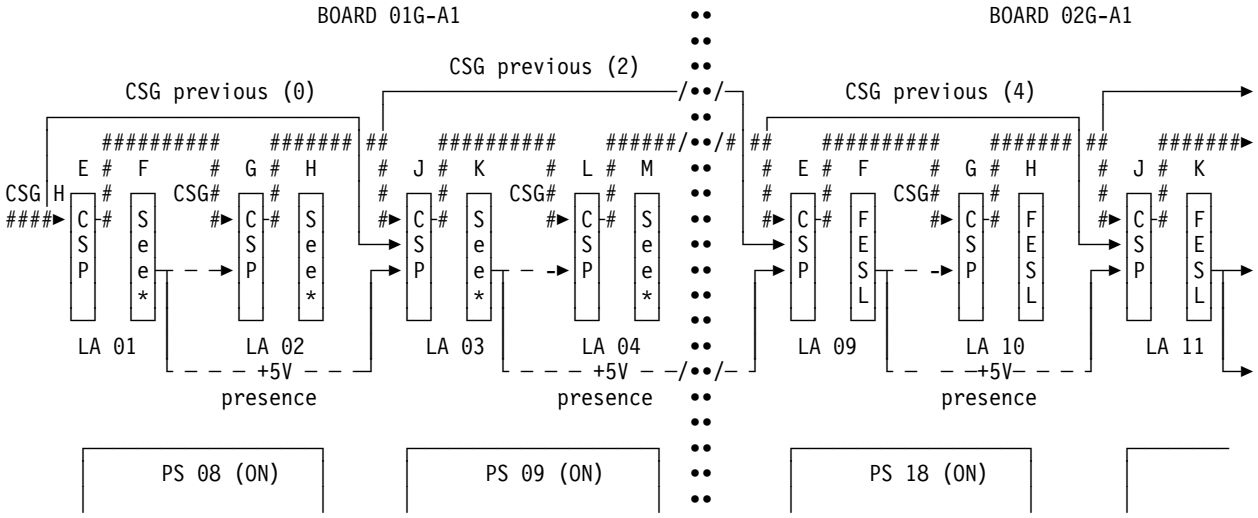
Refer to the drawing below.

- The bypass mechanism is under power control through the 'presence' line level.
- The 'presence' level switches from +5V to ground if the PS is OFF or if there is no FESx card plugged in the odd position.
- If the 'presence' level is +5V, the first CSP of the next PS uses the 'CSG-H' line as input.
- If the 'presence' level is ground, the first CSP of the next PS uses the 'CSG previous' line as input.

Cycle Steal Grant (CSG) Scenario for TSS/HPTSS/ESS/TRSS

All PSs are ON and no Adapters are Missing on the Bus

All the 'presence' lines are at +5V level, so all CSP or TRM cards use the 'CSG' as input line.
The 'CSG previous' line is never used.



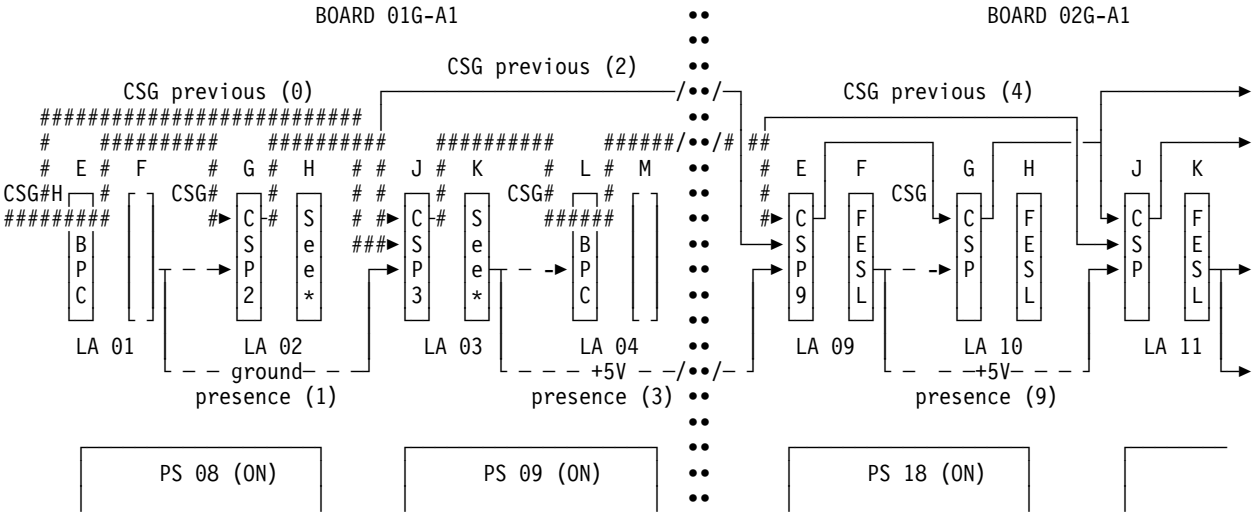
* = Can be an FESL, FESH, or EAC card.

CSG path defined by the bypass mechanism for this example of configuration

Some PSs are OFF or some Adapters are Missing on the Bus

A - If the PS is ON:

1. No LA card in position 01 (LA01 in the drawing) ===> **not allowed**
   - As there is no FESx card in position 1, the 'presence (1)' line is at ground level.
     As the 'presence (1)' line is at ground level, the CSP3 card knows that it must use the 'CSG previous 0' line and:
     – If no BPC card is plugged in position 1, 'CSG' will not be propagated to CSP2 and LA02 will never receive 'CSG'.
     – If a BPC card is plugged in position 1, it will propagate concurrently 'CSG' to the CSP2 and in case of 'CSR' from LAs 02 and 03, both LAs 02 and 03 will answer the request, leading to a bus error.
2. No LA card in position 02 (LA 04 in the drawing) ===> **allowed with BPC card**
   - As the FESx card is plugged in position 3, the 'presence (3)' line level is +5V; thus CSP9 uses as input the 'CSG' line coming from LA04 ; as there is no CSP card in that position, a 'BPC' card must be plugged in to propagate the 'CSG' line from CSP3 to CSP9.

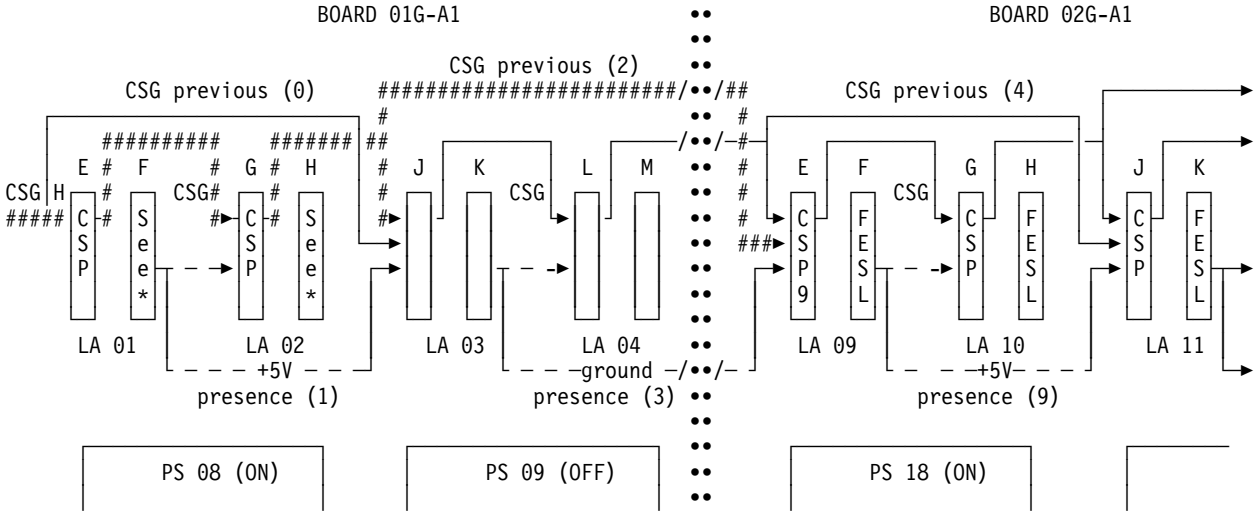


* = Can be an FESL, FESH, or EAC card.

\# CSG path defined by the bypass mechanism for this example of configuration

***B - If one PS is OFF (09 in the drawing) ===>* allowed**

- The level of the 'presence (3)' line switches from +5V to ground. Thus, the CSP9 card knows that it must use the 'CSG previous (2)' line instead of the 'CSG' line.
- No adapter or bypass cards are needed to propagate the CSG.



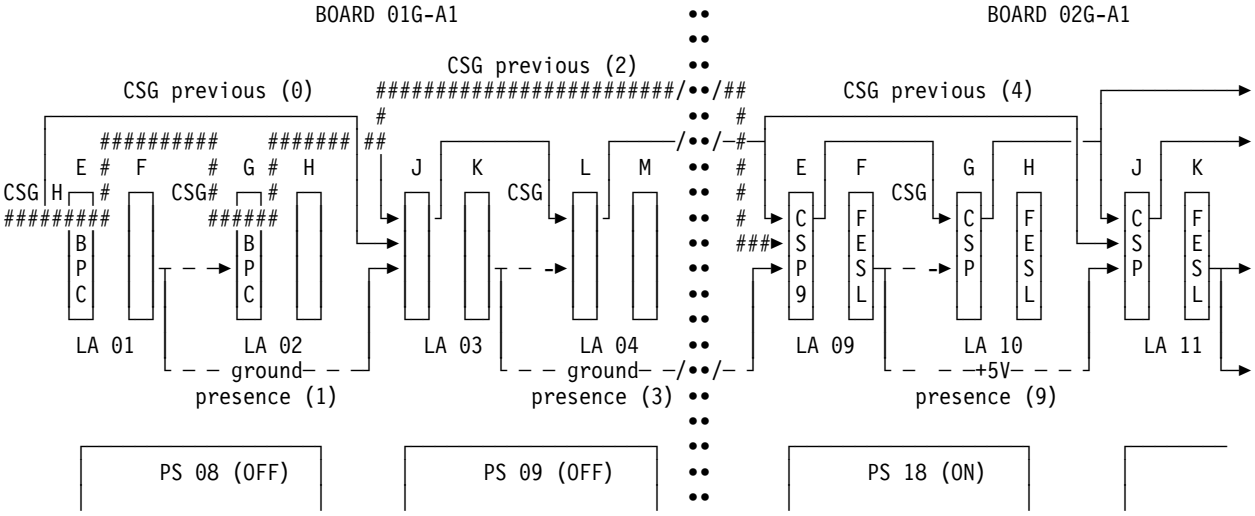
* = Can be an FESL, FESH, or EAC card.

CSG path defined by the bypass mechanism for this example of configuration

C - If two consecutive PSs are OFF (08 and 09 in the drawing):

1. BPC cards in position LA01 and LA02 ===> **mandatory**

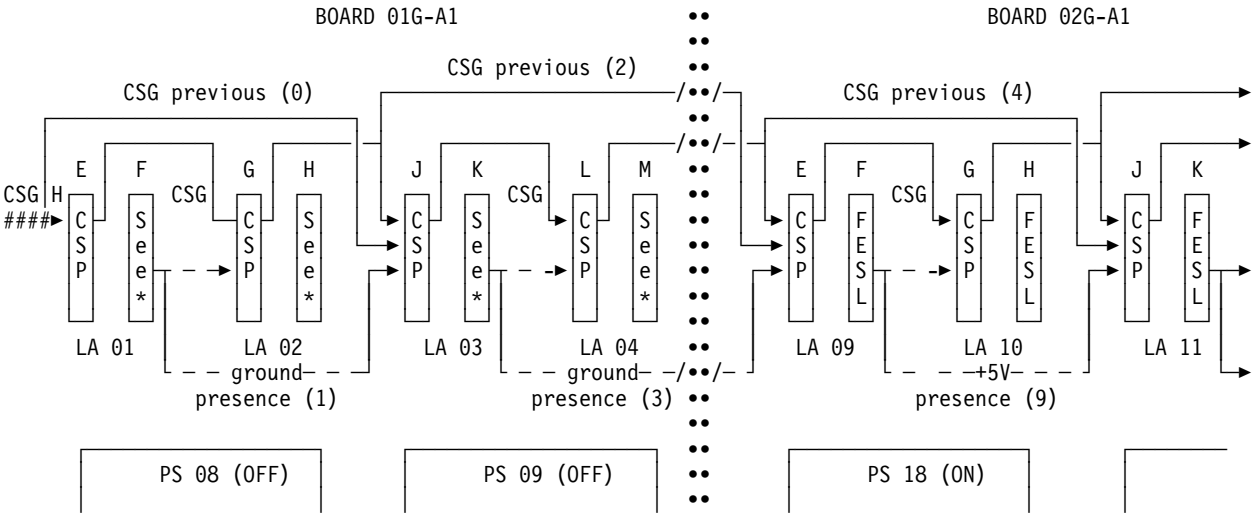
   - 'CSG' propagation is ensured by BPC cards in positions 1 and 2. Then, because 'presence (3)' is grounded, CSG propagation is ensured by 'CSG previous (2)' line to the CSP9.



\# CSG path defined by the bypass mechanism for this example of configuration

2. LA cards in positions LA01 and LA02 ===> **not allowed**

   - 'CSG' propagation is not ensured by the CSP cards because they are powered OFF. Thus, the 'CSG' line is broken.

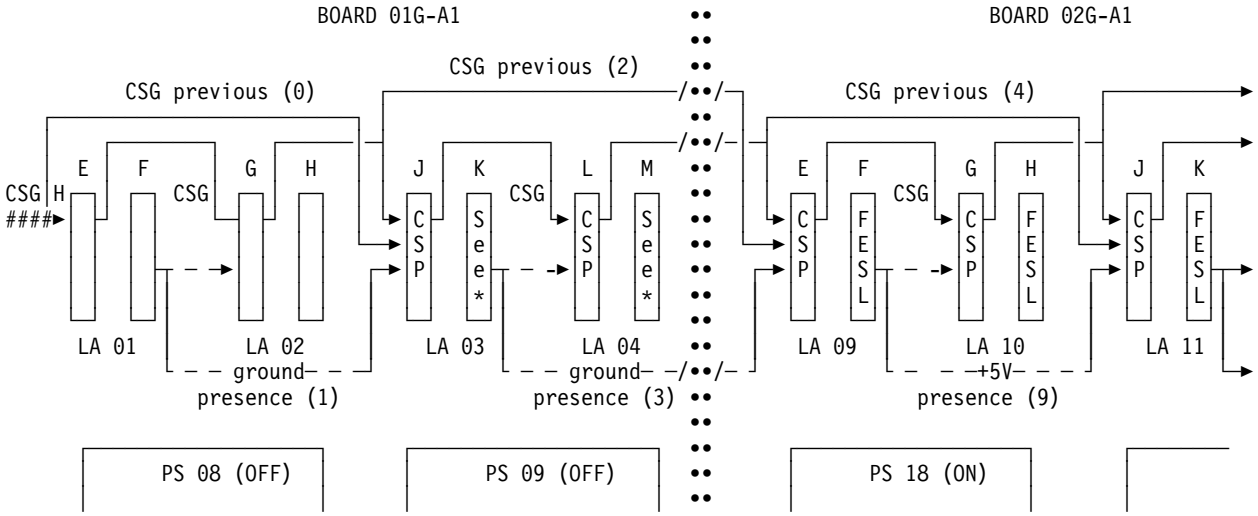


* = Can be an FESL, FESH, or EAC card.

\# CSG path defined by the bypass mechanism for this example of configuration

3. No LA or BPC cards in positions LA01 and LA02 ===> **not allowed**

   - 'CSG' propagation is not ensured because there are no cards in positions 01 and 02. Thus, the 'CSG' line is broken.

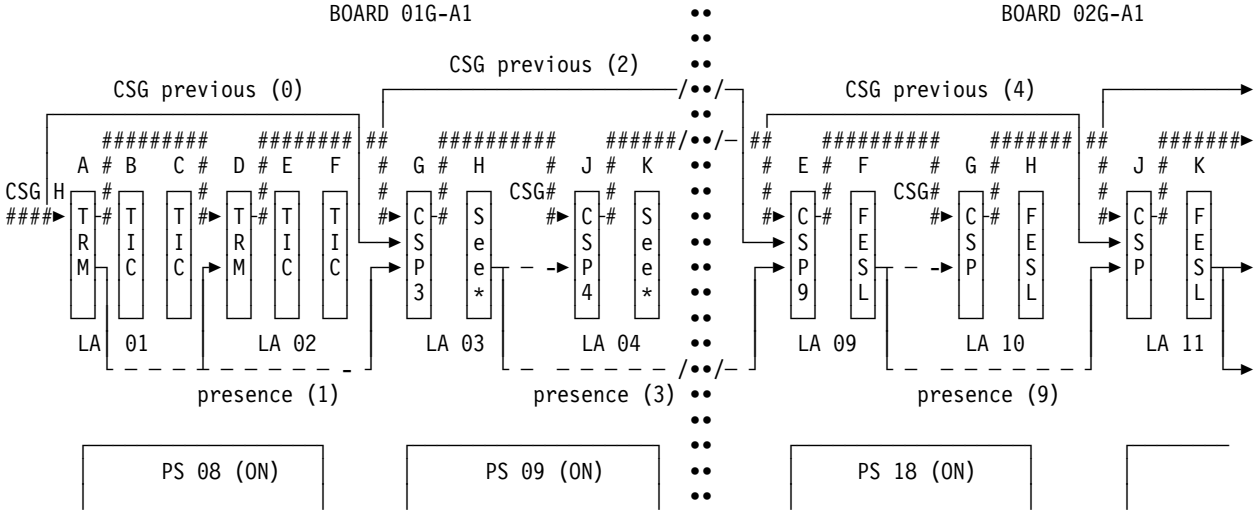


* = Can be an FESL, FESH, or EAC card.

\# CSG path defined by the bypass mechanism for this example of configuration

TSST Board

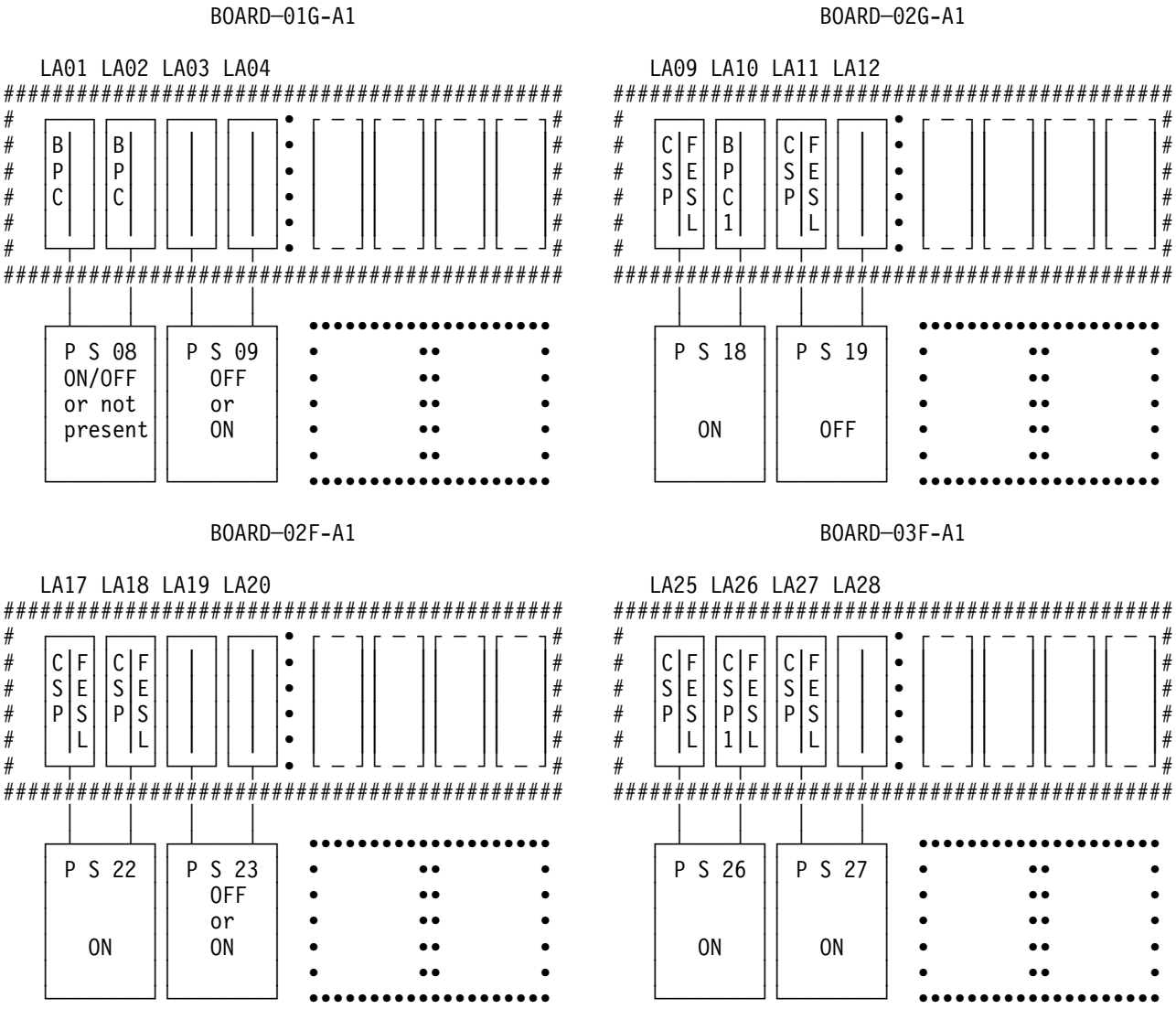
The bypass mechanism is the same as for the TSSB board, but a BPC2 card is used in place of a BPC1 card.



* = Can be an FESL, FESH, or EAC card.

\# CSG path defined by the bypass mechanism for this example of configuration

Example of Valid Configuration for Adapter Bus 1



- LA01 and 02 ===> BPC cards are needed in positions 1 and 2 because there are no scanners in positions 3 and 4 whatever the status of PS 8 and 9.
- LA03 and LA04 ===> No CSP or BPC1 cards are needed in those positions, whatever the status of PS 9.
- LA10 ===> A BPC card is needed because PS 18 is ON.
- LA12 ===> The BPC card is not needed because PS 19 is OFF.
- LA11 and LA12 ===> CSP cards can be present or not because PS 19 is OFF.
- LA28 ===> The BPC card is not needed because LA27 is the last adapter of this bus.
- LA03,04,19 and 20 ===> No BPC cards are needed in those positions whatever the status of PS 9 and 23.
- LA09,17 and 25 ===> Scanners are needed because they are fitted in odd positions and the corresponding PSs are ON.

- PS 18,19,22,23 ===> One out of two PSs can be OFF without using any BPC card (PS 18 ON, 19 OFF, 22 ON, 23 OFF).

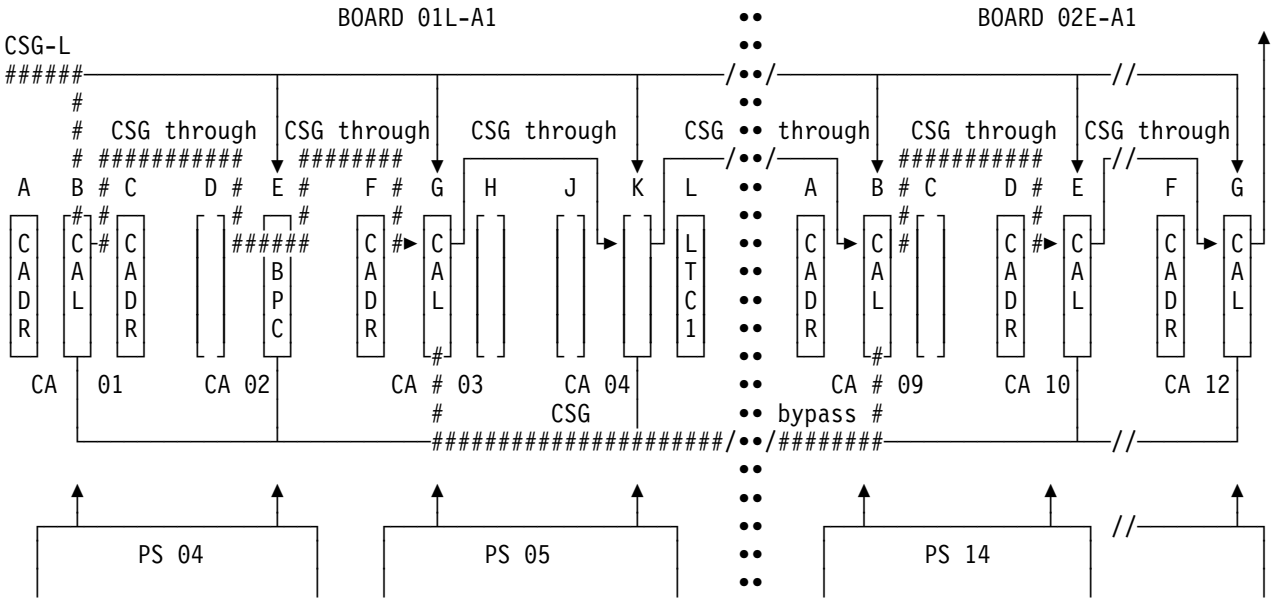
Bypass Mechanism for CAs

- The bypass mechanism is under MOSS and NCP control through the CDF (At IPL time or by a 'shut-down' command).
- The MOSS tells the CAs what the adapter configuration is on the bus (each CA must know if the preceding and the next adapters are present or not).
- Two chains are involved is this mechanism :
  - Cycle Steal Grant (CSG)
  - Autoselection chain.

Adapter Plugging Rules

1. CAs with TPS:
   a. CA cards can be plugged only in the odd positions, and a BPC card must be plugged in the even position.
2. All CAs:
   a. PSs feeding the missing CAs can be ON or OFF.

Cycle Steal Grant (CSG) Scenario for CAs



CSG path defined by the bypass mechanism for this example of configuration

As an answer to 'CSR' from any CA, the CCU raises 'CSG-L' line to the CAs.

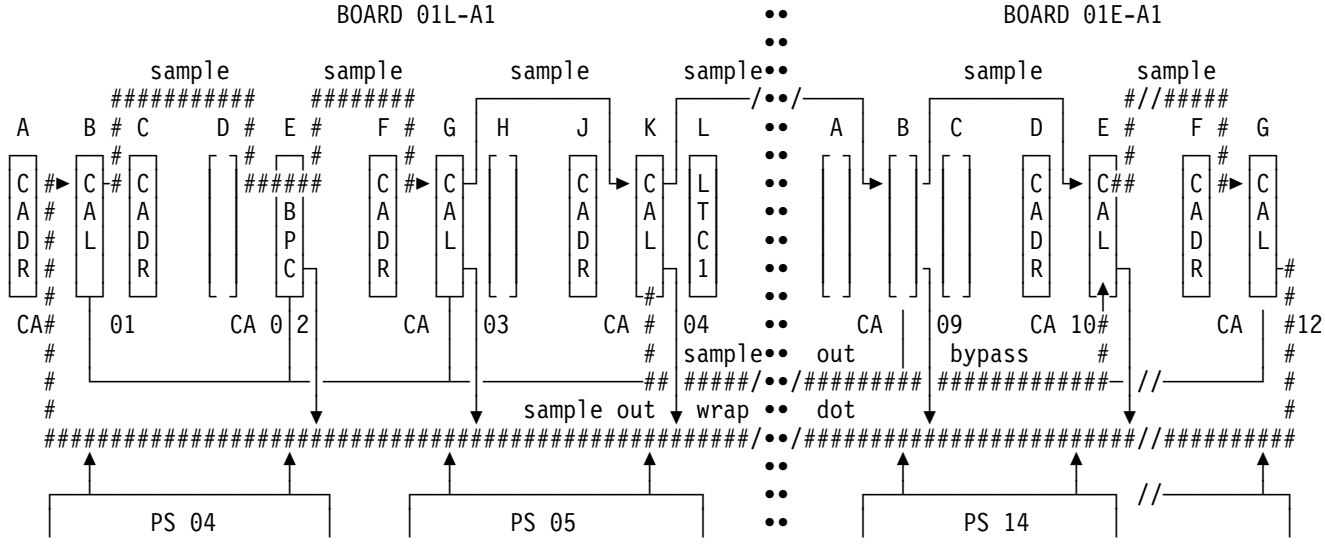
This line is propagated as follows:

- INPUT:
  - The first CA in the chain is looking at 'CSG-L' from the CCU.
  - Other CAs are looking at:
    - 'CSG-through' line if the previous CA is in the chain.
    - 'CSG-bypass' line if the previous CA is not in the chain.
- OUTPUT:
  - The CA which has raised 'CSR' (CA10 in the drawing) keeps the 'CSG' and breaks the chain.
  - Other CAs raise:
    - 'CSG-through' if the next CA is in the chain.
    - 'CSG-bypass' if the next CA is not in the chain.

Only one CA can be looking at 'CSG-bypass' and one CA only can raise 'CSG-bypass', the consequence is that only one CA or group of consecutive CAs can be missing on the bus.

If a CA is TPS (CA01 in the drawing), the next CA must be replaced by a BPC card to propagate the 'CSG-through' line.

Autoselection Scenario for CAs



CSG path defined by the bypass mechanism for this example of configuration

As an answer to 'level 3' interrupts from any CA, the CCU issues an IOH X'0F' to the bus.

There is always one CA initially selected in the chain (CA04 in the drawing).

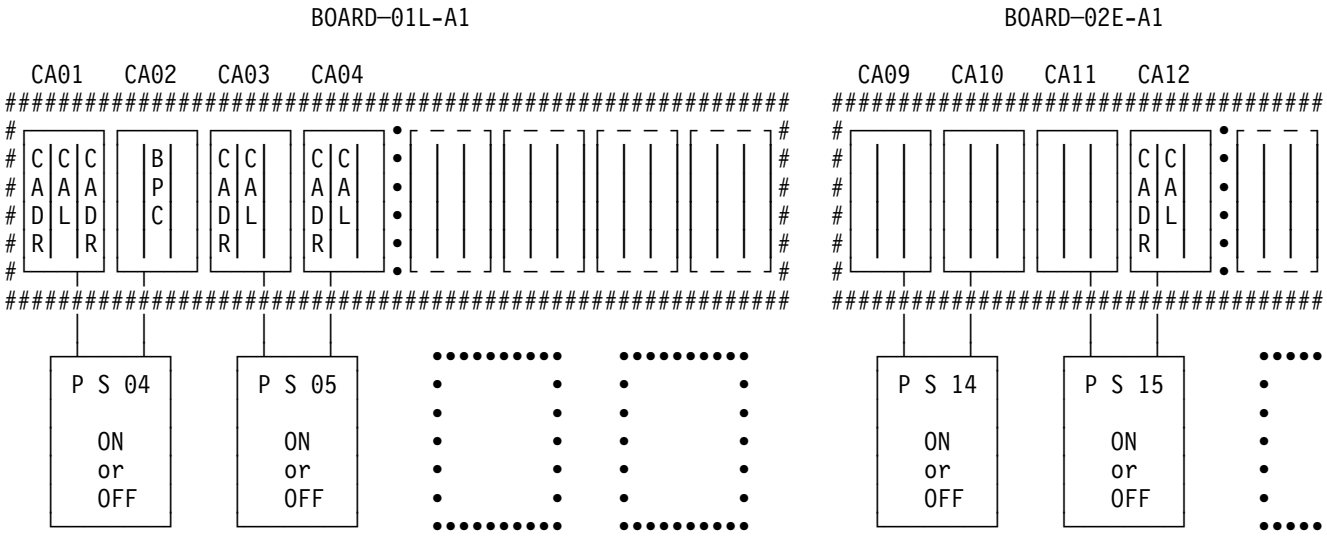
This IOH starts the propagation of the 'sample' line from the initially selected CA as follows:

- INPUT:
  - The first CA on the bus is looking at 'sample out wrap dot' from the last CA.
  - Other CAs are looking at:
    - 'Sample' line if the previous CA is in the chain.
    - 'Sample-bypass' line if the previous CA is not in the chain.
- OUTPUT:
  - The CA to be selected keeps the 'sample' and breaks the chain (CA03 in the drawing).
  - The last CA on the bus raises 'sample out wrap dot'.
  - Other CAs raise:
    - 'Sample' if the next CA is in the chain.
    - 'Sample out-bypass' if the next CA is not in the chain.

One CA only can be looking at the 'sample-bypass' line and one CA only can raise 'sample-bypass', the consequence is that only one CA or group of consecutive CAs can be missing on the bus.

If a CA is TPS (CA01 in the drawing), the next CA must be replaced by a BPC card to propagate the 'sample' line.

Example of Valid Configuration for Adapter Bus 2



You can have more than one adapter missing on the bus if they are consecutive; in this case, no BPC cards are needed.

- CA01 and 02 ===> As CA01 is TPS, there is no adapter in position 2 and a BPC card is needed in position 2.
- CA09, CA10 and CA11 ===> No BPC1 cards are needed to replace missing adapters.

Extended Troubleshooting: Adapter Bus Problem Isolation

Introduction

The following procedures are used when several or all adapters on a bus are failing. These procedures check only the 3745 side of adapter busses.
For isolation, use either:

- “Adapter Board Isolation.”
- “Checking Adapter Buses” on page 3-90.
- “IOC Bus Scoping Routine” on page 3-97.

For adapter buses swapping, see the *MIP*.

In addition the 'S' function in the CDF update can be used. See the *Service Functions.*

Adapter Board Isolation

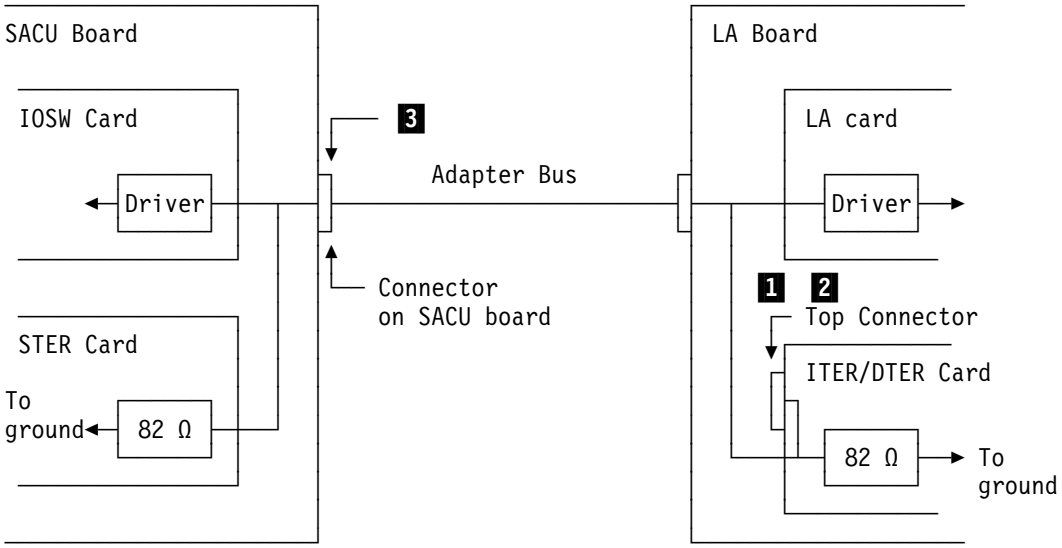
If there is more than one adapter board failing, move the ITER terminator card from board to board, up to the 3745 LA or CA board .

Run the diagnostics after updating the CDF. If the problem persists, resort to selective removal or replacement of the adapter cards to isolate the failure.

Checking Adapter Buses

Introduction

This procedure allows isolating short or open circuits in adapter bus circuits and terminator cards (ITER, DTER, STER).



Initial Conditions

Before starting the checks, you must:

1. Power the 3745 OFF.
2. Unplug all the adapter cards, and the LTC1 and LTC2 cards on the CA board(s).

Procedure

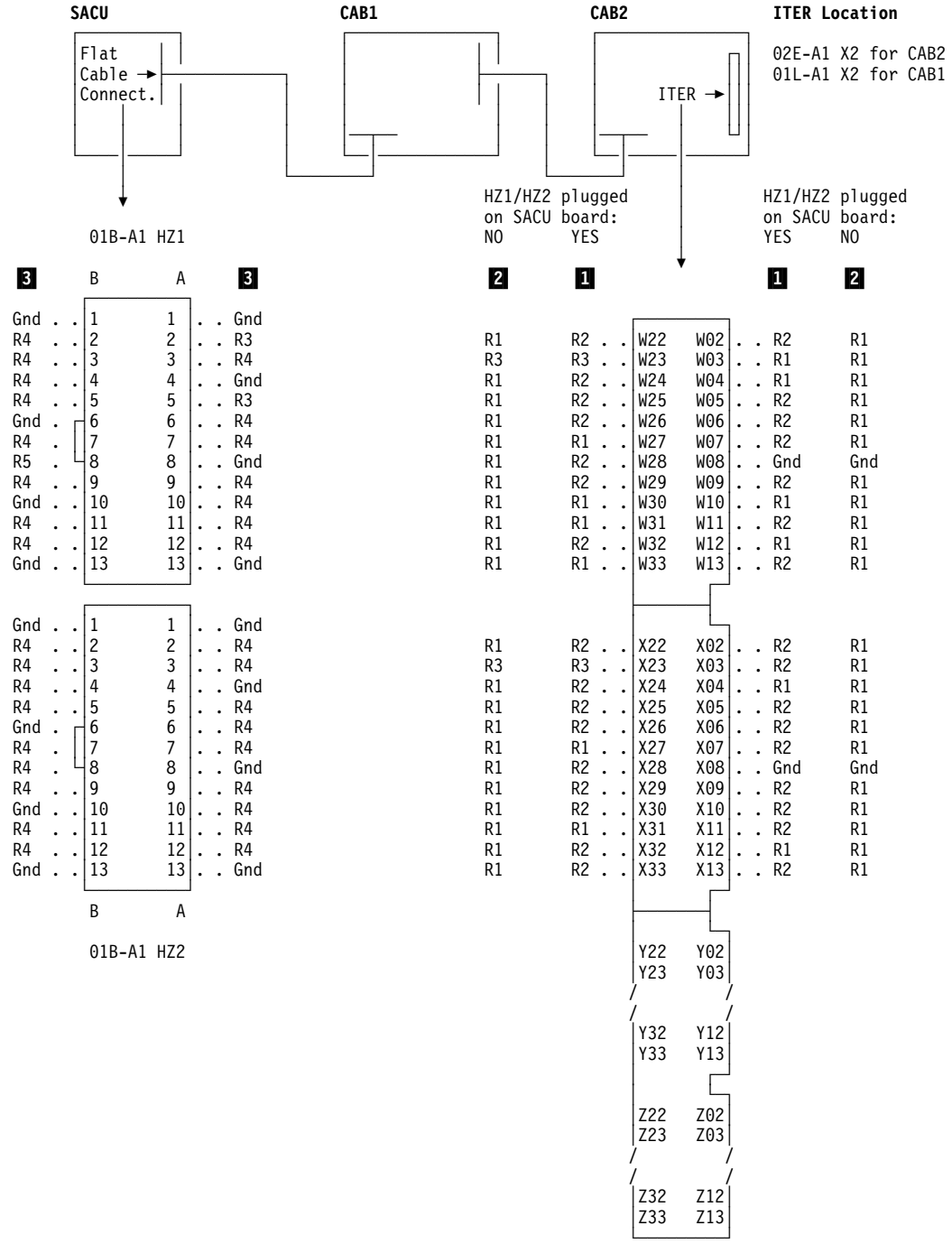
Depending on the bus to be checked, use one of the following pages to measure the resistor value.
Measurement is performed between each referenced pin and the ground pin.

1 ITER/DTER, adapter bus cables, STER continuity:
This check is performed on the ITER/DTER card top connector with all adapter cables plugged.

2 ITER/DTER and adapter bus cables check:
Same procedure as above, but the adapter bus cables are not plugged on the SACU board.

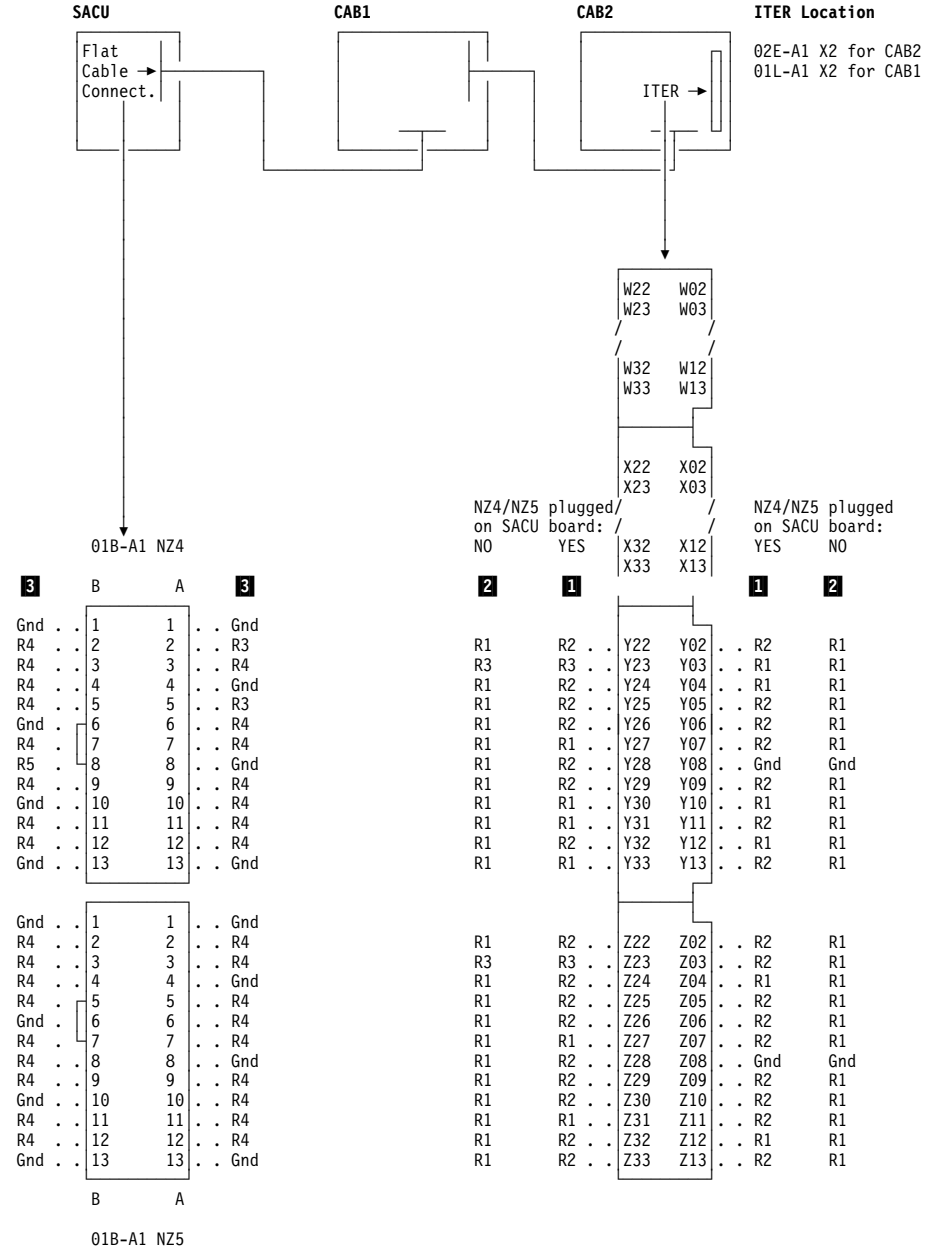
3 Adapter bus cable and ITER/DTER continuity:
This check is performed on the connector of the adapter bus cables on the SACU board side (the adapter bus cables are unplugged from the SACU board).

IOC Adapter Bus 2



Gnd= Ground
R1 = 78 to 86 Ω.
R2 = 39 to 45 Ω.
R3 = Open circuit.
R4 = 78 to 86 Ω with the ITER plugged or, open circuit when the ITER is removed.
(One adapter card must be plugged in the first CAB position.)
R5 = 39 to 45 Ω with the ITER plugged or, 78 to 86 Ω when the ITER is removed.

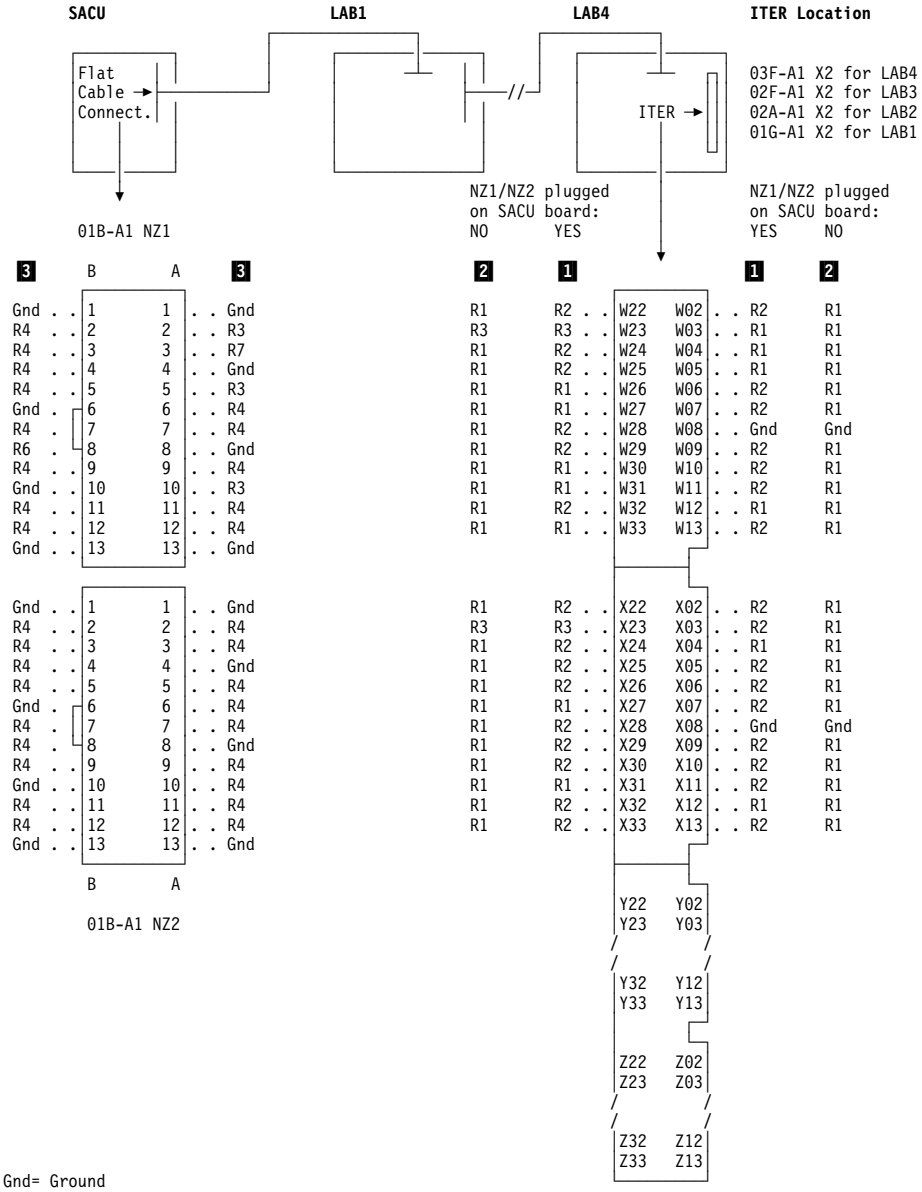
IOC Adapter Bus 3



Gnd= Ground
R1 = 78 to 86 Ω.
R2 = 39 to 45 Ω.
R3 = Open circuit.
R4 = 78 to 86 Ω with the ITER plugged or, open circuit when the ITER is removed.
(One adapter card must be plugged in the first CAB position.)
R5 = 39 to 45 Ω with the ITER plugged or, 78 to 86 Ω when the ITER is removed.

IOC Adapter Bus 4: If you are working on a 3745 Model 21A-61A connected to a 3746 Model 900, unplug the IOC bus coming from the 3746-900 and plug an ITER terminator were the IOC bus cable was plugged. For cable locations see figure below.

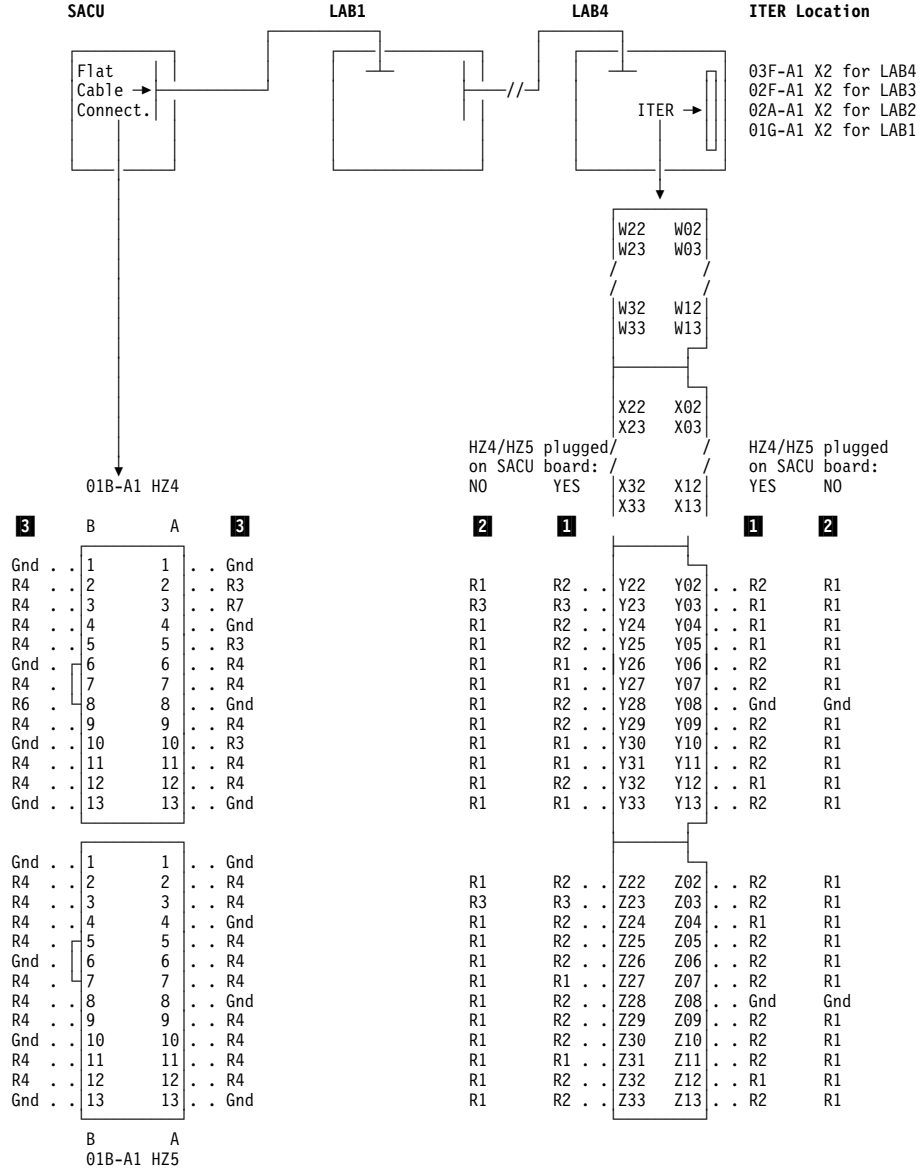
ITER terminator card (PN 66X0521) is available with the shipping group material.



Gnd= Ground
R1 = 78 to 86 Ω.
R2 = 39 to 45 Ω.
R3 = Open circuit.
R4 = 78 to 86 Ω with the ITER plugged or, open circuit when the ITER is removed.
(One adapter card must be plugged in the first LAB position.)
R5 = 39 to 45 Ω with the ITER plugged or, 78 to 86 Ω when the ITER is removed.
R6 = 39 to 45 Ω with the ITER plugged or not plugged. ER is removed.
(One adapter card must be plugged in the first LAB position.)
R7 = 25 to 31 Ω with the ITER plugged or, 39 to 45 Ω when the ITER is removed.
(One adapter card must be plugged in the first LAB position.)

IOC Adapter Bus 1: If you are working on a 3745 Model 21A-61A connected to a 3746 Model 900, unplug the IOC bus coming from the 3746-900 and plug an ITER terminator were the IOC bus cable was plugged. For cable locations see figure below.

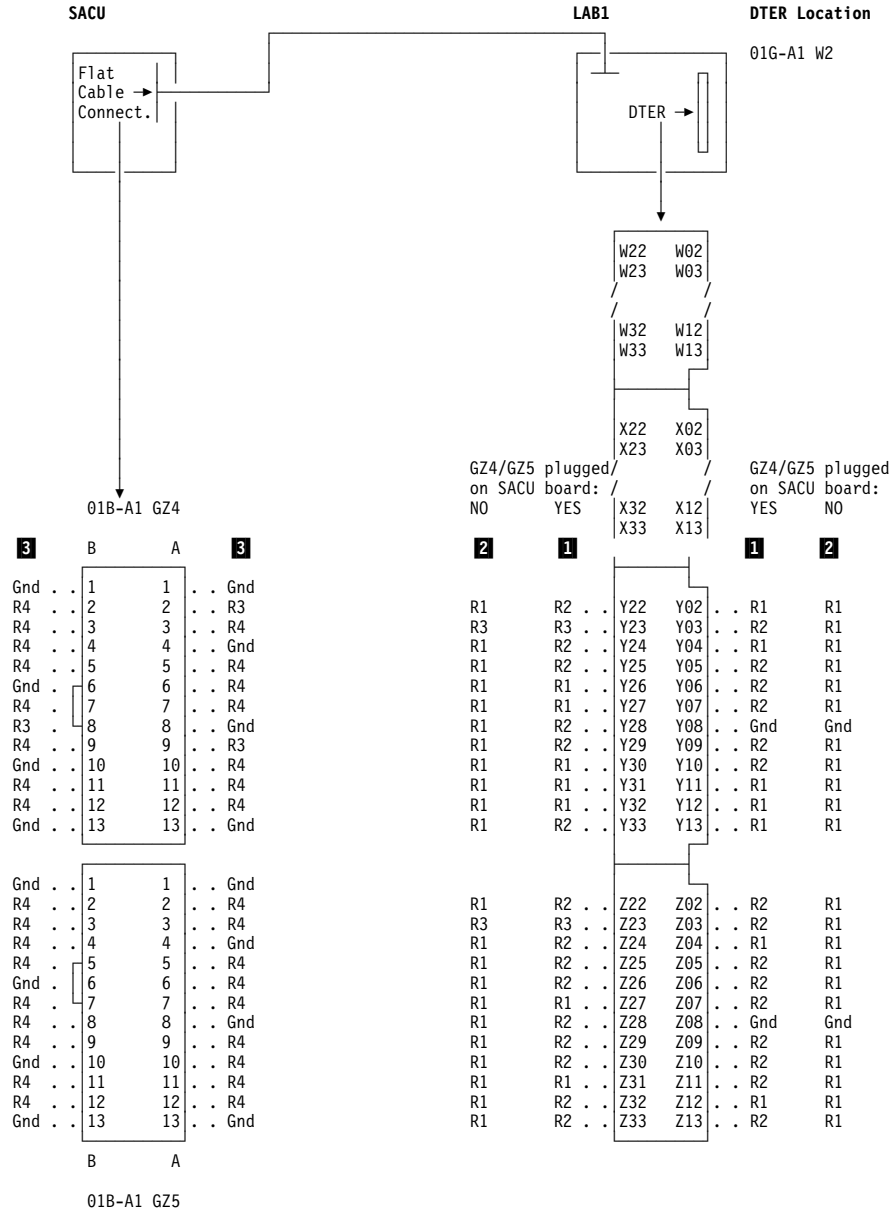
ITER terninator card (PN 66X0521) is available with the shipping group material.



Gnd= Ground
R1 = 78 to 86 Ω.
R2 = 39 to 45 Ω.
R3 = Open circuit.
R4 = 78 to 86 Ω with the ITER plugged or, open circuit when the ITER is removed.
(One adapter card must be plugged in the first LAB position.)
R5 = 39 to 45 Ω with the ITER plugged or, 78 to 86 Ω when the ITER is removed.
R6 = 39 to 45 Ω with the ITER plugged or not plugged.
(One adapter card must be plugged in the first LAB position.)
R7 = 25 to 31 Ω with the ITER plugged or, 39 to 45 Ω when the ITER is removed.
(One adapter card must be plugged in the first LAB position.)

DMA Bus 5: If you are working on a 3745 Model 21A-61A connected to a 3746 Model 900, unplug the DMA bus coming from the 3746-900 and plug an DTER terminator were the DMA bus cable was plugged. For cable locations see figure below.

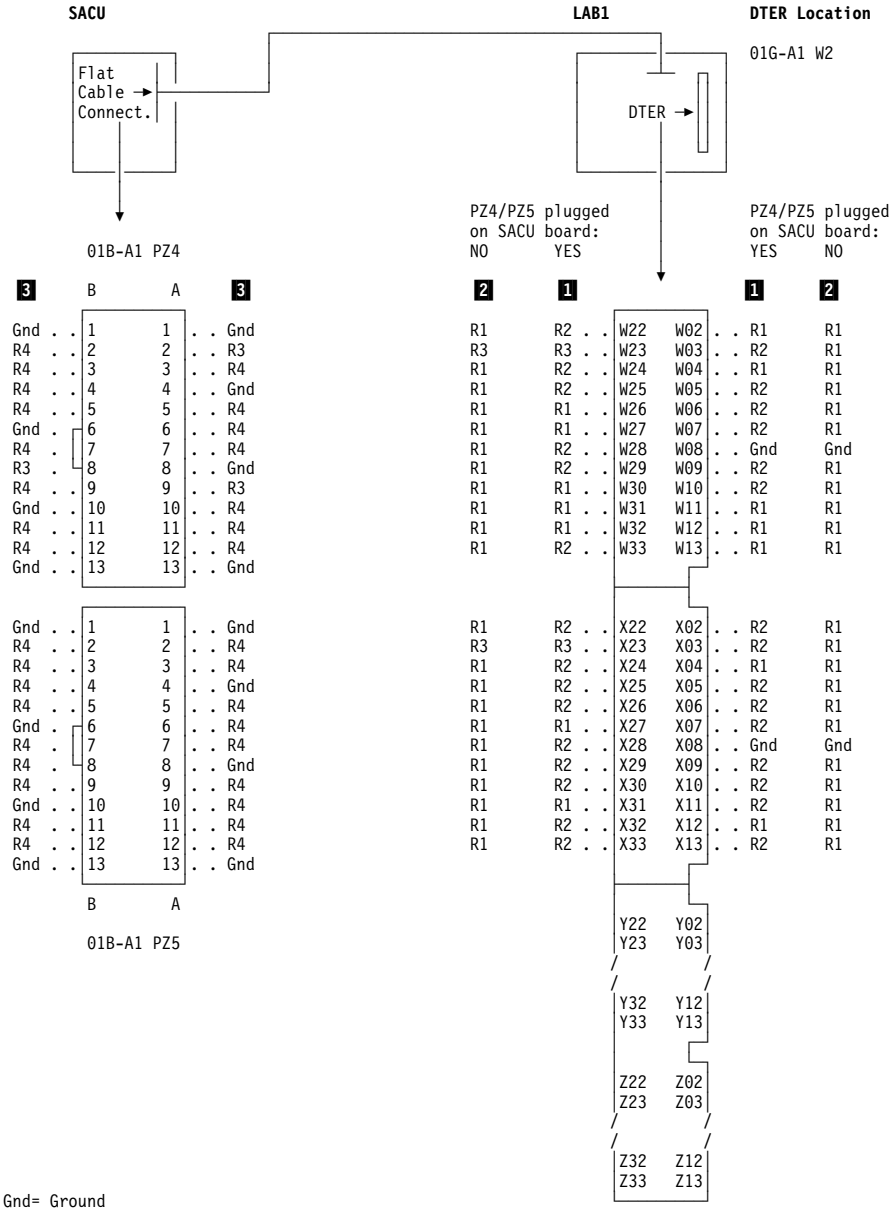
DTER terninator card (PN 66X0521) is available with the shipping group material.



Gnd= Ground
R1 = 78 to 86 Ω.
R2 = 39 to 45 Ω.
R3 = Open circuit.
R4 = 78 to 86 Ω with the DTER plugged or, open circuit when the DTER is removed.
(One adapter card must be plugged in the first LAB position)
R5 = 39 to 45 Ω with the DTER plugged or, 78 to 86 Ω when the DTER is removed.

DMA Bus 6: If you are working on a 3745 Model 21A-61A connected to a 3746 Model 900, unplug the DMA bus coming from the 3746-900 and plug an DTER terminator were the DMA bus cable was plugged. For cable locations see figure below.

DTER terninator card (PN 66X0521) is available with the shipping group material.



IOC Bus Scoping Routine

Introduction

The purpose of the PIO scoping routine is to allow scoping of the PIO tags and data bus for the four IOC buses.
The following adapters can be exercised using MIOH commands sent from the MOSS:

- CAs
- LAs

If you are working on a 3745 Model 21A-61A connected to a 3746 Model 900, unplug the IOC and DMA buses coming from the 3746-900 and plug ITER and DTER terminators were the IOC and DMA bus cables were plugged.

ITER and DTER terninator cards (PN 66X0521) are available with the shipping group material.

How to Start the Routine

1. Start the routine by calling the routine WA01.
   DIAG==> WA01
2. Put in the ADP field the adapter bus number (1 to 4) on which scoping is planned.
   IOC adapter bus = 1
   IOC adapter bus = 2
   IOC adapter bus = 3
   IOC adapter bus = 4

   ADP ≠ ==> 1 (for IOC adapter bus 1)
3. Put the adapter number in the LINE field

   LINE==> 2 (for adapter 02)
4. The screen should look like this:

   DIAG==> WA01 ADP ==> 1 LINE==> 2 OPT==> N
5. Then press SEND.

   A check is made to see if the selected IOC bus can be used, (checking of bits: enable, present, available, concurrent).

   If the conditions are not satisfied for the selection, a message:

   'ADAPTER NOT IN CDF', or
   'ADAPTER NOT INSTALLED', or
   'INVALID REQUEST' is displayed.

   If the inputs are correct, a message is then returned to the operator:

   'xx[1] 02[2] SELECTED - ENTER : Rooccdddd'

   [1] = xx may be TSS, HPTSS, TRSS, ESS, or CA
   [2] = 02 is the adapter number (1 to 32)

The first part of the message allows the operator to check that the right adapter is selected. The second part of the message prompts the operator to send the three parameters which define the MIOH operation:

Adapter Selection

```
ENTER: 'Rooccdddd' THEN PRESS SEND.
  R    : is mandatory
  oo   : defines the OPTION (hexadecimal)
  cc   : defines the COMMAND (hexadecimal)
  dddd : defines the DATA to/from adapter (hexadecimal)
```

These parameters are checked:
If the inputs are valid the MIOH operation is started according to the specified parameters.
If the inputs are not valid, a message is then returned to the operator :
'INVALID INPUTS - ENTER : Rooccdddd'

Parameter Description

Option 'oo': Four options are possible :

1. 'oo'='01' The requested MIOH is executed **only once**. The '01' option may be repeated as long as needed. A message is sent to the operator after each MIOH :
   'ENTER : R for another cycle or REE to leave'

   Therefore if the answer is 'R', the operator is prompted for another MIOH with the selected adapter:
   'ENTER: 'Rooccdddd' THEN PRESS SEND'

   This allows to perform a write followed by a read operation, because inputs may be different.

2. 'oo'='02' The requested MIOH is executed and **loops** on this MIOH until an error is found. The error is reported only once via a RAC . To continue 'G' (for go) has to be typed, the routine then loops indefinitely until the Power On Reset key is pressed or another error is found.

3. 'oo'='03' This option is identical to option '02', except that **no checking** is made. This allows looping about four times faster, and therefore easier scoping. The routine loops indefinitely until the Power On Reset key is pressed.

4. 'oo'='04' This option is **reserved for the TSS, HPTSS, and ESS,** and is used to scope Adapter Level 1 and Level 2 interrupt requests to the CCU. Commands 10 to 21 can be used only with option 04.
   Because this option needs a Power On Reset on the CSP, each operation lasts about 10 seconds.

   For option 04 at TD time on the IOC bus, byte 1 bit 5 will be ON for level 1 interrupts and byte 0 bit 1 ON for level 2.

COMMAND (or MIOH operation) 'cc' Since the purpose of the scoping routine is only to activate the bus lines and the tag lines on the IOC bus, it is only necessary to be able to execute one type of write operation and the corresponding read operation to check the data previously written.
For this reason the command codes are limited to:

1. 'cc'='01' Defines a write operation to any adapter type. TA values are automatically generated, according to the adapter type and the write operation defined for this adapter.
2. 'cc'='02' Defines a read operation from any adapter type. TA values are automatically generated, according to the adapter type and the read operation defined for this adapter.

   In loop mode, (OPTION 'oo'='02' or '03'), when a read operation is requested, the first operation is a write in order to store the data in one register of the addressed adapter. All subsequent operations are read operations in order to recall the data from the register previously written.
3. 'cc'='10' Special for the TSS, HPTSS, and ESS, requests to the selected adapter used with option 04 only, to reset the level 1 interrupt to the CCU. This level 1 is then tested at CCU level and a message:
   'LEVEL 1 INTRPT IS RESET' is displayed.
4. 'cc'='11' Special for the TSS, HPTSS, and ESS, used with option 04 only, requests to the selected adapter to set the level 1 interrupt to the CCU. This level 1 is then tested at CCU level and a message:
   'LEVEL 1 INTRPT IS SET' is displayed.
5. 'cc'='20' Special for the TSS, HPTSS, and ESS, used with option 04 only, requests to the selected adapter to reset the level 2 interrupt to the CCU. This level 2 is then tested at CCU level and a message:
   'LEVEL 2 INTRPT IS RESET' is displayed.
6. 'cc'='21' Special for the TSS, HPTSS, and ESS, used with option 04 only, requests to the selected adapter to set the level 2 interrupt to the CCU. This level 2 is then tested at CCU level and a message:
   'LEVEL 2 INTRPT IS SET' is displayed.

DATA: 'dddd' (mandatory for any command) defines either:

- The data (TD value) send to the adapter through the IOC bus at TD time during a write operation or,
- The data (TD value) received from the adapter through the IOC bus at TD time during a read operation.

For example, data can be hexadecimal: '5555', 'AAAA', ...'

RACs Generated

When the scoping routine does not run, the following RACs are generated. These RACs must not be entered with the BRC function.
Run the corresponding adapter diagnostic.

RAC Meaning

231 Unexpected interrupt CA operation
232 Unexpected interrupt TSS operation
233 Unexpected interrupt HPTSS or ESS operation
234 Unexpected interrupt TRSS operation
235 Level 2 not set by TSS, HPTSS, or ESS
236 Level 2 not reset by TSS, HPTSS, or ESS
237 Level 1 not set by TSS, HPTSS, or ESS
238 Level 1 not reset by TSS, HPTSS, or ESS
241 Unexpected data from CA

242 Unexpected data from TSS
243 Unexpected data from HPTSS or ESS
244 Unexpected data from TRSS

ERC Meaning

The error reference code displayed with the RAC has the following meaning:

0001 Error during selection
0002 Error during write (01 operation)
0003 Error during read (02 operation)
0004 Error during first write (02 requested)

Error Bit (ERR)

The error bit pattern displayed with the RAC has the following meaning:

For RACs 231 to 238:

Byte 0

Bit 0 = CA to CCU level 1
Bit 1 = CA to CCU level 3
Bit 2 = CA to MOSS level 1
Bit 3 = CA to MOSS level 4
Bit 4 = TSS, HPTSS, or ESS to CCU level 1
Bit 5 = TSS, HPTSS, or ESS to CCU level 2
Bit 6 = Not used
Bit 7 = TSS, HPTSS, or ESS to MOSS level 4

Byte 1

Bit 0 = MOSS level 1 IOC time out
Bit 1 = MOSS level 1 IOC invalid CCW
Bit 2 = MOSS level 1 IOC other error
Bit 3 = CCU level 1 SAR parity error
Bit 4 = CCU level 1 IOC time out
Bit 5 = CCU level 1 IOC invalid CCW
Bit 6 = CCU level 1 IOC other error
Bit 7 = CA to MOSS level 1 CAIPL

For RACs 241 to 244:

ERR bits = Data received from the adapter

Examples of Scoping Routine on Bus Terminator

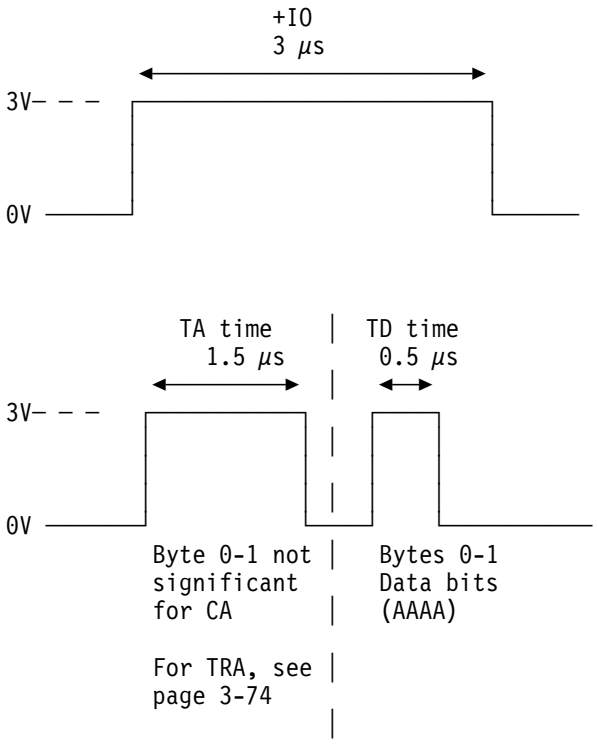
A good quality oscilloscope is required (high luminosity).

For pin locations, see “Bus Terminator (ITER) Connector Pin Assignments” on page 3-103.

Channel Adapter or Token-ring Adapter: CA 03 on adapter bus 2, or TRA 1 on adapter bus 1
Options: 02 or 03
Command: 02 (read)
Data: 'AAAA'

Oscilloscope:
Sync: +IO line
Calibration: 0.5 μs

+IO cycle option 2 = 40 ms
+IO cycle option 3 = 13 ms

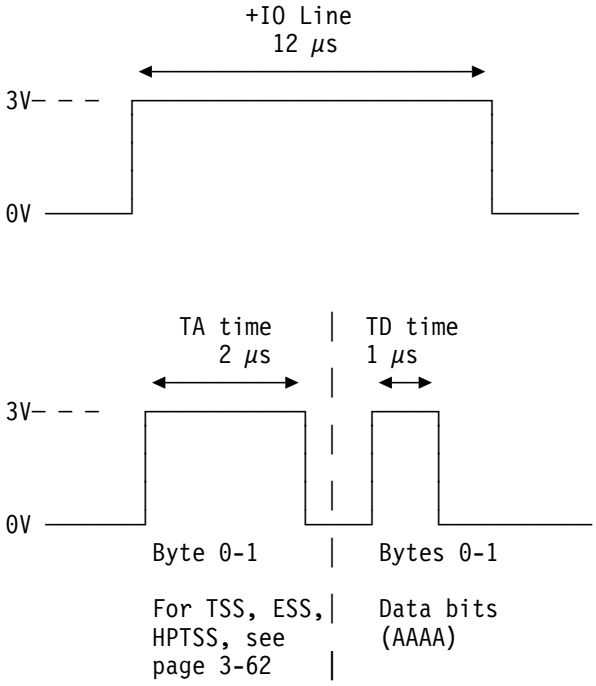


Typical Voltage Operating Ranges: Pulse amplitude = 3 to 5 volts
Ringing = less than 500 mV peak to peak
Rise time = 15 ns
Fall time = 10 ns

LSS or HSS/ELA: LSS 09 on adapter bus 2, or HSS/ELA 04 on adapter bus 1
Options: 02 or 03
Command: 02 (read)
Data: 'AAAA'

Oscilloscope:
Sync: +IO line
Calibration: 2 μs

+IO cycle option 2 = 40 ms
+IO cycle option 3 = 13 ms



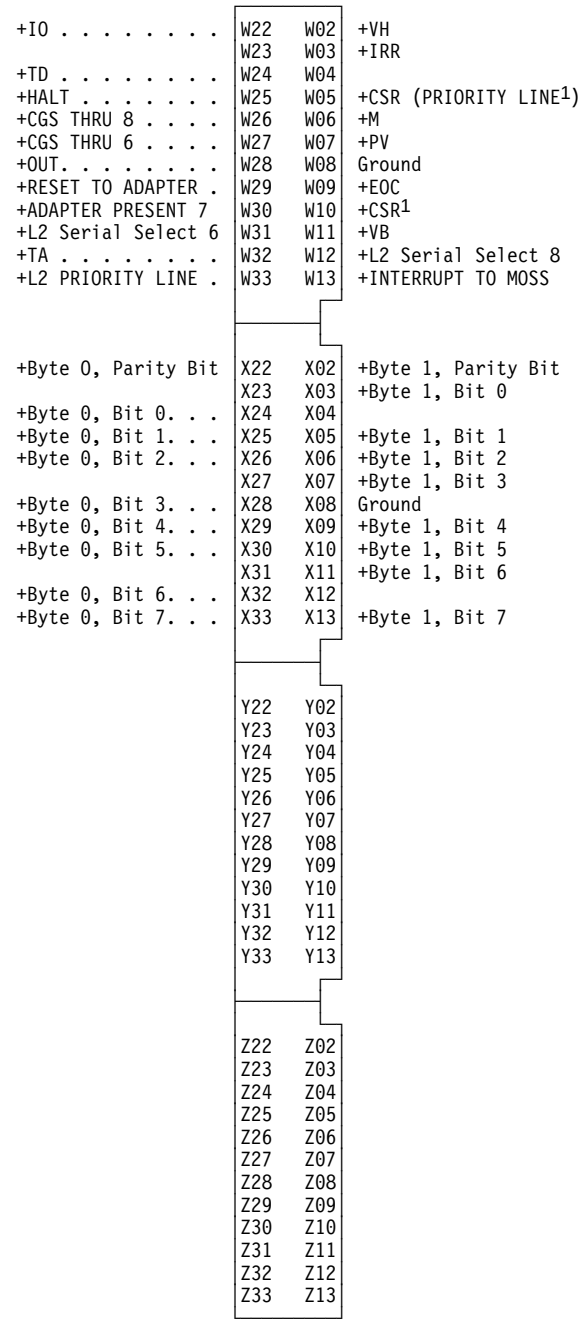

```
At TA time, for LSS 09 (TSS):
 Byte 0 bits P, 3, and 6 are ON
 Byte 1 bits P, 4, and 7 are ON

At TA time, for HSS/ELA 04 (HPTSS/ESS):
 Byte 0 bits P, 2, and 7 are ON
 Byte 1 bits P, 4, and 7 are ON
```

Typical Voltage Operating Ranges: Pulse amplitude = 3 to 5 volts
Ringing = less than 500 mV peak to peak
Rise time = 15 ns
Fall time = 10 ns

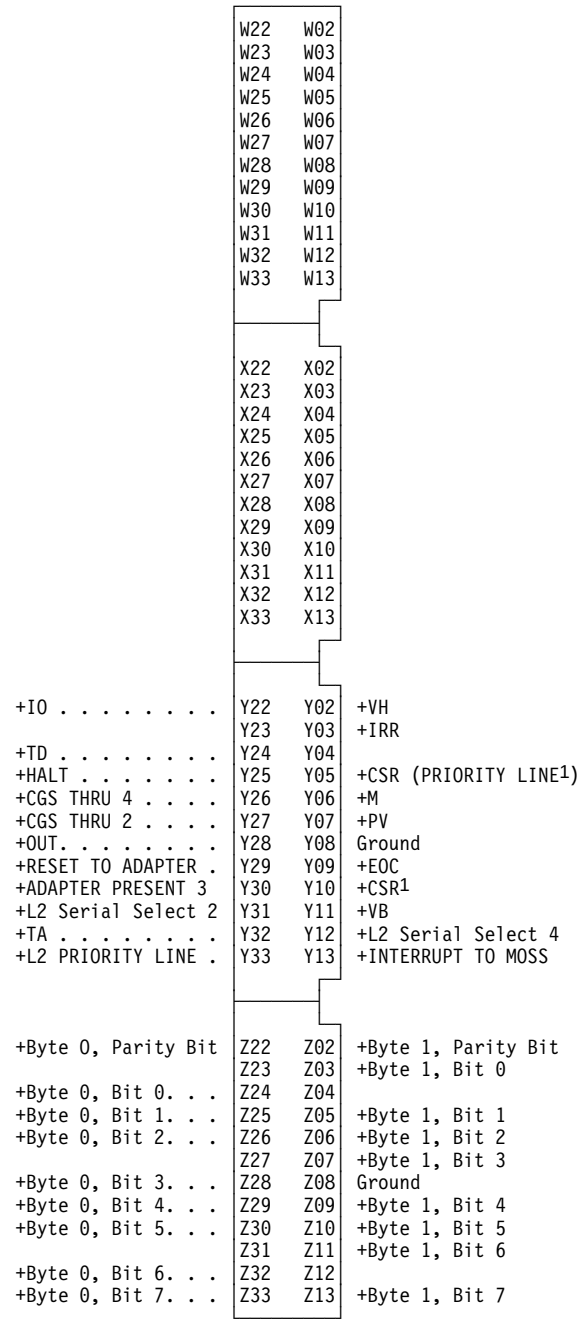
Bus Terminator (ITER) Connector Pin Assignments

Adapter Bus 2 or 4:



1 = For LA only

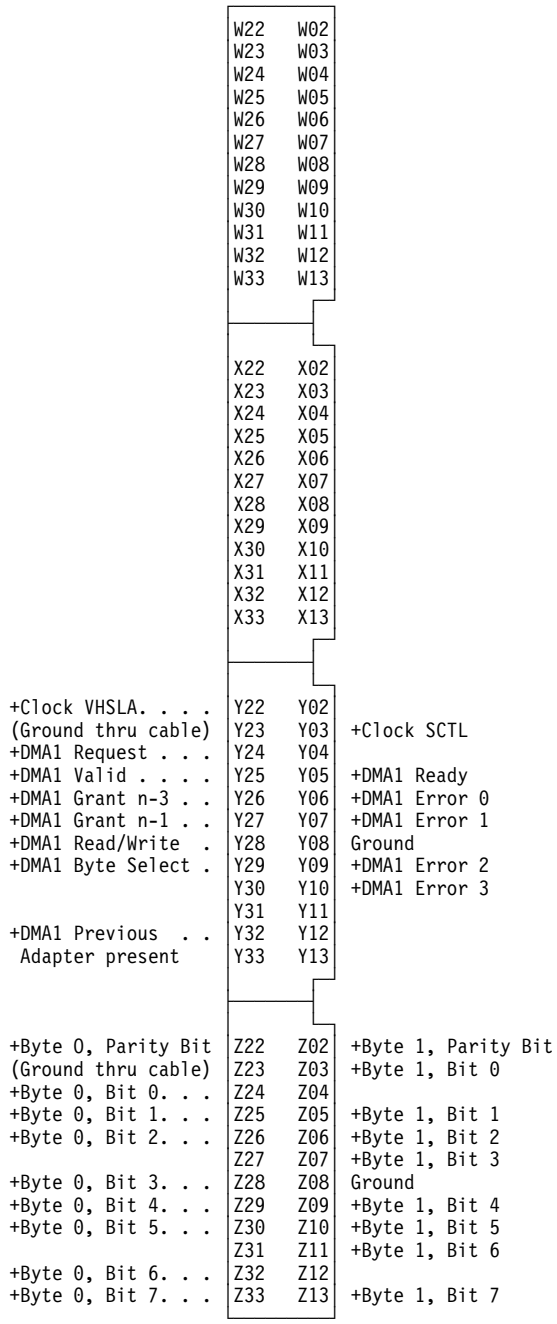
Adapter Bus 1 or 3



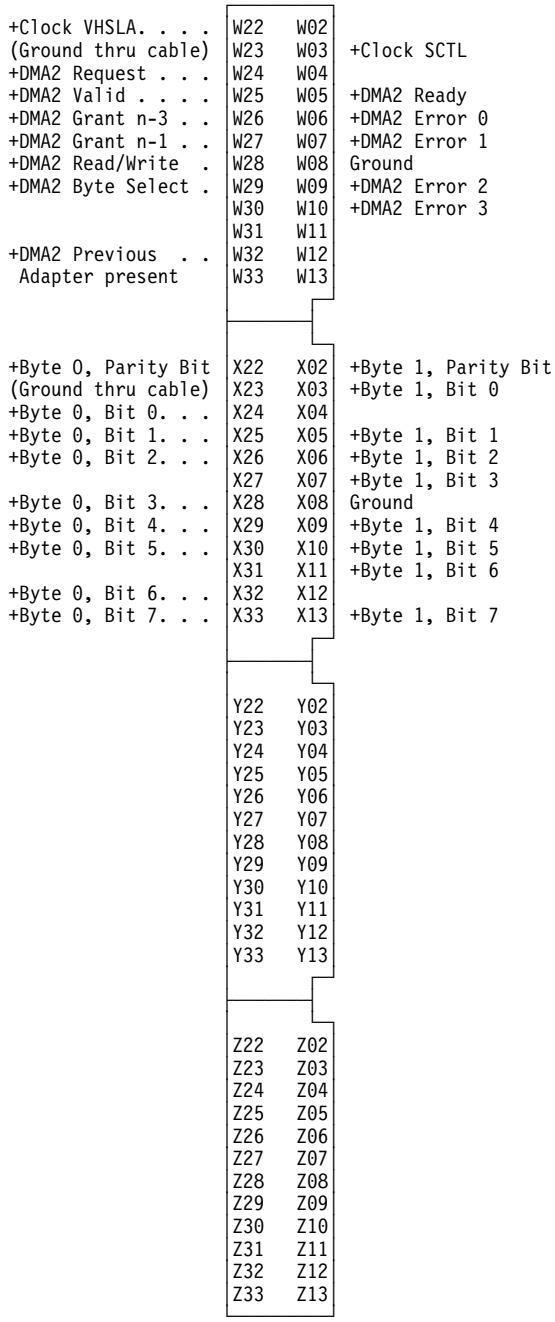
1 = For LA only

DMA Terminator (DTER) Connector Pin Assignments

DMA Bus 5:



DMA Bus 6:


+Clock VHSLA. . . . W22 W02
(Ground thru cable) W23 W03 +Clock SCTL
+DMA2 Request . . . W24 W04
+DMA2 Valid . . . . W25 W05 +DMA2 Ready
+DMA2 Grant n-3 . . W26 W06 +DMA2 Error 0
+DMA2 Grant n-1 . . W27 W07 +DMA2 Error 1
+DMA2 Read/Write . W28 W08 Ground
+DMA2 Byte Select . W29 W09 +DMA2 Error 2
W30 W10 +DMA2 Error 3
W31 W11
+DMA2 Previous . . W32 W12
Adapter present W33 W13
+Byte 0, Parity Bit X22 X02 +Byte 1, Parity Bit
(Ground thru cable) X23 X03 +Byte 1, Bit 0
+Byte 0, Bit 0. . . X24 X04
+Byte 0, Bit 1. . . X25 X05 +Byte 1, Bit 1
+Byte 0, Bit 2. . . X26 X06 +Byte 1, Bit 2
X27 X07 +Byte 1, Bit 3
+Byte 0, Bit 3. . . X28 X08 Ground
+Byte 0, Bit 4. . . X29 X09 +Byte 1, Bit 4
+Byte 0, Bit 5. . . X30 X10 +Byte 1, Bit 5
X31 X11 +Byte 1, Bit 6
+Byte 0, Bit 6. . . X32 X12
+Byte 0, Bit 7. . . X33 X13 +Byte 1, Bit 7
Y22 Y02
Y23 Y03
Y24 Y04
Y25 Y05
Y26 Y06
Y27 Y07
Y28 Y08
Y29 Y09
Y30 Y10
Y31 Y11
Y32 Y12
Y33 Y13
Z22 Z02
Z23 Z03
Z24 Z04
Z25 Z05
Z26 Z06
Z27 Z07
Z28 Z08
Z29 Z09
Z30 Z10
Z31 Z11
Z32 Z12
Z33 Z13

Chapter 4. Transmission Subsystem (TSS)

3745 Data Flow

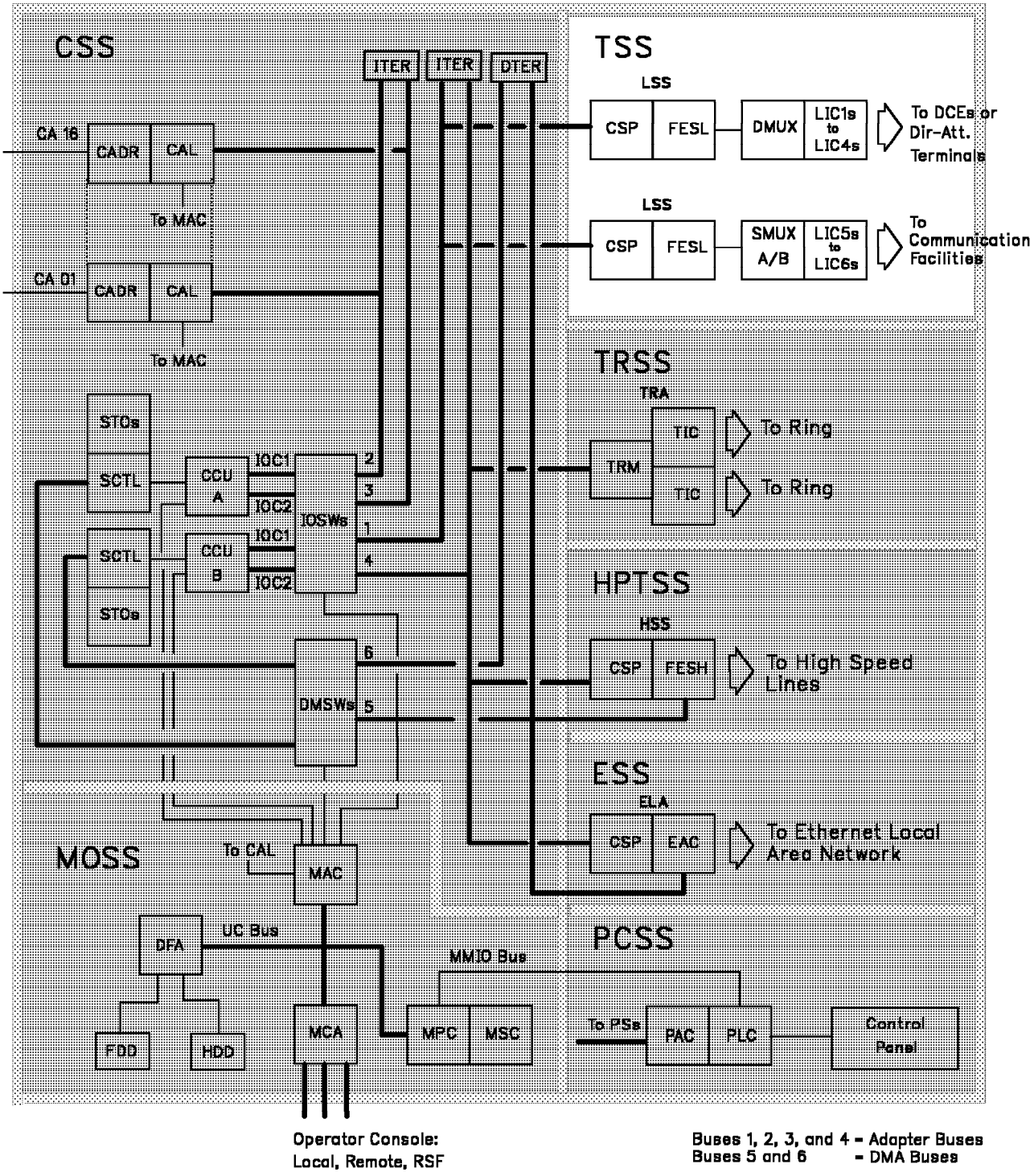
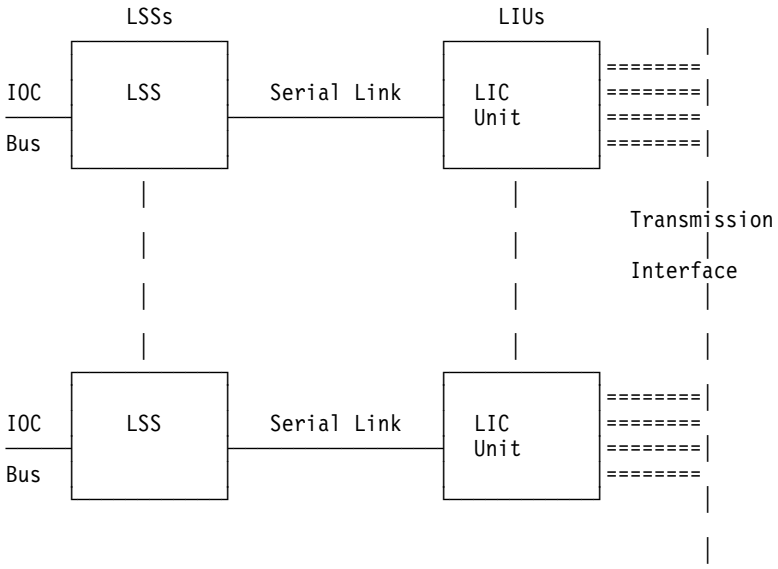


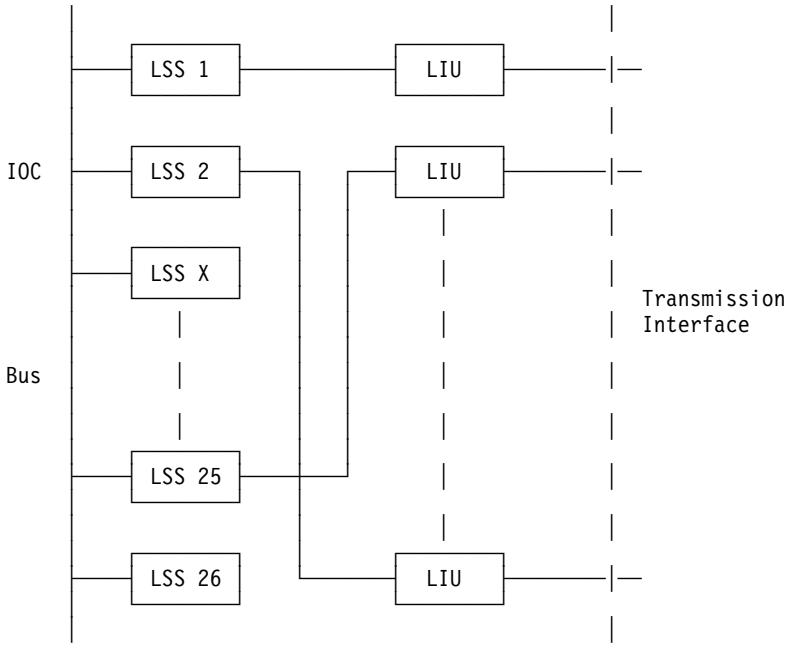
Figure 4-1. TSS in the 3745 Data Flow. For models 21A-61A, DMA and IOC buses are connected to the CBC in the 3746-900. The MCA card is replaced by the MLA card which interfaces to the MPC card through the MMIO bus. This MLA card links the MOSS to the Service Processor through a LAN.

Definitions

The TSS consists of low speed scanners (LSSs), associated to LIC units (LIUs), through serial links.



However, it is possible to connect any LIC Unit (LIU) to any Low Speed Scanner (LSS) by simply moving the Serial Link cables.

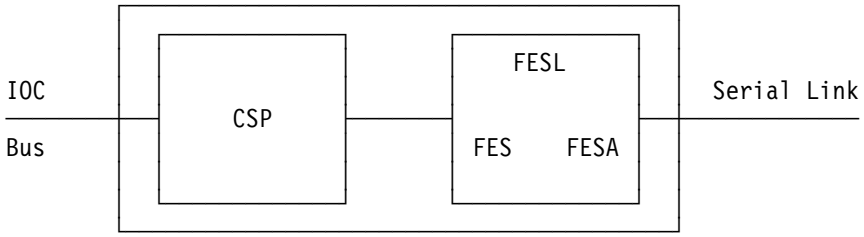


Low Speed Scanner (LSS)

Definition

A low speed scanner (LSS) consists of:

- A communication scanner processor (CSP)
- A front-end scanner Low-Speed (FESL).



Communication Scanner Processor (CSP)

The communication scanner processor (CSP):

- Supports various line protocols with partial handling of the data link control for BSC and SDLC lines

  (The microcode allows the implementation of specific customer protocols.)
- Provides character buffering and cycle steal transfer into CCU main storage
- Supports start-stop with: 8/5, 9/7, 10/7, 10/8, 11/8 bits, BSC (EBCDIC, ASCII), SDLC, DIAL, X.21 native and X.21 bis
- Controls transmission interfaces
- Handles a variable number of lines depending on the protocol and the transmission speed
- Provides four types of operating mode with NCP/EP
- Performs the checkout of the ROS code
- Interconnects the IOC buses through the receivers and drivers.

Front-End Scanner Low-Speed (FESL)

The front-end scanner low-speed (FESL) provides logical connection between the CSP and the LIC unit. It is composed of:

- The front-end scanner (FES)
- The front-end scanner adapter (FESA).

FES: It is composed of two layers:

- The front-end layer serializes and deserializes the characters, provides line service management depending on the protocols, and exchanges the characters with the scanner processor.
- The scanner base layer communicates with the CSP via several paths:
  - An asynchronous path is used by the CSP microcode to initialize and send commands to the FESL and the LICs.
  - A cycle steal path supports data exchange of one halfword with the CSP control store.

An interrupt mechanism is used to request line service management.

FESA: The FESA converts FES parallel data into a serialized bit stream and conversely to communicate with the LIC units.

In addition, the FESA performs modem-in control lead confirmation.

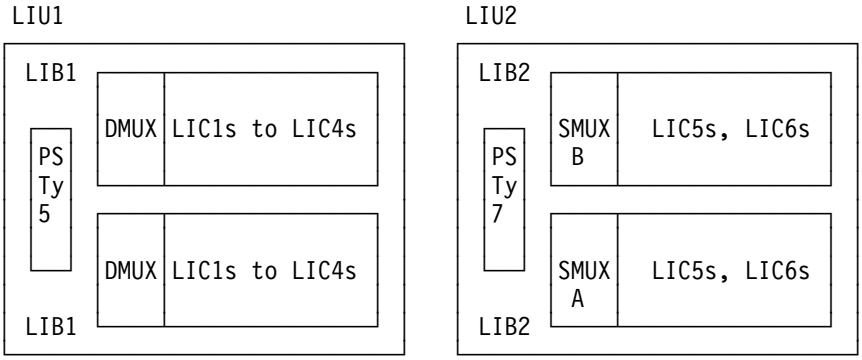
LIC Unit (LIU)

Definition

A line interface coupler unit (LIU) consists of:

- One power supply (PS), associated to
- Two line interface boards (LIBs), housing
- Multiplexer cards (MUXs), and
- Line interface coupler cards (LICs).

Depending on the type of LIC implemented, the above elements are named as follows:



Power Supply

See Chapter 10 for details.

Note: When an LIU is powered OFF, the scanner connected to that LIU must be re-IMLed at next power ON.

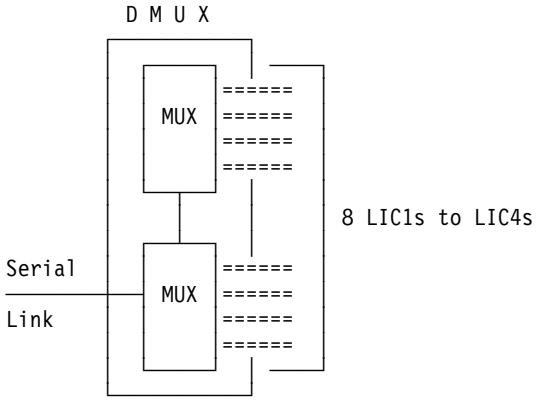
Multiplexer Card (MUX)

Double Multiplexer Card (DMUX)

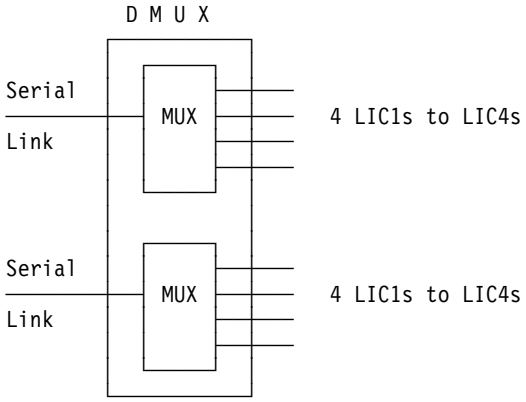
DMUX is associated with LIC1s to LIC4s on LIB1. It provides two serial link attachments to connect to two scanner units. Each of them:

- Converts the serial link bit stream in a suitable form for LIC buses
- Performs the serial link clock recovery, synchronization, and repowering
- Manages LIC control and clocking.

The first MUX can attach up to 8 LICs to one scanner if the second one is not used.



The first MUX can attach up to 4 LICs to one scanner and the second MUX also (see TSS Definition).

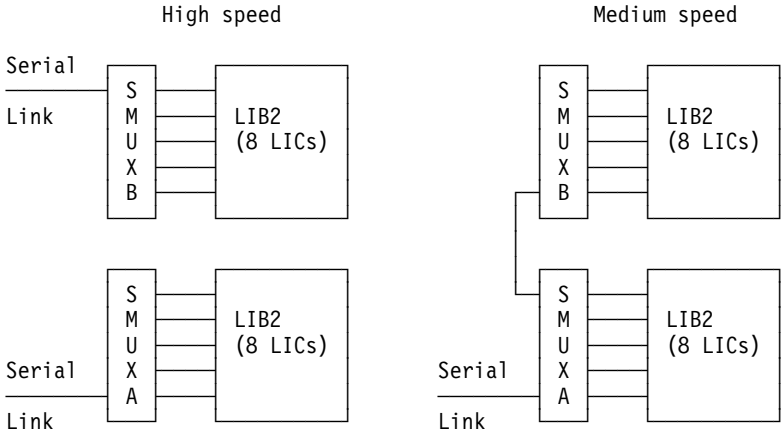


Single Multiplexer Card (SMUX)

SMUXA and SMUXB are slightly different in packaging but are functionally identical.

- SMUXA is associated with eight LIC5s and LIC6s on lower LIB2.
- SMUXB is associated with eight LIC5s and LIC6s on upper LIB2.

Depending on the transmission rate in a given LIU2, only one scanner may be needed for that LIU2. In that case, SMUXB only bypasses the signals and controls from SMUXA to the upper LIB2.



The SMUX cards provide one or two serial link attachment(s) to one or two scanner unit(s). Each of them:

- Converts the serial link bit stream in a suitable form for LIC buses
- Performs the serial link clock recovery, synchronisation and repowering
- Manages LIC control and clocking
- Provides 1 MHz clock signal to the LIC5s and LIC6s
- Provides a 4-bit transmit level bus to the LIC5s DCEs.

Line Interface Coupler (LIC)

One line interface coupler (LIC) attaches up to four FDX/HDX lines to the controller.

Two main families of LICs are available:

- Types 1 to 4 (DTE functionally) to attach up to four:
  - Stand-alone DCEs and/or
  - Direct-attached DTEs.
- Types 5 and 6 (DTE plus DCE functions) to attach up to two telecommunication lines.

LIC1s to LIC4s Characteristics

	LIC Type 1	LIC Type 2 (RPQ) (Note 5)	LIC Type 3	LIC Type 4A (Note 4)	LIC Tpe 4B High Speed (Note 4)
Line Interface	V.24 (RS-232C), V.25 autocall (RS-366), X.21 bis X.20 bis V.25 bis	US wideband. Services 8751, 8801 and 8803 Bell 303	V.35 high-speed	X.21 medium-speed	X.21 high-speed
Transmission Speed	Up to 19200 bps (Note 1)	Up to 230,400 bps (Note 1)	Up to 256,000 bps (Note 1)	Up to 9600 bps (Note 1)	Up to 256,000 bps (Note 1)
Number of Lines	Up to four	One	One	Up to four	One
Transfer Mode	Half-duplex or duplex	Half-duplex or duplex	Half-duplex or duplex	Half-duplex or duplex	Half-duplex or duplex
Protocols	Start-stop, BSC, SDLC	BSC and SDLC	BSC and SDLC	SDLC	SDLC
DTE Clocking (Note 2)	Up to 19200 bps	Not allowed	Not allowed	Not allowed	Not allowed
Direct Attach-ment (Note 3)	Up to 19200 bps	Not allowed	Up to 245,760 bps	Up to 9600 bps	From 19200 to 245,760 bps

Notes:

1. The total number of LICs per CSP is not limited by performance considerations (refer to “Selective Scanning” on page 4-51 for description).
2. Called 'internal clock' on CDF information screen.
3. Direct attachment allowed with internal clock function (ICF).
4. LIC type 4A and LIC type 4B are physically identical (same part number). The microcode sets the LIC to the appropriate type at set mode time.
5. LIC type 2 is available only on RPQ basis.

LIC5s and LIC6s Characteristics

	LIC Type 5	LIC Type 6
Line Interface	Normal Quality or M.1020/1025 4-wire telecommunication lines	DDS, Local Loop, or unloaded baseband 4-wire lines
Transmission Speed	9600 bps 14 400 bps 4800 bps	9600 bps 19.2 or 56 Kbps
Number of Lines	Two	One
Transfer Mode	Half-duplex or duplex	Half-duplex or duplex
Protocols	BSC and SDLC	BSC and SDLC
DTE Clocking	Not allowed	Not allowed
Direct Attach-ment	N/A	N/A

LIC6, Plugging Limitations

- For speeds ≤ 19 200 bps, LIC6s can be plugged contiguously in all card positions of the board.
- For 56 000 bps speed, only one card position out of a pair (even/odd) of card positions can be used to plug the LIC6s in. In this case:

– The LIC6 can be plugged in either the even or the odd position, but any move within a pair of card position (even to odd or odd to even) makes updating the CDF mandatory.
– Any attempt to plug a LIC in the empty position associated with the LIC6 makes the latter inoperative with its yellow LED flashing to signal that condition.

Line Weights

The line weight information is given here for educational purpose only.

Refer to the *Connection and Integration Guide*, SA33-0129, Appendix A, for more information to calculate the line weights.

The weight of a line is a value (0.4 through 100) that represents the percentage of scanner occupation. The total weight of all the lines connected to a scanner must be equal to or less than 100.

The maximum number of LIC positions supported per low-speed scanner depends on the line with the highest transmission speed connected to the scanner, and is limited to:

- Eight LIC1s to LIC4s per scanner (LIU1) or
- Sixteen LIC5s or LIC6s per scanner (LIU2)

At each speed, LIC types 1/4A/5 have two weights per protocol depending on the number of LICs per scanner.

The line weight can be calculated by using the formula:

$$\text{Weight} = \frac{\text{Speed (bps)}}{K}$$

where K is specified by the next table.

Line Protocol	LIC Types 1/4A/5		LIC Types 3/4B/6
	Nbr or LIC 1/4A or Nbr of LIC 5 couples per LSS		
	Less or equal 4	More than 4	
SDLC FDX	1920	1536	2560
SDLC HDX BSC EBCDIC NCP BSC EP	3456	3072	4052
BSC ASCII NCP	2420	2016	3041
Start/Stop (Burst mode)	43xB where B is the nbr of bits/character (e.g. 430 if 10-bit characters)		

Complete information to populate the 3745 properly can be displayed or printed from the *3745 Configuration Program* diskette, GA33-0093 running in any IBM PC.

Inactive Lines

Unlike earlier communication controllers, 3745 LICs are not scanned if **all** the lines connected to them are inactive, and hence do not load the scanner.

LIC Internal Clock Function (ICF)

Implemented on each LIC 1 to 4, the internal clock function (ICF) provides the clock control to:

- Non-clocked DCEs
- Direct-attached terminals.

Serial Link (SL)

A serial link interconnects a LIC unit and a scanner unit via MUX and FESL cards.

Communication Scanner Processor (CSP) Card

The communication scanner processor (CSP) operates under the control of the scanner microcode loaded from the hard disk drive or diskette drive into CSP storage during IML.

Components

As shown by the data flow hereafter, the CSP:

(A) Connects to the IOC bus to receive or transmit data and controls.

(B) Executes the instructions of the microcode to transmit and receive data, supports the link protocols, translates characters, and controls the communication interface.

(C) Stores the microcode, the transmitted/received data, the line interface parameters, and the diagnostics

(D) Provides registers in local storage for current CSP operation and permanent code in the ROS to start the microcode IPL.

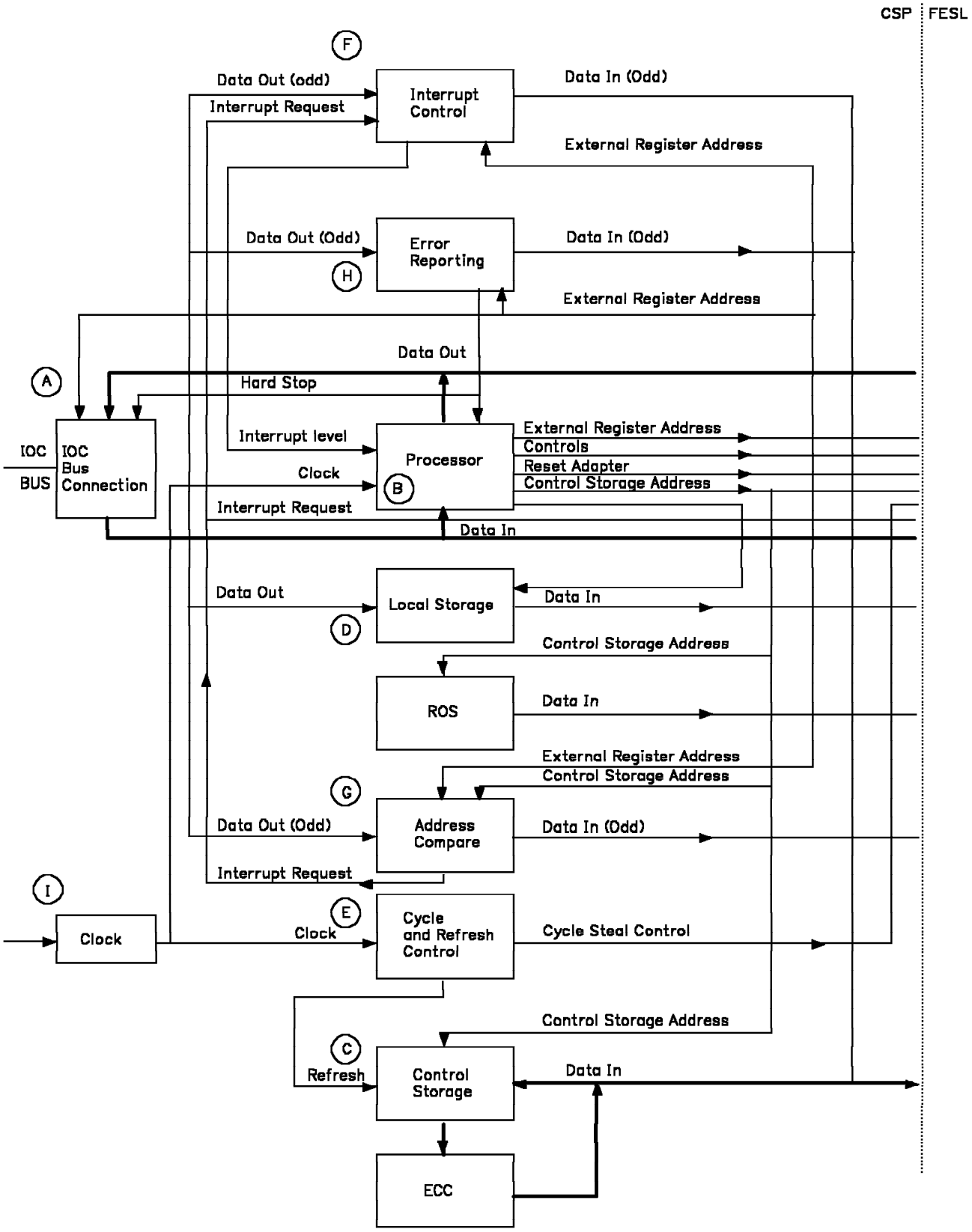
(E) Controls the storage and manages (by hardware only) the cycle steal with the FESL.

(F) Controls the CSP interrupts.

(G) Provides control storage address compare, and generates a CSP interrupt when the selected address is encountered.

(H) Detects and reports the CSP errors via the CSP error register.

(I) Generates clocking signals to the processor, to the FESL card and their associated logic from the basic clock (29.4912 MHz) supplied by the CSP card.


CSP
FESL
F
Data Out (odd)
Interrupt Request
Interrupt Control
Data In (Odd)
External Register Address
Data Out (Odd)
H
Error Reporting
Data In (Odd)
External Register Address
Data Out
A
Hard Stop
IOC
BUS
IOC Bus Connection
Interrupt level
Clock
B
Processor
External Register Address
Controls
Reset Adapter
Control Storage Address
Interrupt Request
Data In
Data Out
D
Local Storage
Data In
Control Storage Address
ROS
Data In
External Register Address
Control Storage Address
G
Data Out (Odd)
Address Compare
Data In (Odd)
Interrupt Request
I
E
Clock
Clock
Cycle and Refresh Control
Cycle Steal Control
Control Storage Address
C
Refresh
Control Storage
Data In
ECC

Local Storage

The local storage is 128 bytes (64 halfwords) addressed by byte or by halfword. It is organized in 16 blocks (or pages) of eight local storage registers (LSRs) each one byte long, used to store the microcode pointers, the cycle steal and command queue control blocks, the program status words, and working register.

The local storage registers can be displayed at or altered from the operator console using the TSS functions.

Read-Only Storage

The read-only storage (ROS) is 8K bytes (4K halfwords) addressed by halfwords. It includes all the permanent code needed for microcode IML and dump, and to perform diagnostics.

The ROS can be displayed from the operator console using the TSS functions.

Control Storage

The control storage is 64K halfwords addressed by halfword.

In each module, an error checking and correction (ECC) mechanism, detects and corrects the single or double bit errors (soft or hard) of that module. When an unrecoverable double error is detected, register X'03' bit 1 is set ON, a hardstop condition is raised, and two data bytes with parity are sent to the CCU.

The control storage is used to store:

- The scanner microcode.
- The buffers for the transmitted and received data, and the line control blocks and parameters.
- Tables and service buffers.

The control storage can be displayed or altered from the operator console using the TSS functions.

CSP External Registers

The CSP uses 32 eight-bit external registers located in the main communication scanner components: IOC bus connection, address compare, error reporting, and front-end scanner (refer to “External Registers Description” on page 4-124 for a detailed description of these registers).

The external registers are connected to the CSP via the data in (odd) bus during read operations, and data out (odd) bus during write operations. Their bits are set ON or OFF by the hardware or the microcode.

The external registers can be displayed or altered from the operator console using the TSS functions.

Address	Function
00	Miscellaneous control
01	IOC bus control
02	IOC bus service
03	CSP error
04	CSP miscellaneous
05	External interrupt request
06	Unused
07	Synchro/configuration data set
08	Unused
09	Unused
0A	Fast get line ID byte 0
0B	Fast get line ID byte 1
0C	Scanner alternate address
10	Extended interrupt request
11	Unused
12	Interrupt req. line interf.add.
13	Asynchronous access RAM A/B/C
14	Data in/out
15	Asynchronous access RAM A/B/C
16	Asynchronous operation status
17	FESL general command
18	Unused
19	PCI/IO interrupt level request
1A	Current CSP interrupt
1B	Address compare control
1C	Address compare byte 0
1D	Address compare byte 1
1E	CSP interrupt masks
1F	Local storage page register (hex)

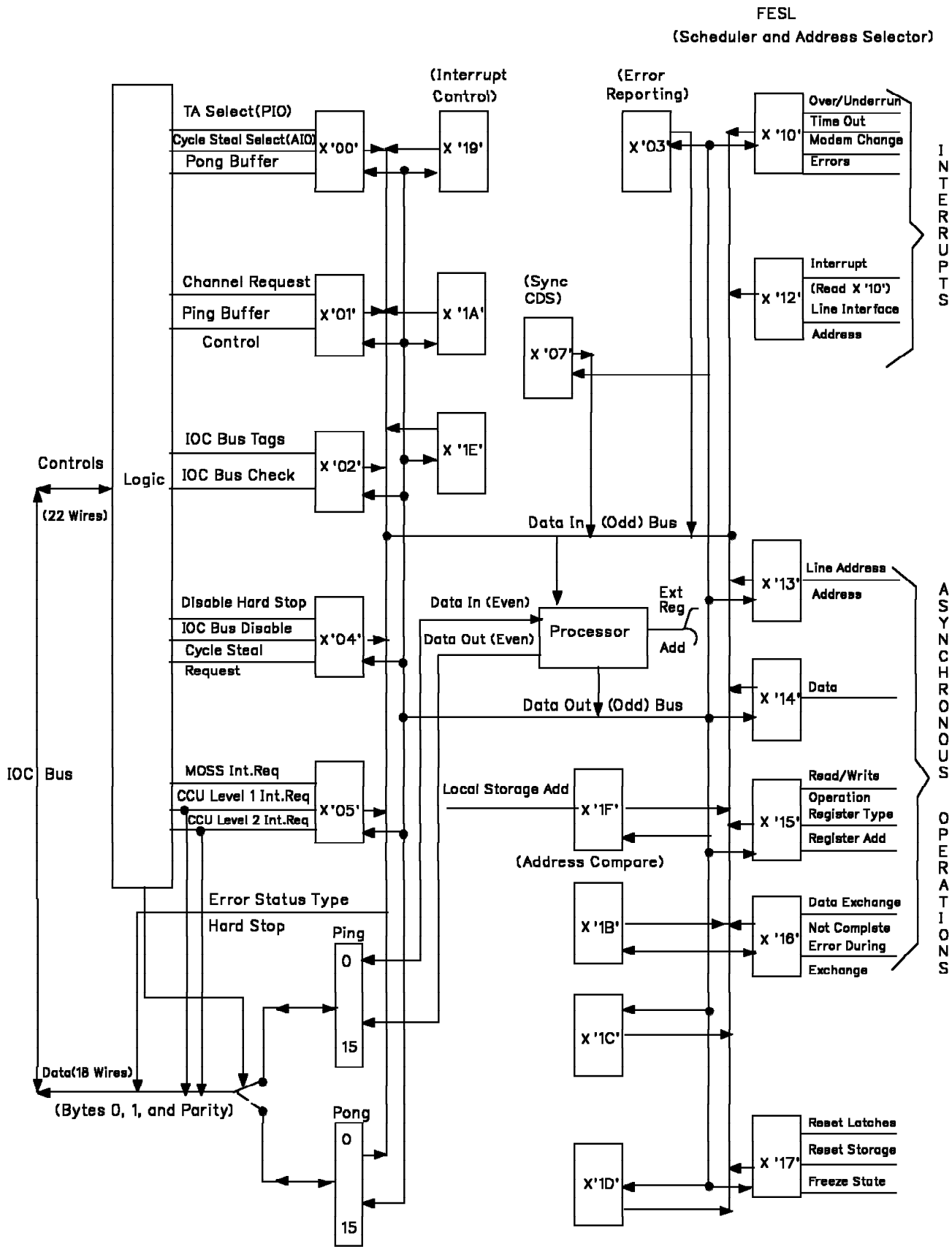


Figure 4-2. CSP External Registers in Data Flow

CCU/CSP Register Use

The CSP external registers are used by the following operations:

- Program-initiated operation (PIO)
- Adapter-initiated operation (AIO)
- Interrupt operation.

Ping/Pong Buffers

Two half-word registers, called the ping and pong buffers, located in the local storage, are alternately connected to the IOC bus in flip/flop mode. They are used for transferring commands, data, and control words between the IOC bus and the CSP.

Switching from one buffer to the other is controlled by the IOC logic.

Processor Characteristics

Program Levels

The interrupts are raised by the microcode (all levels) or by hardware (levels 0, 1, and 2). Levels 0 through 3 can be masked by the microcode. The levels are used as follows:

Level	Function
0	Error handling and address compare
1	CCU instruction processing
2	FESL interrupt processing
3	Queue and command processing
4	(Not used)
5	(Not used)
6	(Not implemented)
7	Timer control and disconnect stop initialization

Clock

An oscillator on the CSP card provides the 29.4912 Mhz square wave to generate the scanner processor's clock. The 29.4912 Mhz is also sent to the FESL card for its clock generation.

Two other clocks are generated in the CSP:

- A 100 ms clock used for timer purposes
- A 15.4 μ clock used to refresh the storage.

Error Management

Internal CSP errors detected by the CSP hardware cause a CSP hardstop. Two bytes of status information are presented by the CSP either to the CCU control program (NCP) or to the MOSS after the hardstop condition is detected.

Hardstop

A hardstop condition is handled by the CSP hardware as follows:

1. A permanent cycle steal request is forced internally to the CSP processor, preventing any cycle steal operation.

   Cycle steal having the highest priority with CSP storage, the CSP microcode processing stops, but the CSP clocks keep running.

   - A level 1 interrupt request is presented to the CCU control program (NCP) if the CSP is in 'connect' mode.
   - A level 4 interrupt request is presented to the MOSS processor control program if the CSP is in 'disconnect' mode.

2. The CCU control program (NCP) responds to its level 1 interrupt request by sending a 'get error status' command, as long as the CSP which has raised the the level 1 is found.

   The CSP then sends the two bytes of 'error status type hardstop' if the CSP clocks are not stopped by the hardstop condition.

3. The MOSS control program responds to its level 4 interrupt request by sending a 'get command completion' command. The CSP then sends the two bytes of 'MOSS command completion' if the CSP clocks are not stopped by the hardstop condition. Then the MOSS control program sends a 'get error status' command to which the CSP responds with the two bytes of 'error status type hardstop'.

The error status type hardstop does not transit through the ping/pong buffers, but is directly presented on the IOC bus data bytes.

The hardstop is reset from the CCU or the MOSS via a programmed reset command or a general reset.

Scanner States

The state of a scanner is shown on the console display.
Refer to the *3745 Service Functions*, SY33-2055. The state may be:

- Inoperative
- Initialized
- Connected
- Disconnected (stop or go)
- Reset.

Inoperative

The scanner is inoperative when it is not in any other state.

Initialized

The scanner is initialized when the CSP is loaded with the microcode and the FESL storage is initialized to all zeros. There is no operation with the control program.

Connected

The scanner is connected when it runs under control of the control program. Errors on CCU I/O instructions are reported to the control program, and errors on MOSS I/O instructions to the MOSS.

Disconnected

The scanner is disconnected when it does not run under control of the control program but under control of the MOSS microcode. Only MOSS I/O instructions are executed. Any instructions from the CCU are not answered.

When disconnected from the control program, the scanner may be:

Running (disconnected-go): The scanner can be in this state while being IMLed, dumped, or being fixed using the TSS services.

Stopped (disconnected-stop): The microcode continues to react to the MOSS instructions. The scanner can be in this state while being fixed using the TSS services.

Any errors are reported to the MOSS.

The scanner may be disconnected by the :

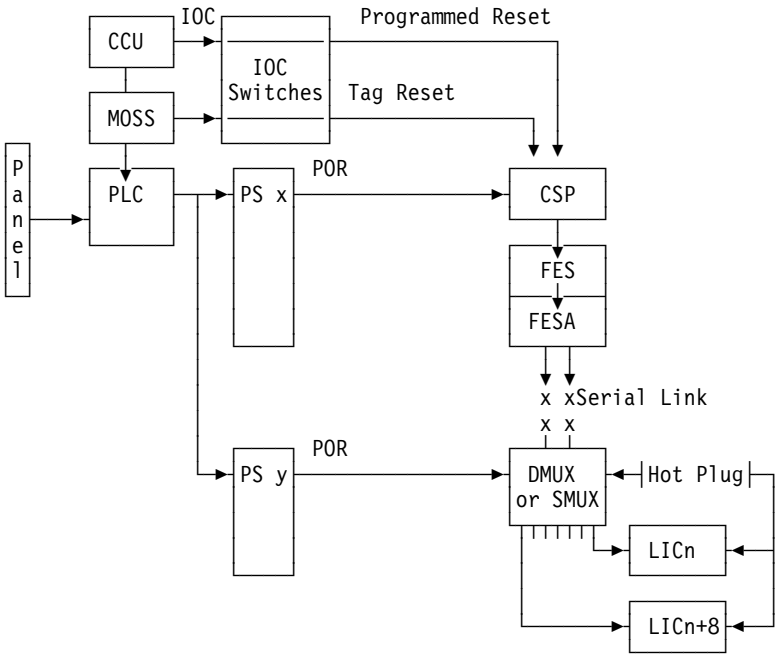
- Operator when entering a service command (stop or address compare with the stop option selected, for example)
- Microcode when certain errors are detected (a CCU interrupt level 1 is requested with the disconnect indication).

CSP Reset

Resetting a CSP can be done by:

1. A specific power ON reset (POR) line coming from the power box for each CSP.
2. A reset tag line coming from both switches: IOC and MOSS (common for all CSPs on one IOC bus).
3. A programmed reset PIO for each CSP, sent by the control program or by the TSS services (operator console).

In these three cases, the state of the CSP is reset. In case of individual POR, the MOSS microcode wait 12 s, before attempting to start an operation again with the CSP.



Power ON Reset

When the CCU activates the line POR (on the IOC bus) during a general IPL or a power ON, the register X'04' bit 2 is set in every scanner. Each of them will:

1. Force a CSP interrupt level 0.
2. Start microcode execution at address 0, initiating the following functions:
   - General reset with a reset of the CSP storage
   - Start of ROS diagnostics
   - Reset of clocks
   - Reset of external registers X'03' (CSP error) and X'08' (error indicators/bad parity generator).
3. Disable the IOC bus and reset the FESL (by setting ON the reset adapter). The LICs and ICFs are reset at the same time.

Programmed Reset

The control program can reset a specific scanner by sending a write command in PIO mode, with the operation code: 'programmed reset', along with the scanner address.

This command is latched on external register '04' bit 1, then, the selected scanner:

1. Disables the hardstop (X'04' bit 3 ON).
2. Starts the microcode at level 0 address 0, with a jump to the end of diagnostics to wait for a dump or re-IML.
3. Resets the interrupt requests to the MOSS and CCU (X'05' bits 0 and 2 ON).
4. Stops the connected FESL (FESL status: freeze) but the storages of the CSP and FESL are not reset and the CSP storage can be dumped.

The 'reset to adapter' is activated by the microcode, rising the X'04' bit 2 during a few instructions.

Tag Reset

The tag reset line originates from the switch card. When activated before a switch operation, it resets all scanners on the same IOC bus.

After a tag reset, there is no complete re-IML of the scanners, merely a short restart sequence in order to allow scanner restart without reloading the microcode. The line is latched on external register X'04' bit 1. When this bit is detected:

1. The ROS microcode is started at address 0.
2. The ROS diagnostics are not run.
3. The CSP external registers are initialized.
4. A general reset is done without a reset of the CSP storage.
5. The reset to FESL is activated.

After the reception of a reset tag, the following operations are done on the FES:

- Reset FES
- Reset RAM
- Freeze FES.

Scanner Commands

The following commands may be used from the operator console to modify the scanner state.

Current State	Possible Scanner Commands	Resulting State
Connected	Stop Reset Dump IML	Disconnected/stop Reset Reset Initialized
Disconnected/go	Stop Reset Dump IML	Disconnected/stop Reset Reset Initialized
Disconnected/stop	Start Reset Dump IML	Disconnected/go Reset Reset Initialized
Reset (or Unknown mode)	Reset Dump IML	Reset Reset Initialized
Initialized	Stop Connect Reset Dump IML	Disconnected/stop Connected Reset Reset Initialized
Inoperative	Reset Dump IML	Reset Reset Initialized

Front End Scanner (FES)

The front-end scanner (FES) is an adapter of the CSP. It is part of the FESL card, and its scanning circuit supports, under the control of the CSP, a wide range of protocols and line interfaces.

Throughput

The FES maximum throughput varies from 256 Kbps (for one line attached), to 307.2 Kbps (for 32 lines at 9600 bps distributed over eight LICs).

The throughput is spread over the LICs up to the last one enabled on the LIC unit-if only one LIC is enabled, all the throughput is devoted to this LIC.

Data Flow

As shown by the data flow hereafter, the FES:

(A) Controls the FES timing, the exchange with the CSP, and the RAM operation.

(B) Controls the transfer of characters between the front-end and the CSP.

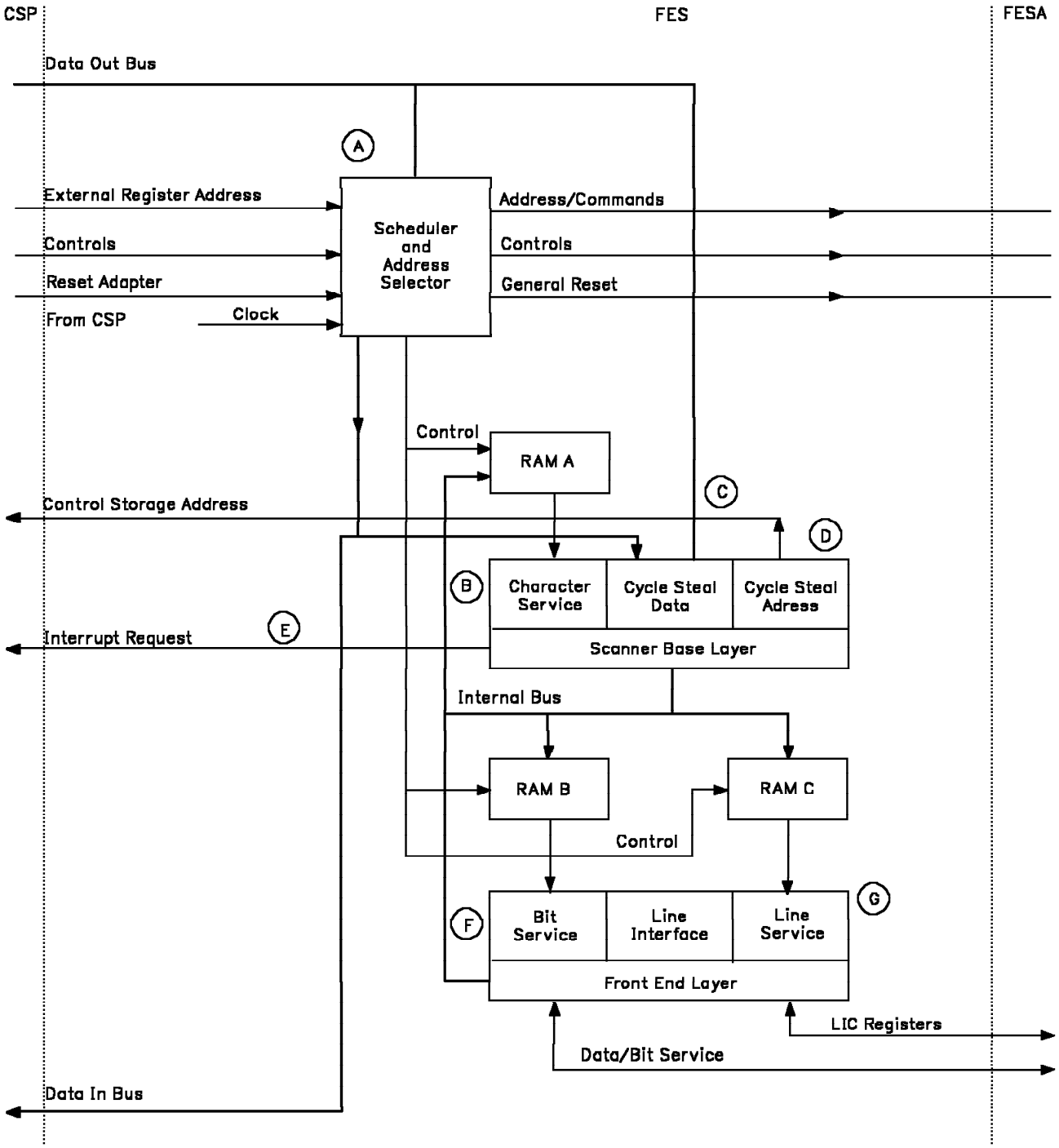
(C) Handles the data halfwords coming from or going to the control storage.

(D) Provides cycle steal control for the CSP.

(E) Interrupts the CSP on level 2 for buffer and data management, and for error reporting.

(F) Serializes/deserializes the data bits transmitted to or received from the FESA.

(G) Provides line services related to link protocol and modem control by managing the LICs via the FESA and the serial link.



Storages

The FES includes three random access storages (RAMs):

- RAM A for character service
- RAM B for bit service
- RAM C for line service.

These RAMs are used in receive and transmit, and give a total of 4x64 = 256 halfwords per RAM.

The FES storages can be displayed or altered from the operator console using the TSS Functions.

Resets FESL

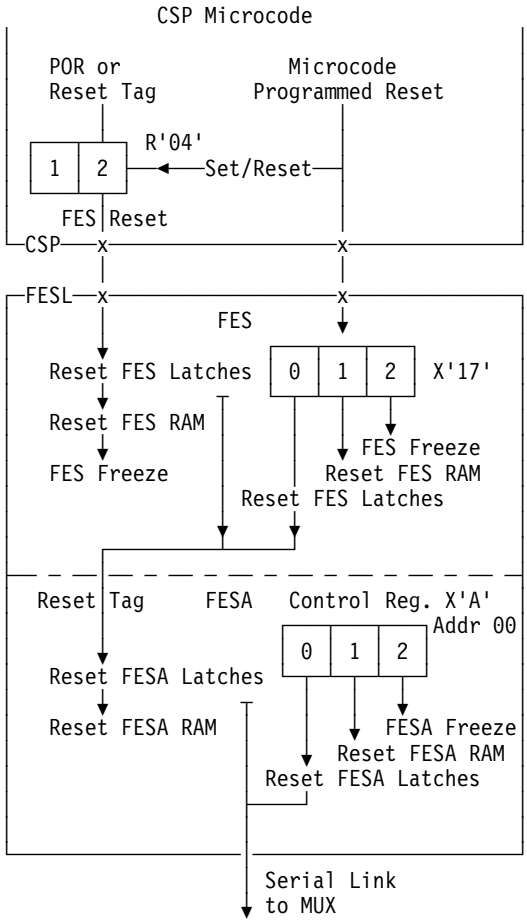
The FES (part of the FESL card) can be reset from the CSP by:

- Power ON reset or reset tag
- Programmed reset.

The FES reset is sent to the FESA to reset:

- The FESA
- The MUXs
- The attached LICs.

FESL Reset Flow



Power ON Reset or Reset Tag

The FES 'reset line' signal is driven by CSP R'04' bit 2. This bit is set by the hardware in case of POR or reset tag, or by the microcode in case of programmed reset. It is reset by the microcode.

Note: The reset tag starts the FES reset twice, once by hardware, as described before, but the microcode, using the same sequence as for programmed reset, starts a second reset.

This 'FES reset' signal:

1. Resets the FES latches and sets the FESA reset tag.
2. Disables the lines between the CSP and the FES.
3. Resets the FES RAMs: all bits are set to zero and the correct parities are written.
4. Stops all scanning (the FES remains in the freeze state after this reset).

The reset tag from FES starts the following sequence in the FESA:

1. Reset FESA latches and set FESA serial link to 'no transmission'.
2. When reset off, reset FESA RAMs.
3. Then, set FESA to normal mode.

Programmed Reset

The FESA can also be reset by the microcode by setting bits 0, 1, and 2 of the control register common address X'A' with line address '00'.

- Bit 0 resets FESA latches and sets FESA serial link to 'no transmission'.
- Bit 1 resets FESA RAMs.
- Bit 2 freezes FESA.

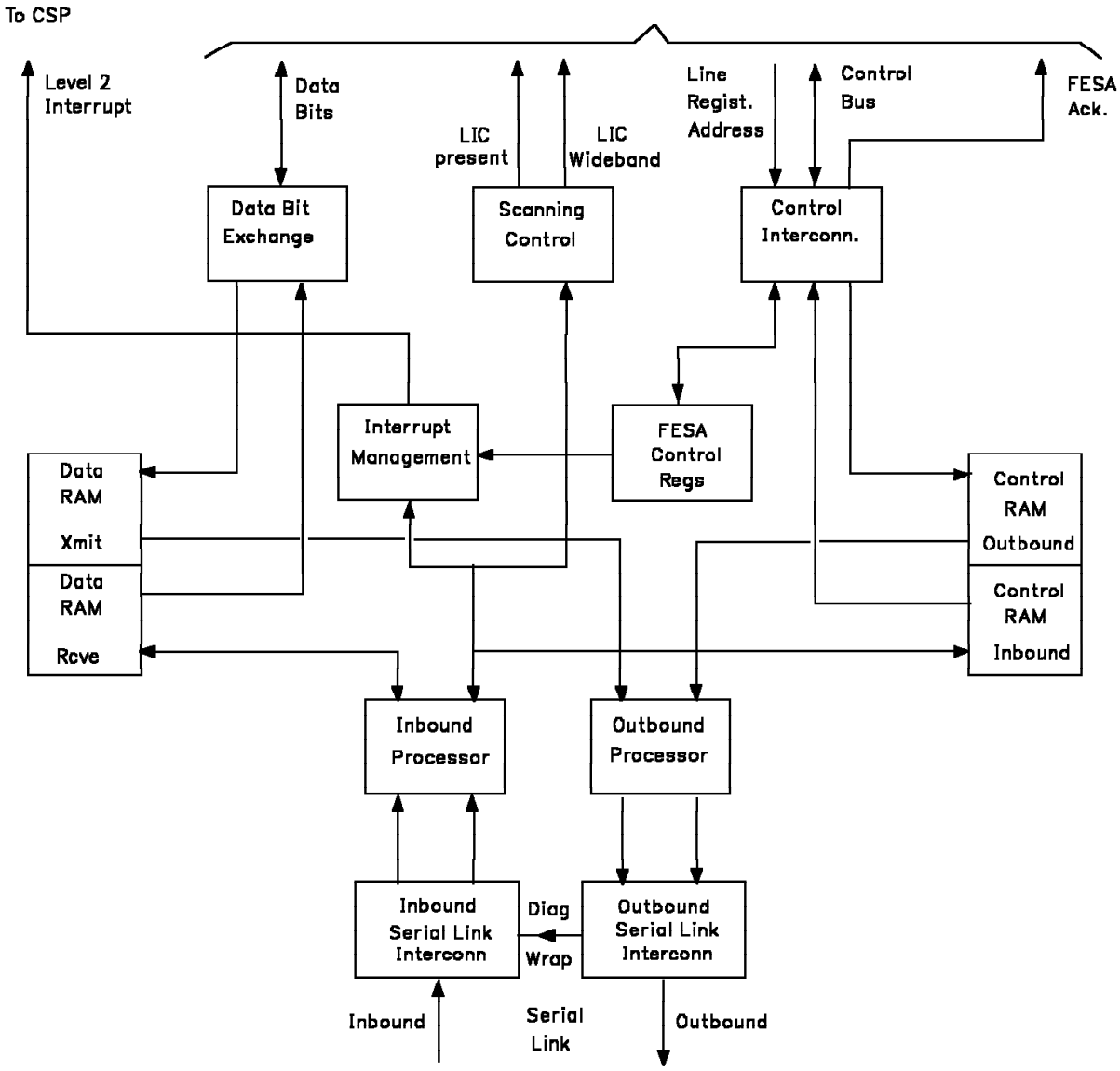
Front End Scanner Adapter (FESA)

The front-end scanner adapter (FESA) is the second part of the FESL card. The purpose of the FESA is to convert the FES parallel bus into the serial link bit stream and conversely.

FESA Data Flow

The FESA data flow shows:

- The interconnection of FESA with the two serial link processors (inbound and outbound).
- The FESA to FES interconnection.
- The internal organization around the FESA RAMs to manage the data and control information exchanged by the FES and the serial link.



FESA-CSP Interconnection

The FESA level 2 interrupt tag allows the FESA to directly communicate with the CSP.

FESA-Serial Link Interconnection

The FESA is connected to the associated LIC units (through the DMUX/SMUX cards) by means of two twisted pairs:

- One pair for the outgoing frames (outbound serial link)
- One pair for the incoming frames (inbound serial link).

FESA Description

The FESA converts FES parallel data into a serial bit stream.

Three RAMs are implemented in the FESA to be used as LIC/MUX registers (inbound and outbound control RAMs), and to be used as data buffer during the process (data RAM).

- The outbound control RAM stores the FES and microcode commands to MUX and LICs (set mode) before to be carried by the proper slots of the outgoing frames sent on the outbound serial link.
- The inbound control RAM stores the MUX and LIC registers information sent by the LICs, and transferred to the CSP on microcode request.
- During the transmit and receive process, the data RAM stores data and control bits for each line. The FESA uses the RAM as a working area to serialize and assemble the data bursts.

Each RAM is divided into 32 areas (one area per line). In the control RAMs, each area contains the line register information.

The RAMs are time-shared by the FES and the two serial link interconnections (inbound and outbound).

The FESA synchronizes the various RAM requests. It monitors the FES RAM access requests and monitors the outbound and inbound serial link frames.

RAMs can be displayed or altered using the TSS functions.

In addition, the FESA:

- Controls the FES scanning mechanism by generating the LIC present and the LIC wideband patterns
- Controls the modem-in leads according to parameters loaded by microcode in the FESA control RAMs
- Detects and reports the errors occurring on the LIC, the MUX, the serial link, or the FESA itself
- Generates the FESA level 2 interrupts to the CSP microcode to report DCE management events or errors
- Performs the diagnostic functions to test the FESL card, the DMUX or SMUX card and the serial link
- Synchronizes the frame and superframe with the MUXs.

FESA RAM Organization

There are three RAMs in the FESA:

- Two 1 Kbyte control RAMs
- One data RAM of 128 halfwords.

FESA Inbound and Outbound Control RAMs

The control RAMs contain all the information required by the FES and the microcode to manage the lines. The control RAMs are divided into 32 areas. Each area stores the contents of the MUX/LIC registers associated to one line.

FESA Inbound/Outbound RAMs Addressing

To access the outbound and inbound RAMs, the CSP microcode uses two CSP external registers: X'13' and X'15'. The FESA external registers are located in the outbound and inbound RAMs.

The following tables show the bits of registers X'13' and X'15' used to access the FESA inbound and outbound RAMs.

X'13': Line Interface Address:

Bits 0 1 2 3 4 5 6 7	Functions
0 1 . . . . C C C . . . . L L X	(Not used, always 00) Card Address Line Address See "FESA Inbound/Outbound RAM Layout"

X'15': Asynchronous Operation Command:

Bits 0 1 2 3 4 5 6 7	Functions
0 . . . . 1 2 . . . . I R R . .	OFF=read, ON=write External See "FESA Inbound/Outbound RAM Layout"

Local Store 6 (CHHITMIO Input):

Bits 0 1 2 3 4 5 6 7	Functions
. . . . I R R E X	OFF=read, ON=write OFF=outbound RAM, ON=inbound RAM See "FESA Inbound/Outbound RAM Layout"

FESA Inbound/Outbound RAM Layout

FESA control register bit 5, controls the type of operation:

OFF Write or output operation
ON Read or input operation.

Bit Decoding	Write (FESA Ctrl Reg Bit 5=0)	Read (FESA Ctrl Reg Bit 5=1)
E I X R R	**Outbound RAM**	**Inbound RAM**
0 0 0 0 0	(Not used)	(Not used)
0 0 0 0 1	Modem out	Driver check pattern
0 0 0 1 0	Line control	Line control
0 0 0 1 1	Driver check mask	Clock failure timer
0 0 1 0 0	FESA modem control	Modem in
0 0 1 0 1	RFS parameters	RFS work timer
0 0 1 1 0	Wrap control	Wrap ctrl/ cable id
0 0 1 1 1	LIC clock mode	LIC card ID/clk mode
0 1 0 0 0	Rcve interrupt control	Rcve interrupt stack
0 1 0 0 1	Xmit interrupt control	Xmit interrupt stack
0 1 0 1 0	FESA/MUX/LIC registers (See note)	FESA/MUX/LIC registers (See note)
. 1 0 1 1	(Not used, FES diag)	(Not used, FES diag)
0 1 1 0 0	DSR/RI parameters	DSR/RI work timer
0 1 1 0 1	RLSD parameters	RFS/TI drop w.rlsd
0 1 1 1 0	ICF RAM 4C	ICF RAM 4C
. 1 1 1 1	(Not used, FES diag)	(Not used, FES diag)

Note: These registers are called 'FESA general registers'. General register '00' is dedicated to line 0, general register '01' is dedicated to line 1, and so on. To extend FESA/MUX/LIC register addressing, the microcode sets the FESA control register with the external register address bit ON (E).

Bit Decoding	Write (FESA Ctrl Reg Bit 5=0)	Read (FESA Ctrl Reg Bit 5=1)
E I X R R	**Outbound RAM**	**Inbound RAM**
1 0 0 1 1	(Not used)	Line error register
1 0 1 0 0	SDF	SDF
1 0 1 0 1	Control SDF/burst size	Control SDF
1 0 1 1 0	PDF	PDF
1 0 1 1 1	Control PDF	Control PDF
1 1 0 0 0	Line diagnostic register	Line diagnostic register
1 1 0 0 1	Logical address	Physical add./EC number
1 1 0 1 0	(Not used, FESA/MUX reg)	(Not used)
1 1 0 1 1	(Not used, FES diag)	(Not used FES diag)
1 1 1 0 0	ICF RAM 4D1	ICF RAM 4D1
1 1 1 0 1	ICF RAM 4D2	ICF RAM 4D2
1 1 1 1 0	(Not used)	Modem-in immediate
1 1 1 1 1	(Not used FES diag)	(Not used FES diag)

FESA Data RAM

The FESA data RAM is divided into 32 areas (one area per line) of four halfwords each:

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Receive SDF	Receive Control
1	Receive PDF 0	(Not used)
2	Receive PDF 1	(Not used)
3	Transmit SDF	Transmit Control 1
4	Transmit PDF	Transmit Control 2

The data RAM is shared by the inbound and outbound serial link data processors, and by the FES for data exchange.

FESA-FES Interconnection Management

LIC-Enabled Leads

The LIC-enabled leads are used by the microcode to dynamically modify the FES scanning range.

A LIC is enabled when at least one line of that LIC is enabled (line control register bit 1 ON).

The LIC is disabled when all lines of the LIC are in the disabled state (line control register bit 1 OFF in all lines.)

The FESA builds the LIC enabled pattern by monitoring the line enabled information sent by the LICs over the inbound serial link.

Note: Disabled LICs are seen as not present by the FES and, consequently, these LICs are not scanned in order to accept higher throughput on remaining actives lines. The 'LIC 0 present' is not given to the FES, which always assumes that the first LIC is present, as a minimum configuration.

The FESA makes no difference between the LIC's physical and logical addresses:

- For the FESA, the position of a LIC is determined by the slots occupied by this LIC in the inbound frame.
- .When a line is enabled by the microcode, and presents 'line enabled' to the FESA, the FESA does not set 'LIC present' immediately.
  Instead, it sets line control register bit 6 in the inbound control RAM ('line enabled remembrance'), and waits for the next 'line enabled' (at next superframe), to set line control register bit 1, and update 'LIC present'.
- The 'LIC-enabled' pattern can be read by the microcode, by successively addressing the two corresponding registers in the FESA.

Note: For example, assuming a LIC plugged in physical position 0 on the LIC board:

If this LIC receives logical address 7, it occupies the slots assigned to LIC number 7 and will be seen as LIC in physical position 7 by the FESA and FES.

If this LIC has no line enabled, it will not be scanned.

LIC Wideband Leads

The LIC wideband information is used by the FES to scan wideband lines four times faster than non-wideband lines.

DCE Lead Management

Modem-in: The modem-in information coming from the lines, is stored in the inbound control RAM address X '1E' of each line.

When a line is scanned by the FES, modem-in is passed by the FESA to the FES for DCE change detection.

To perform the modem-in control, the FESA keeps the confirmed modem-in patterns in the inbound control RAM (Address X'04') for the FES requests, and monitors.

Control of DSR, RI, and RLSD: For any line, the FESA is able to confirm the changes of any of these signals by using specific timers.

DSR, RI, and RLSD are confirmed for both raising and falling edges.

Integration of I (X.21) is performed for I drop only (I going ON is immediately reported to FES in any case.

A different timer starts each time the associated signal switches. The change is confirmed when the time out is reached.

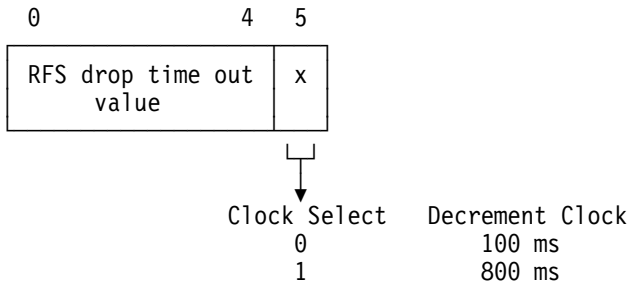
The confirmation delay is specified, for each signal, in a 3-bit parameter field, loaded by the microcode, in the outbound control RAM.

Parameter Value	Time Out
0 0 0	0 (Immediate reporting)
0 0 1	1 ms
0 1 0	4 ms
0 1 1	16 ms
1 0 0	32 ms
1 0 1	64 ms
1 1 0	128 ms
1 1 1 (RI, I, or RLSD)	256 ms
1 1 1 (DSR drop)	10 s
1 1 1 (DSR raising)	Parameter value loaded elsewhere for RI

Control of RFS: Only the drop of RFS is controlled. The FESA monitors the drop on microcode request, in the following way:

The FESA controls the drop of RFS when the microcode loads the RFS drop time out value in the outbound control RAM, along with the clock select bit which chooses the decrement clock.

Outbound Control RAM Address: X'05' (00101)



Control of TI: The immediate value of TI is passed by the FESA to the FES in the modem-in field for DCE change detection.

When TI is masked in the FES, the FESA memorizes (for microcode information) that TI has raised, by setting bit TI 'remembrance' (saved in the inbound control RAM). TI remembrance is reset by the microcode.

Confirmation of Clear (X.21): The 16-bit time confirmation of the X.21 steady states is performed in the LIC.

The only X.21 steady state confirmed by the FESA is 'clear' when the protocol requires a 10 ms confirmation instead of the 16-bit time.

Modem-out: The modem-out pattern coming from the FES, is stored by the FESA in the outbound control RAM.

The FESA also controls the integrity of the modem-out patterns up to the LICs output (LIC driver check).

Serial Link (SL)

All information between the LIC unit and the scanner unit is exchanged via the TSS serial link in two modes:

- Inbound mode from DMUX/SMUX to FESA.

  All LIC information is stacked in FESA RAM and is available for the FES synchronously or asynchronously.

  – The LICs give the data received from transmission lines to the FESA.
  – The FESA reads the registers from the MUXs or LICs.

- Outbound mode from FESA to DMUX/SMUX.

  – The FESA gives to the LICs the data to transmit.
  – The FESA writes into the MUXs or LICs registers.

Connection to LIC5s and LIC6s

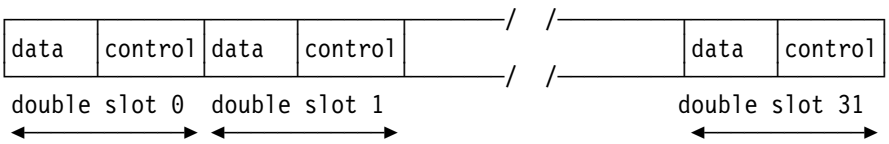
Information exchange between the scanner and LIC5s, and LIC6s DCEs is performed via a serial link, which consists in:

- Inbound link: from LIC to scanner
- Outbound link: from scanner to LIC.

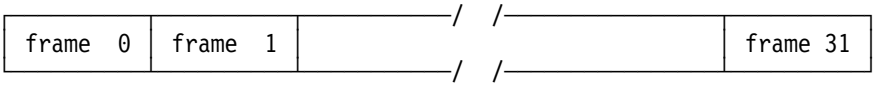
This information is carried in a frame structure.

Frames

A frame is a sequence of 32 double slots (data + control).



A superframe is defined as a sequence of 32 frames. A corresponding delimiter is put in the control slots of frame 31, to indicate the end of a superframe.



Slots

A double slot is made of:

- A data slot
- A control slot.

A slot is an eight-bit element of information.

Data Slots

Data exchange between the scanner and the DCE is performed on a request/answer basis, in order to enslave the serial link data speed to the DCE transmit and receive clocks.

The transmit and data slots carried by the serial outbound and inbound links, contain bursts of data, or are empty. Up to five data bits can be sent or received in a data burst. A data delimiter indicates the actual length of a data burst.

An empty data slot is ignored by the LIC and RTS remains in its previous state.

Control Slots

Control slots are used by the SMUX or DTE (LIC) registers, according to the frame number. Inside a superframe, the control slots of all even frames are dedicated to the V.24 registers.

Notes:

1. One double slot is used for DCEs working at speeds less than 20 Kbps.
2. Four double slots are needed for DCEs working at 56 Kbps.
3. A maximum of four DCEs working at 56 Kbps can be attached to a same scanner.
4. When an even (resp. odd) DCE cassette address is used by a 56 Kbps DCE, the odd (resp. even) corresponding address must be left free.

Double Multiplexer Card (DMUX)

For LIC types 1 to 4 (DTE function only).

DMUX Functions

The two MUXs (on the DMUX card) convert the serial link bit stream coming from the FES into the LICs bit stream.

On the serial link side the DMUX:

- Monitors the frames coming from the FESA.
- Retrieves and decodes the serial link bit stream encoded information (Manchester code).
- Detects the frame sync and transmits it to the LICs.
- Copies in the proper register the incoming information addressed to the DMUX.

On the LIC bus side the DMUX:

- Monitors the serial information coming from the LICs.
- Transmits it to the FESA via the serial link, after Manchester encoding.
- Sends control data stored in DMUX registers to the FESA.

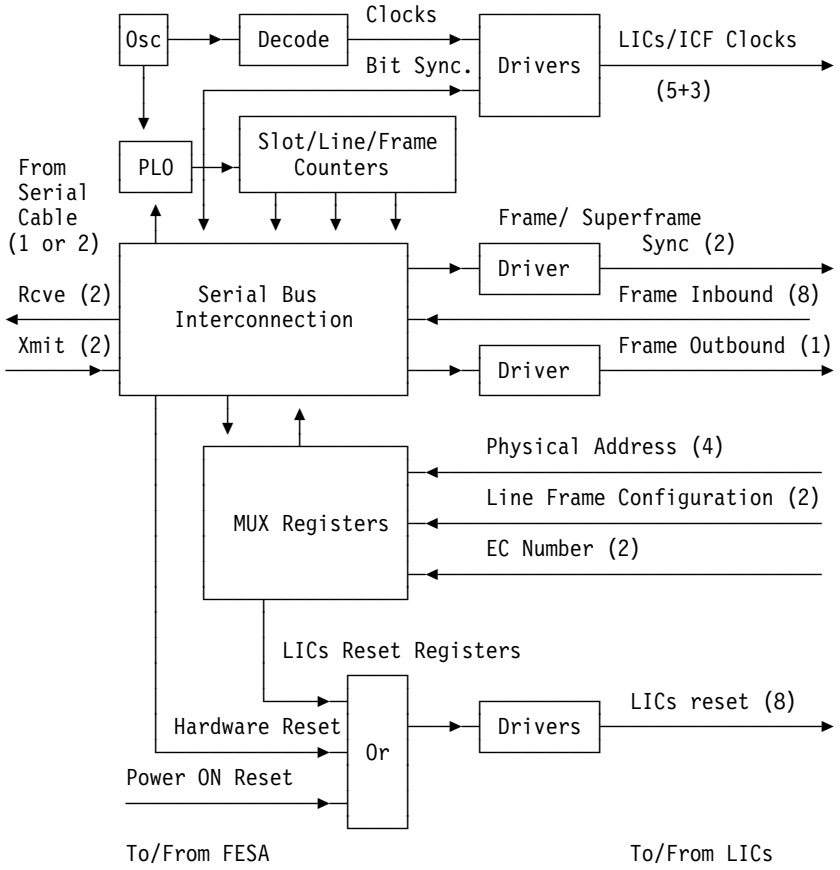
In addition the DMUX provides:

- A bit timing synchronized from the received data (PLO function)
- Three clocks for the LIC internal clock function (ICF)
- Three functional clocks for LICs synchronized on the outbound data flow
- Two clocks for the clock failure detection function assumed by the LIC
- Eight LIC reset commands (to isolate any LIC from the inbound data flow)
- DMUX physical address, machine frame configuration, and DMUX EC number information to the FESA
- Error detection
- Diagnostic facilities.

MUX 1 or 2 Data Flow

There are two multiplexors (MUX) within a DMUX card. Each MUX attaches to one serial link.

The data flow of the two MUXs is identical and is as follow:



Note: Numbers in parentheses are the number of leads.

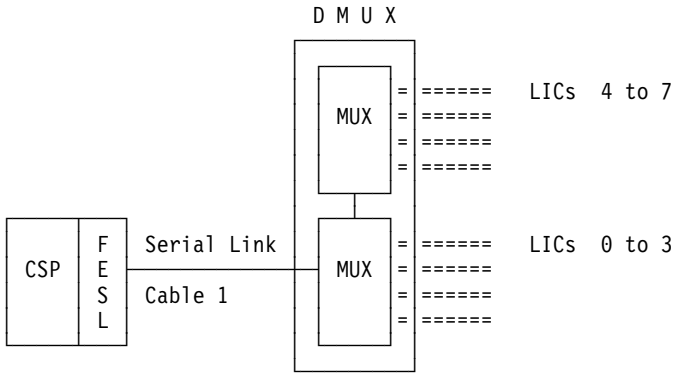
DMUX Functional Description

Only one or both of the two MUXs of the DMUX card can be used, depending on whether they are connecting to one or two scanners.

Connection to One Scanner

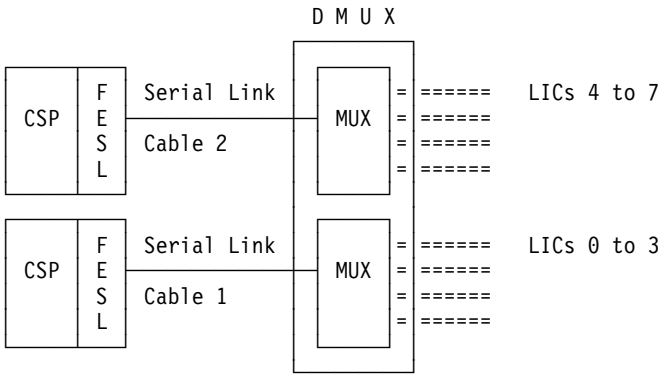
In this "MUX extended configuration", up to 8 LICs (physical addresses 0 to 7) are connected to the scanner.

Such a configuration sets a "cable 2 present" bit OFF in the DMUX card.



Connection to Two Scanners

In this "not extended configuration", up to 4 LICs (physical addresses 0 to 3 or 4 to 7) are connected to each scanner. Such a configuration sets a "cable 2 present" bit ON in the DMUX card.



* Those four LICs are reported to their scanners as LICs 0-3.

Serial link cable 1 can be removed (for example to maintain CSP) without disturbing serial link cable 2 operations.

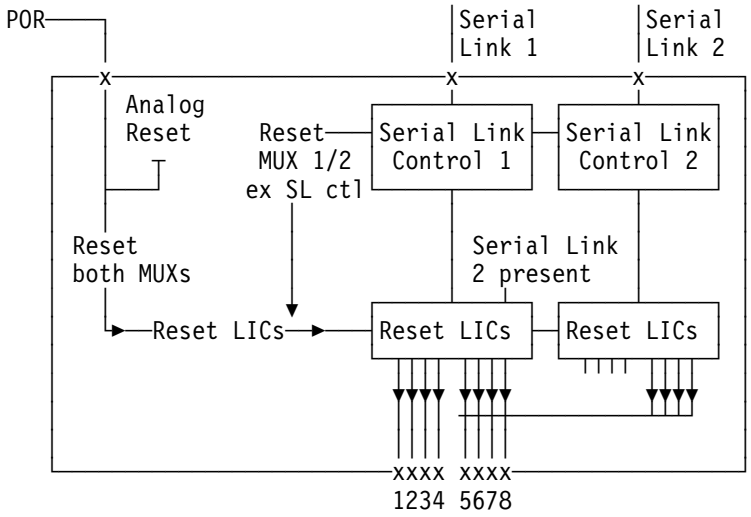
This is also true for serial link cable 2 removal, but with the following restriction:

- First unplug the cable at the FESL end.
- Then unplug the cable at the DMUX end.

Note: When a LIC unit (LIU) is powered OFF, the scanners connected to that LIU must be re-IMLed at next power ON.

Reset DMUX

The DMUX card and, consequently the two MUXs, can be reset:



1. A POR line coming from the associated power box (one line for two DMUX cards). In that case, a MUX reset is executed and a reset LIC is sent to each associated LIC.
2. The DMUX card being HOT pluggable, an analog reset circuit allows performing the reset as for a POR line.
3. If 'no transmission' is detected on the serial link, the MUX itself generates a reset MUX, except on the serial link control part, and generates a reset on the associated LICs (extend mode or not.)

LIC reset

LIC reset is executed either by the selective reset LIC line coming from the MUX or by an analog reset circuit on the LIC itself, in case of hot plugging.

A selective reset can be executed by the microcode through the serial link by selecting the appropriate bit in the LIC reset register of the MUX.

The reset allows isolating the LIC from the MUX (via the LIC bus), and from the attached lines.

DMUX Hot Plugging

Bottom connectors with several level of indentations, and an analogic power ON reset delay, provide the required power sequences.

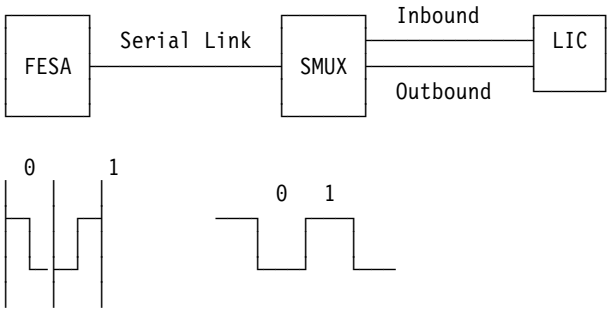
Single Multiplexer Card (SMUXA/B)

They are used for LIC types 5 and 6 (DTE plus DCE functions). SMUXA and SMUXB are slightly different in packaging (cable connector), but are functionally identical. SMUXA or SMUXB are hereafter referred to as SMUX cards.

- SMUXA is associated to the lower board of a LIC unit 2.
- SMUXB is associated to the upper board of a LIC unit 2.

SMUX Functions

The SMUX cards convert the serial Manchester-encoded bit stream into the LIC serial outbound bit stream and conversely the serial inbound bit stream from the LICs into serial Manchester-encoded bit stream for the FES.



On the serial link side, the SMUX:

- Monitors the frames coming from the FESA.
- Retrieves and decodes the Manchester-encoded information.
- Detects the frame synchronization pattern and transmits sync pulses to the LICs.
- Loads the information devoted to the SMUX into the proper register.

On the LIC bus side, the SMUX:

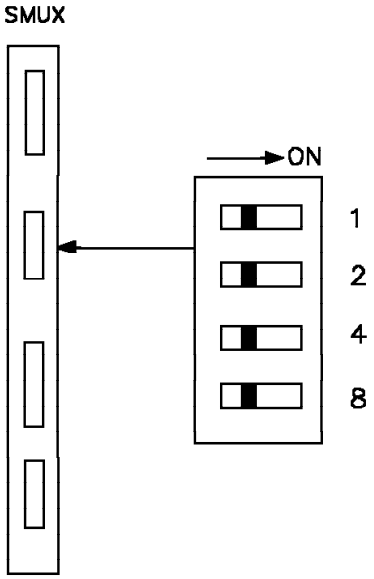
- Monitors the serial information coming from the LICs.
- Transmits it to the FESA after Manchester-encoding.
- Sends the control information from the SMUX registers to the FESA.

In addition the SMUX provides:

- A bit timing synchronized from the received data (PLO function)
- Two functional clock signals to the LICs (synchronized from the outbound data flow)
- Eight LIC reset commands (to isolate any LIC from the inbound data flow)
- SMUX physical address, machine frame configuration, SMUX EC number and "LIC5/6 present" indication
- Error detection
- Diagnostic facilities
- 1 MHz clock signal to the LICs for PKD operation
- Four binary-coded bits to LICs 5 for transmit level setting (see "Transmit Level" next).

Transmit Level

The transmit level is country-dependent. The correct transmit level for a given country must be set at installation time by the CE on each SMUX card, by means of four switches (0 to -15 dBm).



At IML, those switch values are read into each corresponding LIC5 non-volatile RAM. However, if one of those transmit levels has to be slightly modified in the field (for example to compensate for line impairments), it can be modified from the PKD by the CE.

Card Replacement

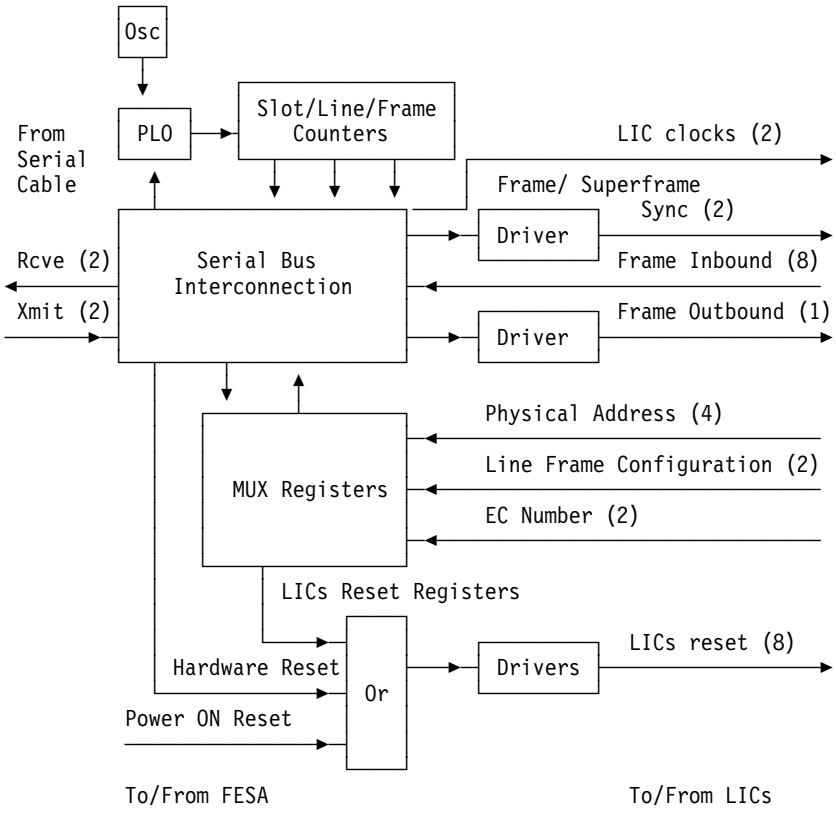
In case of SMUX field replacement, carefully note down the previous SMUX switch setting, or use the following table to determine the maximum authorized transmit level in your country.

Country (Nonswitched Lines)	Xmit Level
AG and A/PG (generally)	0
Australia	-13
Canada	0
Chile	- 6
Denmark	-10
EMEA (generally)	- 6
Finland	-10
France	-15

Country (Nonswitched Lines)	Xmit Level
Greece	0
Hong-Kong	- 9
Iceland	-10
Ireland	0
Italy	-10
Japan	-15
Sweden	-10
UK	-13

SMUX Data Flow

SMUX A/B data flow is as follows:



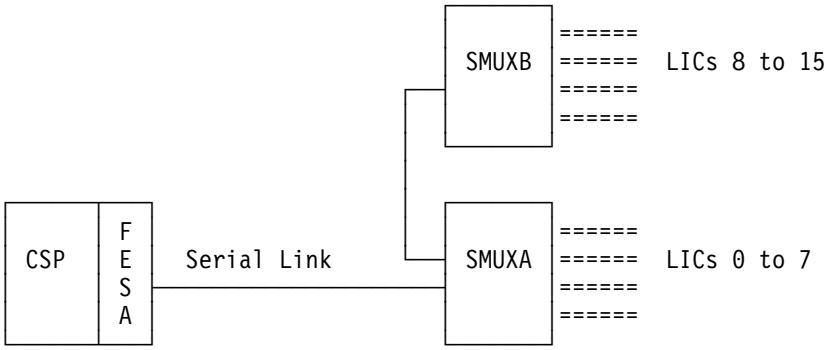
Note: Numbers in parentheses indicate the number of leads.

SMUX Functional Description

Although SMUXB might not be used, SMUXA and SMUXB are permanently installed on both LIB2s of an LIU2. If a serial link cable is connected to a SMUXB, it works exactly as with a SMUXA.

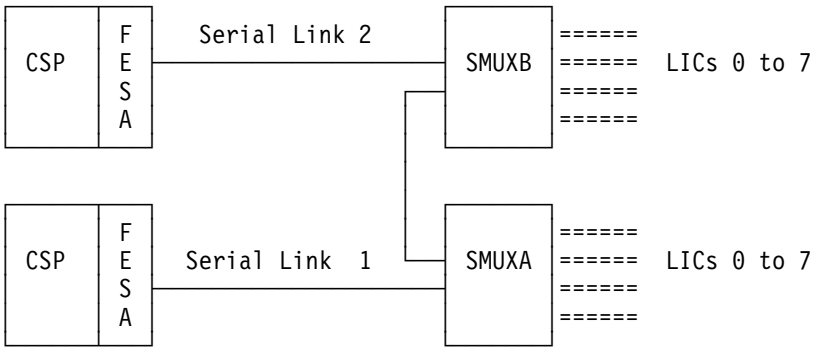
Connection to One Scanner

Up to 16 LICs (address 0 to 15) are connected to the scanner.



Connection to Two Scanners

Up to 8 LICs (address 0 to 7) are connected to each scanner.



SMUX Reset

The SMUX A and B cards can be reset in one of the following ways:

1. By the POR line coming from the associated LIU2 power supply. The POR line acts on both SMUX A and B cards. Both SMUX A and B are reset and send a 'LIC reset' to each associated LIC.
2. By an 'analog reset' when a SMUX card is hot-plugged.
3. When an absence of signal is detected on the outbound serial link.

LIC Reset

LIC reset is done either by the selective reset line coming from the SMUX or by an analog reset circuit when the LIC is hot-plugged. Selective reset can be done:

- Either by microcode through the serial link, or
- By selecting the appropriate bit in the LIC registers of the SMUX.

SMUX Hot Plugging

Bottom connectors with several levels of indentations and an analogic power ON reset delay provide the required power sequences.

LICs Type 1 to 4 Cards

LICs type 1 to 4 provide the DTE function only. They connect the DMUX card to various types of DCEs or direct-attached DTEs. There are four types of LIC according to the CCITT interfaces.

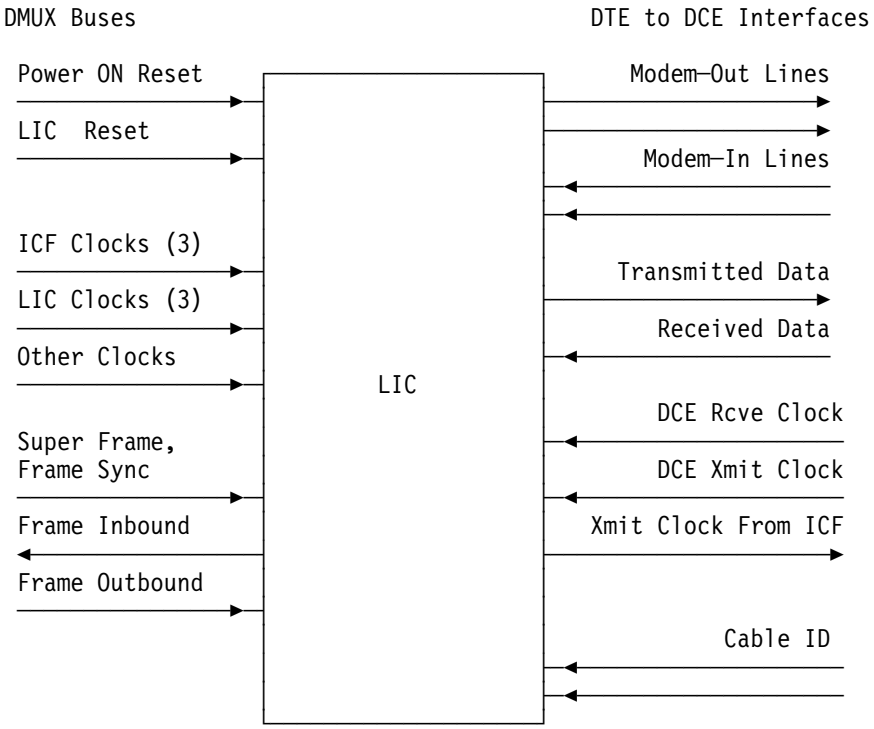
The LIC1 to LIC4 to DMUX interconnection is identical (the number and meaning of bits may however differ according to the type of DCE attachment).

Some LICs require internally generated clock signals for either:

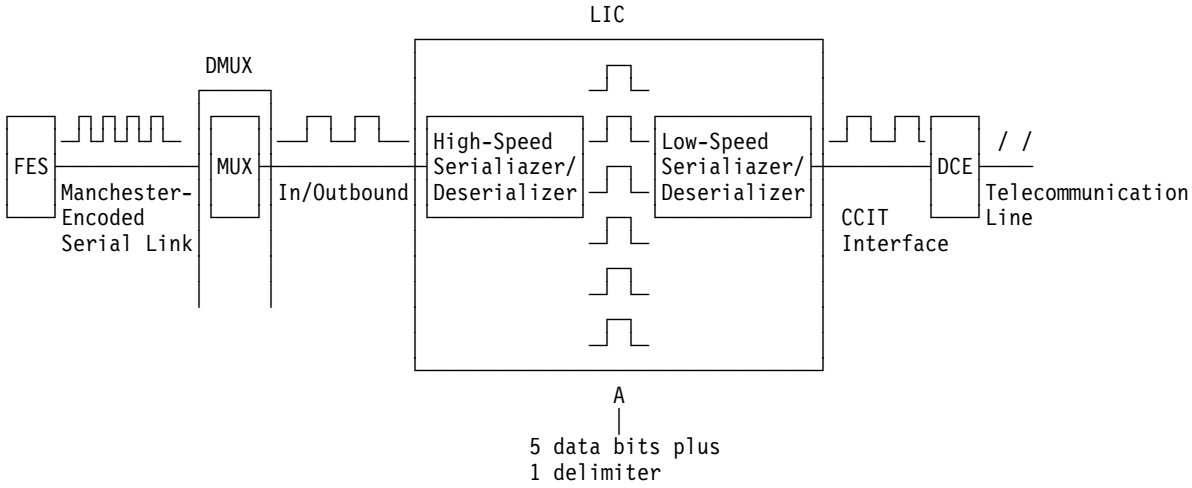
- Low-speed DCE attachment
- Direct attachment to terminals.

The internal clock function (ICF) on the LIC card itself, provides these clock facilities.

Interface Lines



Transmit/Receive Data Mechanism



The data is passed from/to the FES to the telecommunication line via the MUX and LIC as shown above. The LIC communicates with the FES to:

- Request new data to be transmitted (when in transmit mode)
- Signal 'transmit overrun/underrun': 'LIC line error register bit 3' (when in transmit mode)
- Signal 'overrun': 'LIC line error register bit 2' if more than 5 data bits are received between two serial link requests (when in receive mode).

LIC Reset

See also "DMUX reset".

The purpose of the LIC reset command is to isolate the LIC from the LIC bus and from the attached lines (the DMUX card provides one reset lead per LIC).

- At power ON, all leads are activated during the power ON reset, until the DMUX detects a start pattern from the FESA.
- After power ON, one reset lead may be activated on request, to reset the logic in the corresponding LIC and to disable all the line interface drivers.
- In the reset state, no information can be exchanged with this LIC.
- Any command to a LIC in reset state ends with a LIC check at the FES-FESA interconnection.

Line Enable/Disable

When a line is enabled, it accepts read/write operations as well as data transmission/reception and DCE interface handling.

After a LIC reset, all lines are automatically disabled and do not manage any more data transmission/reception or DCE interface.

- On one-line LICs, when the line is disabled (but not in the reset state), it can be written **and** read.
- On four-line LICs:
  - When the four lines are disabled (but not in the reset state), it can be written **but cannot be read**.
  - When one line at least is enabled, it can be written **and** read.

Each LIC (not under reset state) monitors the incoming and outgoing frames to receive and send register information belonging to its lines. This allows the lines, even disabled, to receive commands from the microcode and the FES, and to pass status information to the scanner. These facilities allow the FESA to:

- Handle the line enabled/disabled bits to generate the LIC present pattern.
- Modify the FES scanning and dynamically adapt the FES resources to the line configuration changes, without manual intervention.

Note: For example, assuming a LIC plugged in physical position 0 on the LIC board:

- If this LIC receives logical address 7, it occupies the slots assigned to LIC number 7 and is seen as a LIC in physical position 7 by the FESA and FES.
- If this LIC has no line enabled, it will not be scanned.

See “LIC-Enabled Leads” on page 4-35 for the microcode handling of these leads.

Selective Scanning

Selective scanning gives more flexibility for backup configurations using the same scanner, since only those LICs with at least one line enabled, are scanned.

As a result, the total weight of the LICs which can be installed or connected physically to one scanner may be more than the supported weight of the scanner (100), as long as the total weight of the lines enabled at any time, does not exceed the scanner's supported weight.

Selective scanning enables the customer to install on the same scanner, LICs which are enabled only for one configuration at one time, and LICS which will be enabled only for a second configuration later (the first configuration having to be disabled first).

Selective scanning is managed by the CSP microcode.

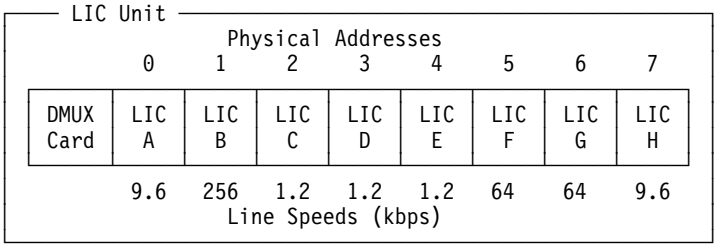
Notes:

1. When modifying a configuration which includes LIC4(s), the scanner must be re-IMLed.
2. No checking is made to verify that a scanner is overloaded.

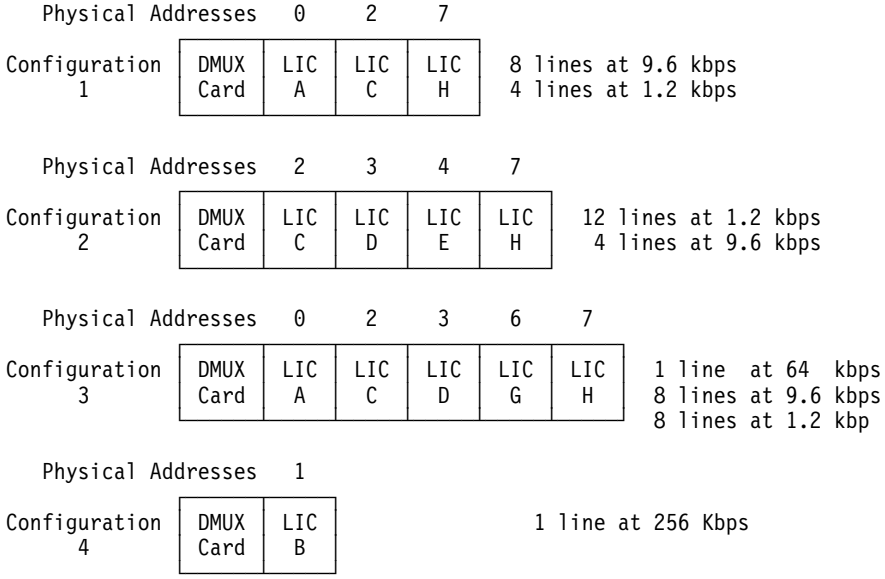
LIC Logical Addressing Function

The LIC logical function allows selective scanning. In the example of configuration changes hereafter:

- The logical address function allows multi-configuration changes without card plugging or unplugging.



- The customer may define several configurations without any physical LIC changes. For example:

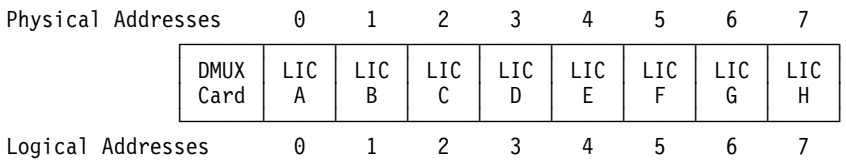


LIC Swap

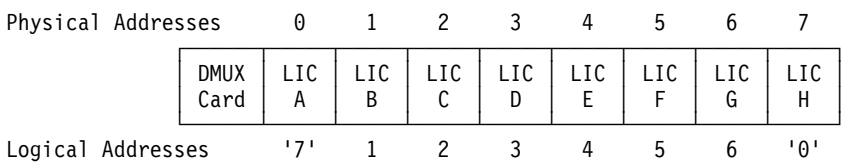
The logical addressing function implemented in the 3745 LICs, allows LIC address swapping.

Supposing two LICs, one plugged at physical address A (LICA) and the other one plugged at physical address H (LICH), the logical addressing function allows to 'swap' the logical addresses between LICA and LICH. For example, assign logical address A to LICH, and logical address H to LICA.

Before the swap



After the swap



After the swap, on the serial link, LICA takes the slots of LICH and LICH takes the slots of LICA.

LIC Address Register Contents

In Write Mode		In Read Mode	
Bits	**Meanings**	**Bits**	**Meanings**
0	LIC logical address bit 0	0	LIC wired address bit 0
1	LIC logical address bit 1	1	LIC wired address bit 1
2	LIC logical address bit 2	2	LIC wired address bit 2
3	Enable/disable logical add	3	(Not used)
4	(Not used)	4	EC number
5	(Not used)	5	EC number

LIC Control Register

The LIC control register X'02' bits 1 and 3 (line enable E0 and E1) control the swapping.

Bits	Meaning
0	High-speed line
1	Line enable E0
2	X.21 CCITT used by FESA 80
3	Line enable E1
4	(Not used)
5	Transmit bit echo

Enable Clock Mode

Register X'03' bits 4 and 5 select the clock mode. They are OFF after a reset command (that is 00 = diag mode).

There is no clock until the enable clock mode bit is set, except if the LIC detects that the cable ID is a local attach cable. After the reset the LIC forces the local attach clock mode: 11 (speed given by ICF after reset: 2400 bps).

Transmit Clock Gating by RFS (LICs 1, 2, and 3)

If LIC control register X'02' bit 2 is set for a given line, it allows gating the interface transmit clock by the modem-in lead RFS (despite the clock mode setting).

There is no clock failure reporting if the transmit clock on the interface is stopped because RFS is OFF.

LIC 4 Personalization

There is only one LIC type 4 part number. LIC type 4A or 4B (personalization) is defined at IML by the microcode.

LIC 4 "wideband bit", when set, specifies LIC 4A depending on the NCP speed parameter definition at set mode time.

LIC Wideband with Line Speed Higher than 128 Kbps

The wideband LIC is scanned four times faster than the non-wideband LIC. The wideband LIC line takes four data slots in the frame.

- With a line speed less than 128 kbps, the four data slots dedicated to the LIC in a frame are sufficient for the four lines attached.
- With a line speed higher than 128 kbps, only one line may be attached to the scanner (the 'high-speed line' bit is set in the control register).

RTS Through DCE or Data Paths

According to the value of modem-out bit 5, the lead RTS of the DCE interface will change with the new modem-out register or at the boundary of a transmit data burst as follows:

- RTS through the DCE path:

  When modem-out bit 5 is ON, the RTS changes according to the modem-out bit 1 sent to the LIC by the FESA in even frames.
  The RTS change occurs as soon as the new modem-out is loaded.

- RTS through the data path:

  When modem-out bit 5 is OFF, the RTS changes according to the value of bit 0 of the transmit data burst.
  The RTS change occurs at the boundary of the transmit burst, that is, with the last data bit.

LIC Modem-In Process for Non-X.21 Lines

The LIC sends the modem-in information without any process to the FESA. The FESA then processes this information in order to raise an interrupt to the FES only with confirmed modem-in information.
For more details see “DCE Lead Management” on page 4-36.

LIC Modem-In Process for X.21 Lines

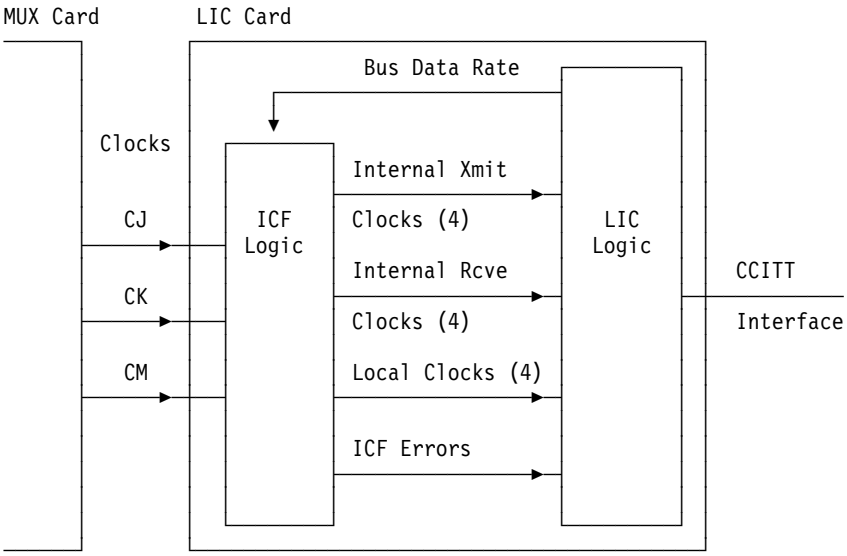
The LIC performs the confirmation of X.21 steady states by scanning a 16-bit time.

The LIC sends the modem-in information to the FESA and when the state is confirmed after the 16-bit count, the 'bit state confirm' of X.21 modem-in register is raised.

The microcode has the option (when register X'06' is ON) to perform a 10 ms confirmation instead of a 16-bit time. In that case, the LIC sends modem-In to the FESA, and the FESA itself confirms the state for DCE CLEAR after a 10 ms count, state confirm still being delivered after a 16-bit time for the other three states.

Internal Clock Function (ICF)

ICF Data Flow



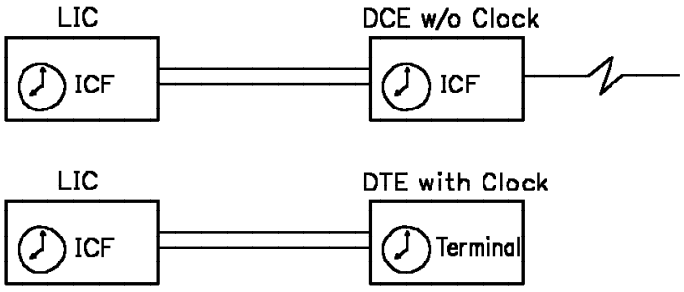
For each line, the transmission speed is selected at initialization by the microcode (set mode depending on NCP generation). The internal clock function (ICF) provides the transmit and/or receive clocks to the:

- LICs and their low-speed non-clocked DCEs.
- LICs only when their direct-attached terminals use their own clock.
- LICs and their direct-attached unclocked terminals.

The ICF is not used when a LIC is attached to a clocked DCE.

Depending on the above configurations, the ICF mode can be 'internal', '3745' or 'external', and the clockings are provided as follows.

Internal Mode

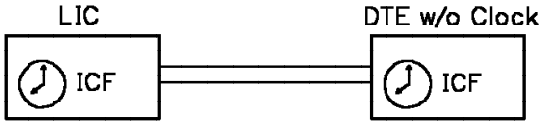


The internal clocking mode is set by the microcode at initialization time in the LIC card (ICF activated).
NCP parameters: clock=internal, speed=xxx.

The following data rates are available:

- For asynchronous lines (start-stop)
  - From 50 to 19 200 bps
  - 1200 bps transmit / 75 bps receive (for test purposes).
- For synchronous lines (BSC or SDLC): from 50 to 4800 bps.

3745 Mode

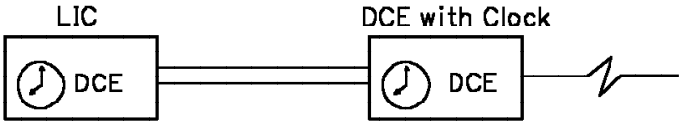


The 3745 clocking mode is set by the microcode at initialization time in the LIC card (ICF activated).
NCP parameters=direct attach, speed=xxx.

The following data rates are available:

- For asynchronous lines (start-stop): from 50 to 19 200 bps.
- For synchronous lines
  - Up to 245 760 bps for SDLC
  - Up to 55 845 bps for BSC

External Mode



The external clocking mode does not activate the ICF since the DCE provides the transmit and receive clocks to both the LIC and itself.

LIC Wraps

Refer to “Problem Determination Aids for LIC1s to LIC4s” on page 4-205 for more information on wraps, to *Advanced Operations Guide*, SA33-0097, to invoke these functions from the MOSS console and to *Diagnostics Description,* SY33-2059, for diagnostics using LIC wraps.

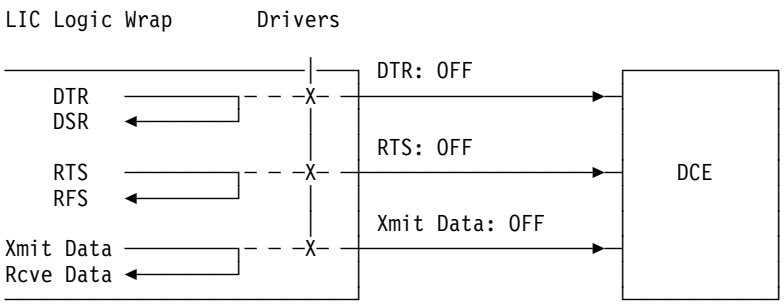
Two LIC wraps are available on the CCITT interface of the LICs:

- Loop 1 (line wrap)
- Loop 3 (loop back).

(LIC register X'2' bit 'loop 1' or bit 'loop 3').

Loop 1 on V.24

Loop 1 on the V.24 interface performs the following wraps:

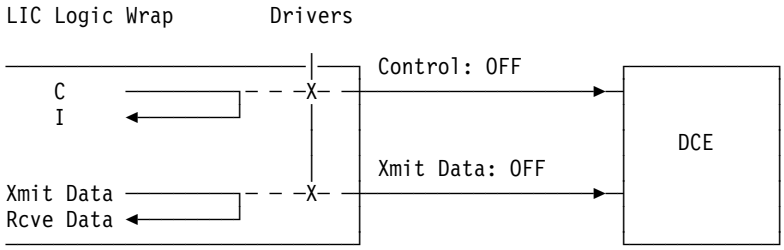


Loop 1 on V.25

For the V.25 autocall interface, transmit data line is replaced by digit present line inside the LIC1 hardware, and no transmit or receive clock is available.

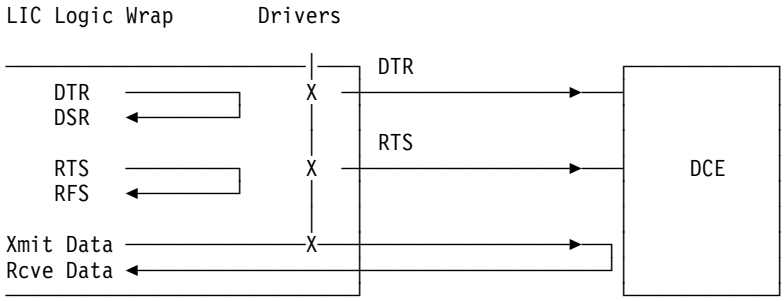
Loop 1 on X.21

Loop 1 on the X.21 interface performs the following wraps:



Loop 3 on V.24

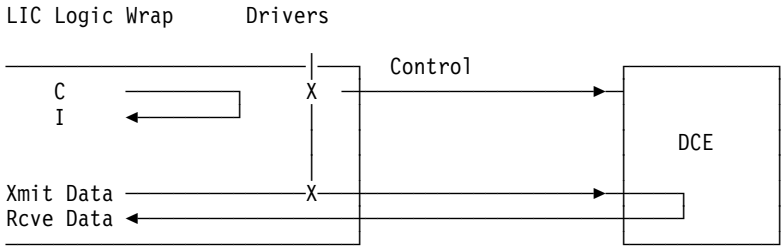
Loop 3 on the V.24 interface performs the following wraps:



Only DTR and RTS are wrapped to DSR and RFS before the drivers.

Loop 3 on X.21

'Loop 3' on the X.21 interface performs the following wrap:



Hot Plugging of LICs

The bottom of the LIC card has three levels of indentation to provide the required power sequences. When plugged power ON, the LIC logic gets into the reset state long enough to avoid transient disturbances on the interfaces.

LICs Type 5 and 6 DTE Function

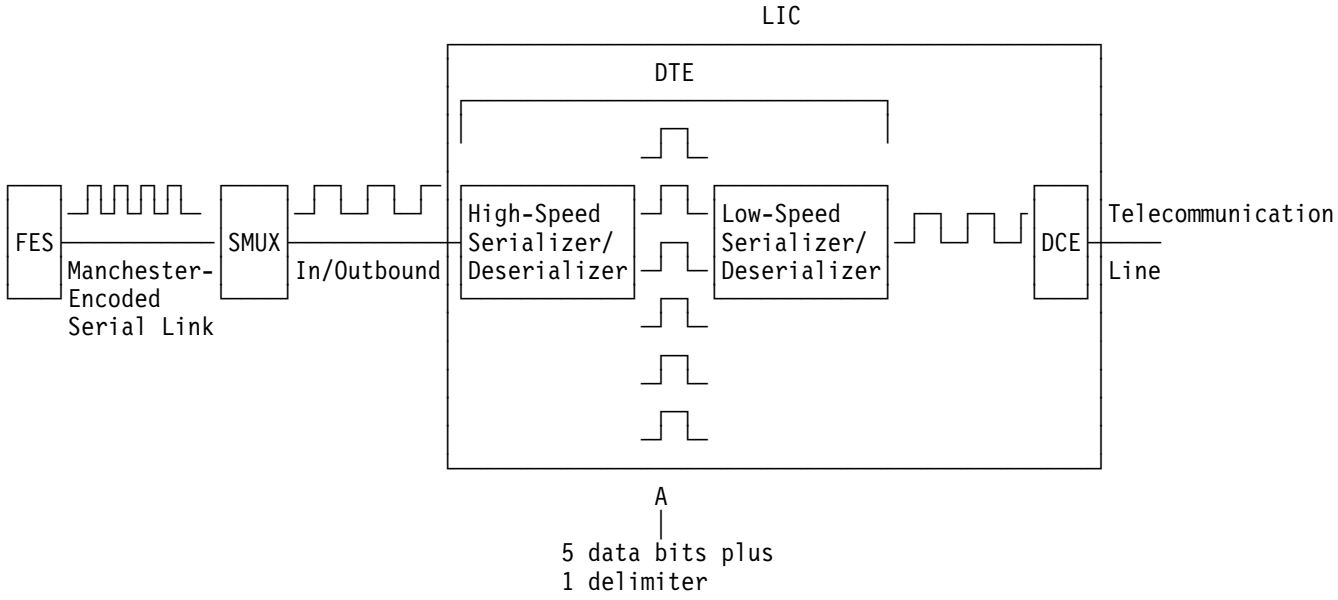
LICs type 5 and 6 provide DTE and integrated DCE functions. They connect SMUX cards to telecommunication lines.

- LIC5s connect to normal quality or M.1020/1025 4-wire telecommunication lines.
- LIC6s connect to DDS, local loops or unloaded baseband 4-wire lines in the US only.

The following is information about the DTE part of LIC5s and LIC6s which is common to both LICs. Refer to the specific LIC5 or LIC6 section for DCE function.

Transmit/Receive Data Mechanism

LIC5s and LIC6s interconnection to SMUX cards is identical (the number and meaning of bits may however differ according to the type of line).



The data is passed from/to the FES to the telecommunication line via the MUX and LIC as shown above. The LIC communicates with the FES to:

- Request new data to be transmitted (when in transmit mode)
- Signal 'transmit overrun': 'LIC line error register bit 3' (when in transmit mode)
- Signal 'transmit underrun': 'LIC line error register bit 3' (when in transmit mode)
- Signal 'overrun': 'LIC line error register bit 2' if more than 5 data bits are received between two serial link requests (when in receive mode).

LIC Reset

See “SMUX Reset” on page 4-48, and “LIC Reset” on page 4-50.

Line Enable/Disable

See “Line Enable/Disable” on page 4-50

Selective Scanning

See “Selective Scanning” on page 4-51.

LIC Swap

See “LIC Swap” on page 4-52, keeping in mind that LIC5s have only four logical addresses per SMUX card.

LIC Address Register Contents

In Write Mode		In Read Mode	
Bits	**Meanings**	**Bits**	**Meanings**
0	LIC logical address bit 0	0	LIC wired address bit 0
1	LIC logical address bit 1	1	LIC wired address bit 1
2	LIC logical address bit 2	2	LIC wired address bit 2
3	Enable/disable logical add	3	Odd position
4	(Not used)	4	EC number
5	(Not used)	5	EC number

LIC Control Register

The LIC control register X'02' bits 1 and 3 (line enable E0 and E1) controls the swapping.

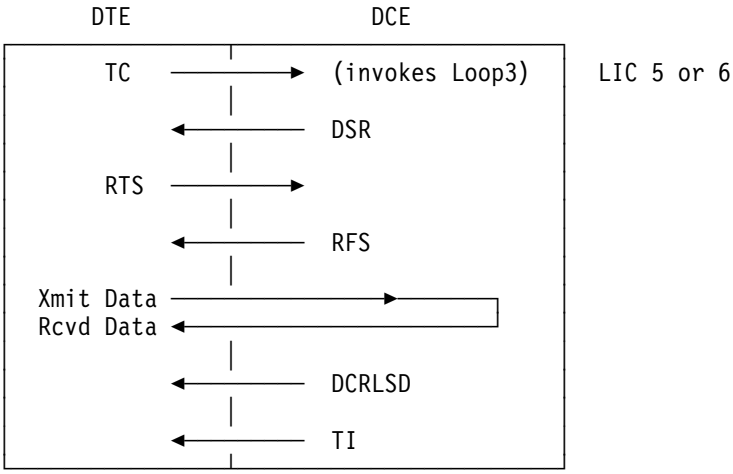
Bits	Meaning
0	(Not used)
1	Line enable E0
2	(Not used)
3	Line enable E1
4	(Not used)
5	Transmit bit echo

LIC Wraps

Refer to “Problem Determination Aids for LIC1s to LIC4s” on page 4-205 for more information on wraps and to the *Advanced Operations Guide*, SA33-0097 to invoke these functions from the MOSS console.

Loop 3 on V.24

Loop 3 on the V.24 interface performs the following wraps:



Loop 3 is performed between the transmitter output and the receiver input (before the line transformers) in the DCE part of LIC5s and LIC6s.

A 700-ohm load is maintained on the line during Loop 3. Loop 3 is started by test control (TC) rise. The DCE answers back by raising test indicator (TI), then starts data looping.

LICs Hot Plugging

The bottom connector of the LIC card has three levels of indentation to provide the required power sequences. When plugged power ON, the LIC logic goes into the reset state long enough to avoid transient disturbances on the interfaces.

LIC Type 5 DCE Function

Maintenance Approach

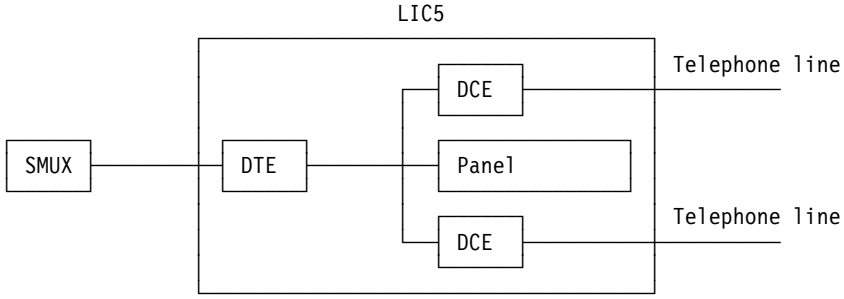
Four basic methods are used to identify network/link problems or DCE failures:

1. Link problem determination aids (LPDA-2) which is a hardware function implemented in each LIC5 DCE.

   LPDA-2 is used in conjunction with the NetView program and console at the host location. LPDA-2 commands and report messages are given in "LPDA Description", SY33-2064.
2. MOSS wrap tests.
3. Diagnostics invoked from the MOSS console.
4. Manual tests from 5869 portable keypad display (PKD).

For details, see “Problem Determination Aids for LIC5s and LIC6s” on page 4-209, and appropriate 786X and 5822 documentation listed in the MIP bibliography.

Data Flow



Logic Part

- DTE serializer/deserializer
- DCE microprocessor and signal processor
- DCE ROS, RAM, and NVPROM.

Analog Part

- DCE coder/decoder
- DCE transmit/receive filters
- DCE line transformers.

Speeds

Each LIC5 houses two DCEs which can operate over non-switched 4-wire telephone lines at:

- 4800 bps, (2400 bps back-up) or
- 9600 bps, (7200 bps back-up) or
- 14 400 bps, (12 000 bps back-up).

In the event of severe degradation, due to temporary line problems, the back-up speed may be used.

In a multipoint network, the back-up inbound speed may be required for only one or several drops, while the other drops continue to operate at full speed.

In the unlikely event of severe permanent line problems, due for example to a high level of non-linear distortion, the customer may require a deconditioning.

Speed Setting

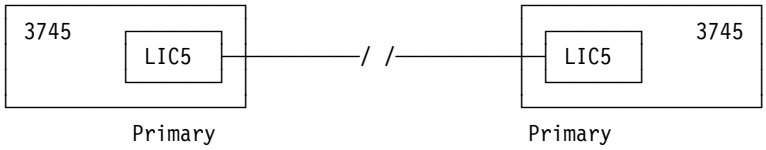
The speed is set at LIC installation at the PKD, and can be different for each DCE of a given LIC5.

The speed setting cannot be done either by NetView or by the MOSS.

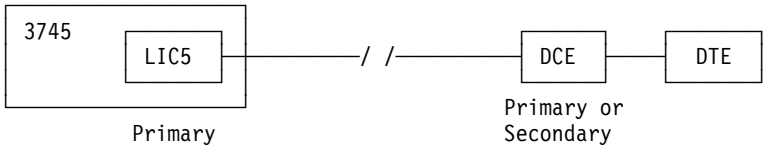
Configurations

LIC5 DCEs are compatible with IBM 586X and 786X DCEs. They operate in point-to-point or multipoint configurations as follows.

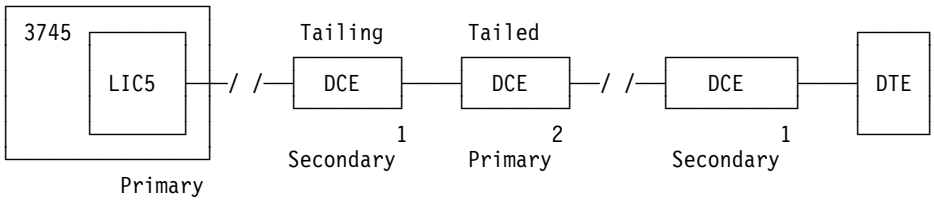
Point-to-Point - LIC5 to LIC5



Point-to-Point - LIC5 to 586X or 786X

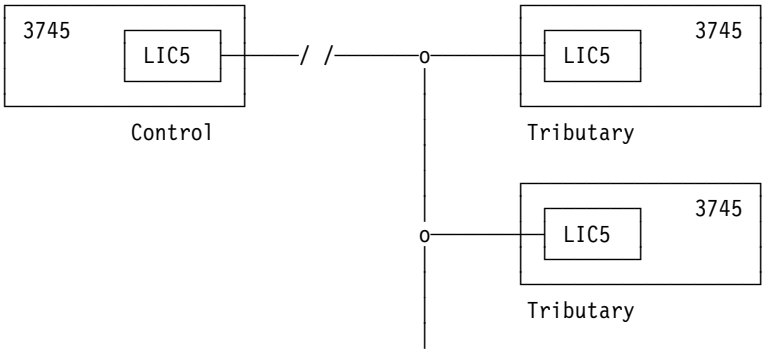


Point-to-Point - LIC5 to Tailed 586X

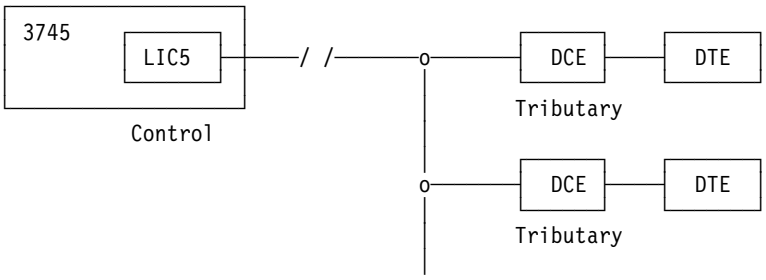


1. Transmit clock = received
2. Transmit clock = external
   Speed control = DTE.

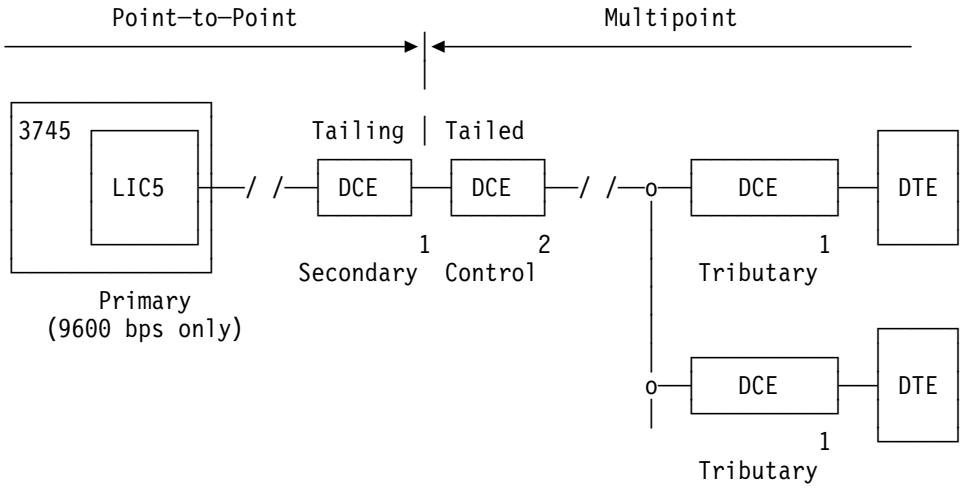
Multipoint - LIC5 to LIC5s



Multipoint - LIC5 to 586Xs



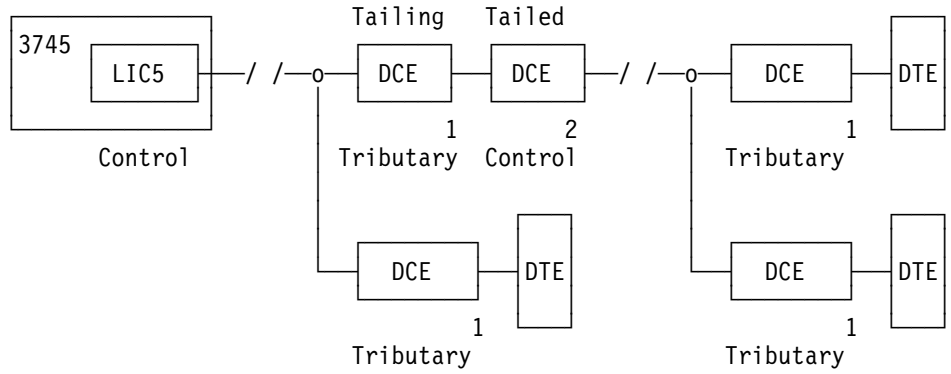
Multipoint - LIC5 to One Tailed 586X



1. Transmit clock = received
2. Transmit clock = external
   Speed control = DTE.

Multipoint - LIC5 to 586Xs (Including Tailed)

This configuration does not support LPDA2.



1. Transmit clock = received
2. Transmit clock = external
   Speed control = DTE.

Configuration Options

Depending on what type of modulation is used (IBM native, or CCITT), the different ways of setting the various CNM functions are:

CNM Functions	Modulation		Settable by:		
	IBM Native	CCITT	NetView	PKD	MOSS
Manual commands	Yes	Local	No	Yes	No
Local Wrap (Loop 3)	Yes	Yes	No	Yes	Yes
Remote Wrap (Loop 2)	Yes	Yes	No	Yes	No
Local Self Test	Yes	Yes	Yes	Yes	Yes
LPDA-2	Yes	Local	Yes	No	No
Sense/Operate Contacts	Remote	No	Yes	Yes	No

1. Although a LIC5 has no 'sense/operate' contact feature, it is possible to have these functions implemented in the remote 586X, and to use them through a LIC5.

Data Encoding and Modulation

LIC5s use combined amplitude and bi-phase differential modulation encoding. Each couple (phase, amplitude) corresponds to a single bit pattern.

In addition, the data is scrambled/descrambled to avoid single frequencies over the telephone line when repetitive data patterns appear at the DCE interface.

Below are the:

- Modulation rate
- Carrier frequency
- Number of encoded bits per signaling period
- Modulation type.

For the configurations A to E shown in the following table:

	A	B	C	D	E	F	G
14 400 bps	*	*					
9600 bps			*	*	*		
4800 bps						*	*
Native	*		*	*		*	
CCITT V.27 bis							*
CCITT V.33		*					
CCITT V.29					*		
Pt–to–Pt	*	*		*	*	*	*
Multipt. Inbound			*	*		*	*
Multipt. Outbound	*			*		*	*

A. Native Mode

Speed	14 400 bps	12 000 bps
Modulation Rate	2400	2400
Carrier Frequency	1700	1700
Number of encoded bits per signalling periods	6	5
Modulation	QAM trellis coded	QAM trellis coded
RTS/RFS Delay	2 ms	2 ms

B. CCITT Mode

Speed	14 400 bps	12 000 bps
Modulation Rate	2400	2400
Carrier Frequency	1800	1800
Number of encoded bits per signalling periods	6	5
Modulation	QAM V.33	QAM V.33
RTS/RFS Delay	2 ms	2 ms

C and D. Native Mode

Speed	9600 bps	7200 bps
Modulation Rate	2400	2400
Carrier Frequency	1700	1700
Number of encoded bits per signalling periods	4	3
Modulation	QAM or QAM with TCM	QAM or QAM with TCM
RTS/RFS Delay	2 ms	2 ms

E. CCITT Mode

Speed	9600 bps	7200 bps	4800 bps
Modulation Rate	2400	2400	2400
Carrier Frequency	1700	1700	1700
Number of encoded bits per signalling periods	4	3	2
Modulation	QAM V.29	QAM V.29	QAM V.29
RTS/RFS Delay	2 ms	2 ms	2 ms

F. Native Mode

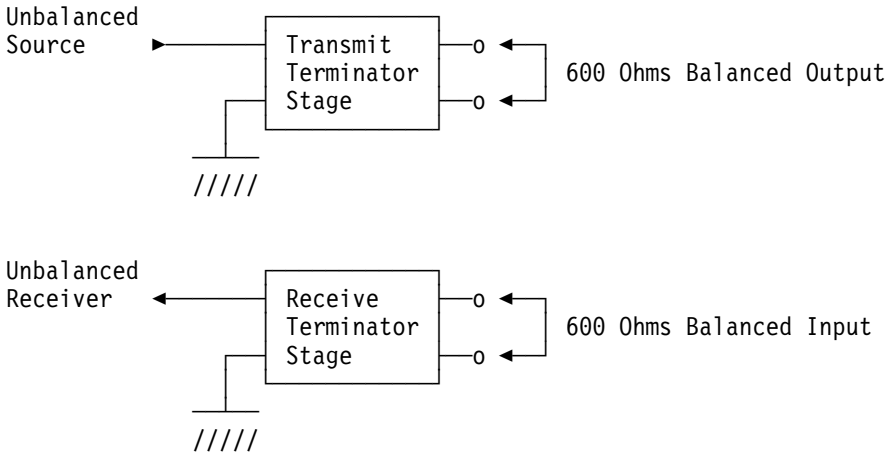
Speed	4800 bps	2400 bps
Modulation Rate	2400	2400
Carrier Frequency	1700	1700
Number of encoded bits per signalling periods	2	1
Modulation	4–phase differential encoding	4–phase differential encoding with TCM
RTS/RFS Delay	2 ms	2 ms

G. CCITT Mode

Speed	4800 bps	2400 bps
Modulation Rate	1600	1200
Carrier Frequency	1800	1800
Number of encoded bits per signalling periods	3	2
Modulation	8–phase differential encoding	4–phase differential encoding
RTS/RFS Delay	2 ms	2 ms

DCE to Telephone Line Interface

LIC5 interfaces the telephone line through balanced impedances matching the networks (both input and output circuitries may be regarded as 2-port networks).



The circuits are not damaged:

- Under open circuit condition
- By a short circuit between the leads
- By a short circuit from either lead to ground.

The DC isolation between input and output leads with regard to ground is greater than 20 MΩ.

Surge Protection

Primary protection

A telephone line surge protection (carbon block or gas tube) should also be provided by the line connector before the DCE wall plug.

Secondary protection

Three protection devices connected from tip to frame ground, from ring to frame ground, and tip to ring.

In the countries where it is authorized, this limits the maximum voltage to 80 V peak (line-to-ground) or 80 V peak (line-to-line). In addition, the transformer saturation characteristics, and the Zener diode network across the line transformer secondary windings, limit the maximum peak voltage to 12 V (line-to-ground).

Transit Time

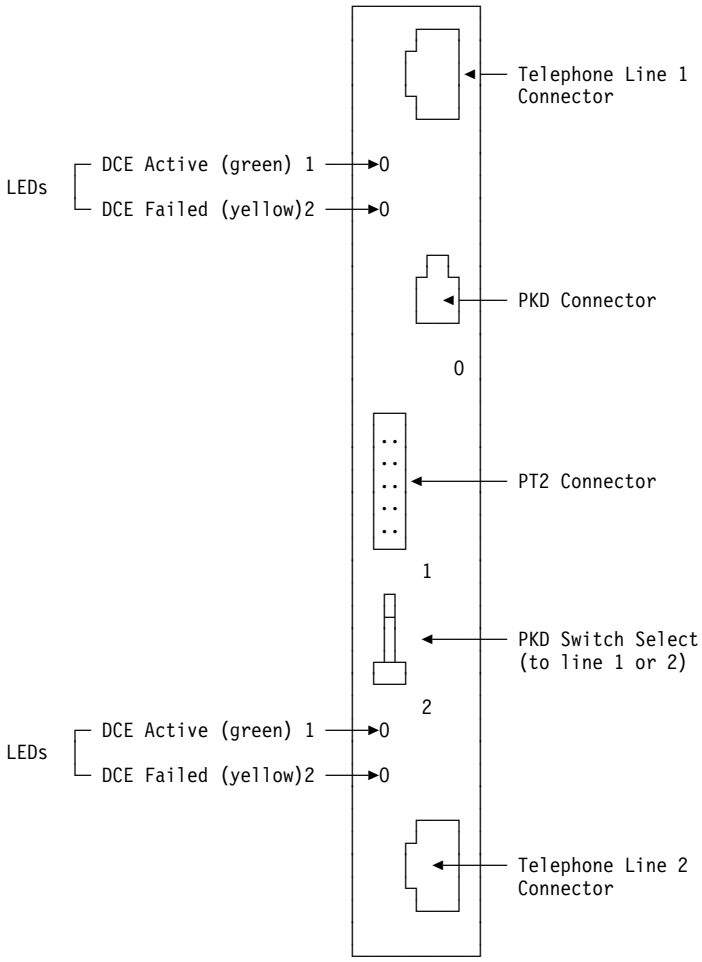
The transit time is the time that elapses between the input of a bit in the local transmitter and the output of this bit from the remote receiver, assuming a zero transmission delay over the telephone line.

Modulation Type	Transit Time (ms)					
	14 400	12 000	9600	7200	4800	2400
IBM Native	21.4	21.4	17.2	18.0		
CCITT V.33	21.4	21.4				
IBM Native			18.0	18.0		
CCITT V.29			16.8	16.8	16.8	
IBM Native					17.4	21.4
CCITT V.27 bis					12.2	15.6

RFS Delay

The RFS delay is 2 ms for a LIC5 in any configuration. It must be added to the transit time to evaluate the turn-around time.

LIC5 Panel



1 lit	DTR is ON (green LED)
2 lit	Severe local DCE error is detected (yellow LED)
1 and 2 flashing	LIC card plugged in a wrong place

Line Specifications

- 4-wire non-switched lines
- US and Canada: non-conditioned
- Other countries: CCITT M.1020 or M.1025 conditioning.

Line Spectrum

- V.27 bis
  - Centered on 1800 Hz
  - Spreads from 1000 to 2600 Hz.
- Native and V.29
  - Centered on 1700 Hz
  - Spreads from 450 to 3050 Hz, including a 12.5 % roll-off.
- V.33
  - Centered on 1800 Hz

– Spreads from 600 to 3000 Hz.

3002 Channel (US) Characteristics

Attenuation distortion (Overall loss relative to that at 1004 Hz):
-2 to + 8 dB from 500 to 2500 Hz
-3 to +12 dB from 300 to 3000 Hz

Delay distortion Less than 1750 μ from 800 to 2600 Hz

Insertion loss at 1004 Hz 16 dB

Non-linear distortion (H2) 25 dB minimum

Non-linear distortion (H3) 30 dB minimum

Phase jitter No more than 10° peak-to-peak

Frequency shift ± 5 Hz

Signal to noise ratio 24 dB

Impulse noise Threshold of -6 dB to signal level at an average rate of 15 impulses per 15 mm.

M.1020 Line Characteristics

Attenuation distortion (Overall loss relative to that at 800 Hz):
-2 to +6 dB from 300 to 500 Hz
-1 to +3 dB from 500 to 2800 Hz
-2 to +6 dB from 2800 to 3000 Hz

Delay distortion (Group delay relative to the minimum group delay):
Less than 500 μ from 1000 to 2600 Hz
Less than 1500 μ from 600 to 2600 Hz
Less than 3000 μ from 500 to 2800 Hz

Insertion loss at 800 Hz 13 dB ± 4

Harmonic distortion 25 dB minimum (below received level)

Phase jitter No more than 15° peak-to-peak (normally 10°.)

Frequency shift ± 5 Hz

Signal to noise ratio 24 dB

Impulse noise Threshold of -8 dB to signal level, at an average rate of 18 impulses per 15 mm.

M.1025 Line Characteristics

Attenuation distortion (Overall loss relative to that at 800 Hz):
-2 to +12 dB from 300 to 500 Hz
-2 to + 8 dB from 500 to 2500 Hz
-2 to +12 dB from 2500 to 3000 Hz

Delay distortion (Group delay relative to the minimum group delay):
Less than 300 μ from 600 to 2800 Hz
Less than 1500 μ from 1000 to 2600 Hz

Frequency error Less than ± 5 Hz

Insertion loss at 800 Hz 13 dB ± 4

Harmonic distortion 25 dB minimum (below received level)

Phase jitter No more than 15° peak-to-peak (normally 10°)

Frequency shift ± 5 Hz

Signal to noise ratio 24 dB

Impulse noise Threshold of -8 dB to signal level at an average rate of 18 impulses per 15 mm.

Specific Country Line Characteristics

In the following countries, the line characteristics are specified by the PTT:

- **France**

  The French PTT offer a 4-wire normal quality line with the following specifications:

  Attenuation distortion (Overall loss relative to that at 800 Hz):
  -2.6 to +4.5 dB from 500 to 2000 Hz
  -2.6 to +6.0 dB from 300 to 2600 Hz
  -3 to + 9 dB from 1700 to 2300 Hz
  -3 to +12 dB from 2300 to 2800 Hz
  Loss at 800 Hz: 6.4 dB, with a possible variation of less than 4.5 dB.

  Delay distortion (Group delay relative to the minimum group delay):
  Less than 1000 μ from 1000 to 2400 Hz
  Less than 1500 μ from 800 to 2600 Hz
  The dc loop resistance of a wholly metallic line is less than 4000 Ω.

- **Japan**

  The NTT offer a normal quality line (3.4 kHz service). According to NTT-supplied information, these lines should have the following specifications:

  Attenuation distortion (Overall loss relative to that at 800 Hz over carrier section):
  -3.8 to +13.0 dB from 300 to 400 Hz
  -3.8 to + 5.8 dB from 400 to 600 Hz
  -3.8 to + 3.8 dB from 600 to 2400 Hz
  -3.8 to + 9.4 dB from 2400 to 3000 Hz
  -3.8 to +17.4 dB from 3000 to 3400 Hz

  Delay distortion (Group delay relative to the minimum group delay):
  Less than 1750 μ from 1000 to 3000 Hz

- **UK**

  The Post Office provides a quality telephone line according to CCITT recommendation M.1025.

Options and Configurations

The options are entered from the PKD, using the 'CONF' command or via LPDA-2 commands. They are stored into a non-volatile RAM except for microcode and EC levels.

These options are:

- Read and set by customer
- Read and set by CE only
- Read only.

They can be read and set:

- Through the PKD
- Through the LPDA-2 commands
- In the local LIC type 5 DCE
- In the remote DCE (LIC type 5 or IBM 586X DCE).

The table below shows the various ways of reading and setting these options.

Keying 'LOCAL CONFIGURATION' will cause the DCE to display and scroll its own configuration field by field; the operator may update each configuration field which appears on the display.

If the operator does not update the configuration, TI is NOT raised and data traffic can take place without interruption.

If the operator updates the configuration, (keying 'ERASE'), TI is raised, CD and RFS are dropped at local interface, and the **data traffic through the DCE is interrupted**.

Keying 'REMOTE CONFIGURATION' causes the DCE to display and scroll the configuration of the selected remote DCE.

During the operation, TI is raised, CD and RFS are dropped at the local and the remote interface, and the data traffic through the DCE is interrupted.

Options	Settable in the local LIC5		Settable in the Remote LIC5 (if not CCITT)	
	PKD	LPDA-2	PKD	LPDA-2
DCE address	*		*	
Default speed	*	*	*	*
Pt/Pt - Mpt	*	*	*	*
Control - tributary	*	*	*	*
Type: IBM native	*		*	
Long training seq.	*	*	*	*
Anti streaming	*	*	*	*
Xmit clock control	*	*	*	*
RFS delay	*	*	*	*
Line quality threshold	*	*	*	*
Rcve level threshold	*	*	*	*
Hit count threshold		*		*
Nonsw. Transmit level	⌑			
CCITT	⌑			
CD sensitivity	⌑			
LPDA-1 enable				
LPDA-2 enable	*		*	
2nd back-up speed	*	*	*	*
Auto self test	*	*	*	*
Switched Xmit level				
Auto-answer				
Ring protection				
Auto-disconnection				
Telephone numbers				
Serial number				
Base card EC level	Δ	Δ		
Machine EC level				
Microcode EC levels	Δ	Δ		
Customer information		*		*

* Read and set by customer
⌑ Set by CE only
Δ Read-only.

Note: As options and some other configuration items can be set either locally or remotely, contentions may occur. The last configuration received, either from the line or from the attached operator panel, overrides the previous one.

Some of the above options are self explanatory; the others are explained hereafter.

DCE Address

- Control and primary LIC5s: always 01
- Tributary and secondary LIC5s: any value except 00, FC, FD, FE and FF.

Default Speed

The non-volatile RAM holds the default speed indication, defined at configuration time, which is used at each power ON.

Point-to-Point/Multipoint
LIC5 can be 'primary', 'control', 'secondary', or 'tributary'.

Transmit Clock Control
Two options are available:

Internal clock The transmit clock is provided internally by the LIC5.

Receive clock The local transmit clock is locked onto the receive clock (decoded from the received data).

Line Quality Threshold
If the line quality parameter is greater than or equal to that threshold, the line quality indication 'LQ' in the background information blinks on the displayed value, and the buzzer gives an audible alarm.

The threshold value ranges from 0 to 15. Background display line quality is in hexadecimal:

```
0 1 2 3 4 5 6 7 8 9 A B C D E F
```

(At installation, the threshold value is 8, which corresponds to a 10^{-5} bit error rate.)

LPDA-2 setting ranges from 0 to E, panel setting from 0 to F. F means 'no threshold'.

Receive Level Threshold
This is to specify the threshold above which a warning indication will be reported during LPDA-2 modem and line status report. This value ranges from 0 to -43 dBm.

Carrier Detector Sensitivity
Two sensitivities are provided:

Low CD sensitivity Received signal below 31 dBm is not detected
Normal CD sensitivity Received signal is detected down to 43 dBm.

LPDA-2 Hit Count Threshold
- This value ranges from 0 to 64.
- LPDA-2 setting ranges from 0 to 63. (64 meaning is 'no threshold').
- This field cannot be accessed from the panel.

Transmit Level
See SMUX A/B section for authorized levels and settings.

CCITT
Applied to point-to-point, makes the LIC5 compatible with CCITT V.27 bis, V.29 or V.33 recommendation for 4800, 9600 or 14 400 bps.

LPDA-2 Enabled
- If enabled (default option) the DCE intercepts and executes LPDA-2 commands.
- If disabled, the DCE ignores LPDA-2 commands.
- Since LPDA-2 commands flow into the DCE like other pieces of data, the disable option may be selected if there is a chance that the LPDA-2 header

may be erroneously detected in the data bit stream. The LPDA-2 header is guaranteed unique for the following data transmission protocols:

- SDLC NRZI
- BSC USACII or EBCDIC
- ALC.

First/Second Back-Up Speed

Only used with CCITT V.29 option, to specify whether 7200 or 4800 bps back-up speed is used.

Card EC Level

One digit, between 0 and 3, wired on the LIC5 card, that specifies the level of the electronic components.

Microcode EC Level

The EC level of the ROS and UVPROMs can be read onto the PKD from the ROS. They cannot be updated.

Host Support

Host support for LIC5s is NetView from R3, using LPDA-2 functions. See *LPDA Description,* SY33-2064 for LPDA-2 protocols, formats, and commands. Three sets of commands are available for:

- Problem determination
- DCE configuration
- Testing from the TSS.

Problem Determination Commands

Supported commands are:

- DCE status and test
- Line status
- Transmit/receive test
- Line analysis.

DCE Configuration Commands

The following 'operational commands' are supported:

- Read local configuration
- Write local configuration
- Set local transmit speed
- Read remote configuration
- Write remote configuration
- Set remote transmit speed
- Remote contact sense/operate.

Note: The following commands are **not supported**:

- Call-out
- Disconnect
- Local contact sense/operate in local LIC5
- Read local coupler
- Read remote coupler
- Write local coupler

- Write remote coupler.

TSS Commands

Two commands can be initiated from the TSS (FESA) to test the LIC5s:

- CCITT loop-3 (with or without line wrap block)
- Self-test.

CCITT Loop-3

This test is initiated by the 3745 TSS (FESA) on the DTE interface. The FESA has to detect RFS going ON before sending the data to be looped.

For security purposes, the FESA can set up a timer (2100 ms maximum) to guard against no answer from a failing DCE.

The TSS/FESA follows the following sequence:

- Start loop:
  1. Put RTS OFF
  2. Detect RFS OFF in less than 50 ms
  3. Set TC ON
  4. Detect TI ON in less than 700 ms
  5. Set RTS ON
  6. Detect RFS ON in less than 200 ms
  7. Send data to be looped on TD.
- End loop:
  1. Stop data transmission
  2. Put RTS OFF
  3. Detect RFS OFF in less than 50 ms
  4. Put TC OFF
  5. Detect TI OFF in less than 100 ms.

Self Test

This test is achieved without line wrap plug for a given line.

The self-test from offline diagnostics preempts any other DCE functions. It is intended to be run when the DCE is not connected to the network.

- The 'modem failed' bit is set to 1 in case of error.
- The 'modem busy' bit is raised solely as an answer to the self-test request from the 3745.

The test sequence is as follows:

1. Read interface:
   - 'Modem failed' bit ON = error
   - 'Modem busy' bit staying ON for more than 4 s = error.
2. Set 'self-test request' ON:
   'Modem busy' should come ON in less than 200 ms.
3. Put 'self-test request' OFF (to avoid continuous self-test):
   - 'Modem busy' should come OFF in less than 4 s.
   - 'Modem failed' OFF = self-test successful.

Manual Tests

The following manual tests are all initiated from the PKD:

	Data Disruptive
Local loop back	Yes[1]
Remote loop back	Yes[1]
Local self-test	Yes[1]
Local status	No
Remote self-test	Yes
Remote status	Yes
Digital test (transmit/receive test)	Yes[1]
Analog test (line analysis)	Yes

[1] Run continuously until you press 'EXIT'.

Descriptions of the above manual tests are given later in this chapter, under 'Problem Determination Aids' for LIC5s/LIC6s.

Alarm Tone Detection

A failure tone is sent when a hard internal failure is detected. However, LIC5 DCEs detect both:

- Remote power OFF tones
- Remote failure tones.

Alarm tones are not detected if the DCE is executing a self-test.

If a failure tone and a power OFF tone are detected while executing a local status, only one of them is displayed.

Tone Characteristics

Frequency 325 Hz ± 10 Hz

Level As written in NVRAM (default value provided by the switches on the SMUX card)

Power OFF tone duration

- 100 ms ± 20 ms if power OFF lasts more than 100 ms
- Equals the power OFF duration if power OFF lasts less than 100 ms.

Failure tone duration

300 ms (repeated every 90 s until the DCE is powered OFF or the internal error disappears).

Tone Reception

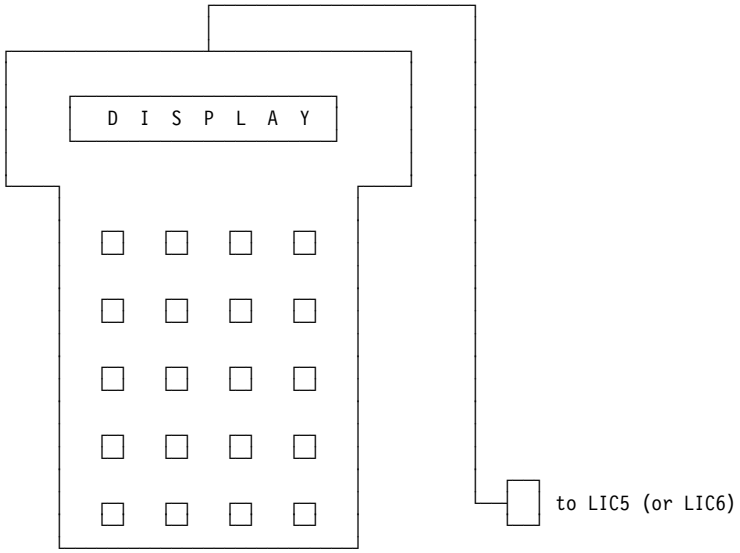
The detection is controlled by the microprocessor which monitors the tone duration in order to differentiate the power OFF tone from the failure tone.

DCE Configuration

DCE (LIC5 or 586X) configuration (local or remote) is achieved by keying a set of commands from the IBM 5869 PKD connected to the relevant LIC5. See the *Connection and Integration Guide*, SA33-0129 for detailed command procedures, except for CE procedures, which are described in the *MIP*, SY33-2054 appendix B.

Portable Keypad Display (PKD)

The IBM 5869 PKD consists of a keyboard with 20 keys, associated with a 16-character alphanumeric display, and an audible alarm.



KEYPAD

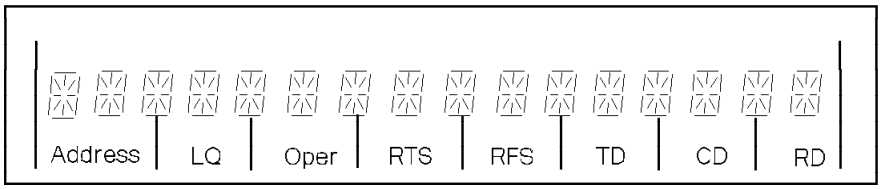
	TEST	STATUS	SPEED	CONFIG
LOC	0	1	2	3
	TEST	STATUS	FULL	CONFIG
REM	4	5	6	7
	ANALOG	DIGITAL	BCKUP	CMD
	8	9	A	B
	PD			LOC. LOOP
	C	D	E	F
	GO	ERASE	EXIT	STOP

The following are the main display operations available. For procedures, display analysis, and actions, refer to:

- *3745 Problem Determination Guide*, SA33-0096
- *3745 Connection and Integration Guide*, SA33-0129.

Lamp Test

The 'GO' key displays all positions during 5 s on the screen to test the LEDs.



A specific key display can also be tested (by keeping that key pressed longer than 5 s).

Background Information

This is the default information that appears on the screen in normal mode.

From Left to Right

- LPDA2 address (2 characters): always 01
- LINE QUALITY Irrelevant=X: 0 to F (0 is the best)
- OPERATE Off=X: L=Non-switched, W=Local Wrap via TC
- RTS OFF=0 ON= 1
- RFS OFF=0 ON= 1
- CD OFF=0 ON=1
- TD blinks on TD activity, and also indicates the speed of transmission: F = full, B = backup
- RD blinks on RD activity, an also indicates the speed of reception: F = full, B = backup.

Note:

- 'WRAP' is displayed instead of line address and line quality if a manual loop back test is running.
  - Transitions between 0 and 1 on the screen indicate that activity is taking place on the lead (except for RD and TD).
  - If there is no activity the actual status is displayed.
- When CD = 0, RD indicates the speed of last data reception.
- When RFS= 0, TD indicates the speed of last data transmission.

DCE Information

When the background information is displayed, the operator can obtain the following DCE main information:

When pressing the ERASE key: 'aaaa bbb cc' appears on the display

aaaa 4800 bps or 9600 bps or 14 400 bps or V.27 or V.29 or V.33

bbb Transmit clock option

- INT for internal (from local)
- RCV for received (from remote).

cc Network configuration

- PP for point-to-point primary
- PS for point-to-point secondary
- MC for multipoint control
- MT for multipoint tributary
- MT for CCITT V.29 or V.33.

As long as the operator keeps pressing the ERASE key, the DCE information is displayed.

Releasing the ERASE key returns to background display. This operation is not data-disruptive.

LIC 5 Physical Address

When the background information is displayed, press the EXIT key for more than 0.5s. The LIC physical position on the board is then displayed.

POR - Bring-Up Information

At power ON reset time all the segments on the screen are lit ('English flag'). Then 'COPYRIGHT IBM 88' appears on the screen.

Normally, after the initial self-test is completed, the screen displays the background information.

In case of a severe problem the 'English flags' remain on the screen. Otherwise, the DCE goes to operate and this is the normal case.

If the initial self test detects a severe error, the message:

```
LIC 5 FAILED
```

appears on the screen during 2 s and the DCE loops on bring-up.

Keying Procedures

Each function is performed in three steps:

1. Selection
2. Execution
3. Report.

Command Rejection

In some cases commands are rejected:

NO RESPONSE For some reason the remote did not answer, disruption of data transmission has already taken place.

BAD RESPONSE The remote gave an invalid answer (wrong FCS), disruption of data has already taken place.

BUSY TC ON If the lead TC is ON, all operator commands are rejected with the following message: BUSY TC ON. The buzzer sounds 1 beep and the message stays on the screen until the operator presses EXIT. There is no disruption of data.

NOT EXECUTED The command can also be rejected with the 'NOT EXECUTED' message. Either it was a remote command and the DCE is in CCITT mode, or the DCE is continuously busy with host commands (this may be an abnormal condition). If the message is caused by CCITT mode, there is no disruption of data.

A remote speed change is not executed if the clock option of the remote DCE is not set to internal clock.

The buzzer sends the audible warning at the beginning of the report.

In report step, pressing a function key causes return to selection step. This is a means to chain several commands without being pre-empted by commands coming from the host or the line (see contentions).

Self-Tests

The following self-tests are available:

- Local self-test (key 0)
- Remote self-test (key 4).

Status

The following status can be examined:

- Local status (key 1): Not disruptive but forbidding LPDA-2 commands, it informs on:
  - Logged warnings
  - Line quality and received level in dBm
  - Hit count since the last 15 minutes
  - DTE interface local status and transitions
- Remote status (key 5): **Disruptive**.
  - Logged warnings
  - Line quality and received level in dBm
  - Hit count since the last 15 minutes
  - DTE interface local status and transitions

Analog Test

This test (key 8) provides line analysis. It involves both local and remote DCEs and lasts 6 s at each side.

Digital Test

This test (key 9) is a transmit/receive test. It involves both the local and remote DCEs.

Blocks of data are sent from the local to the remote DTE which wraps them back to the local one.

Block errors are counted on both sides and displayed on both screens. See page 4-213.

Local Loop

This command (key F) prepares the DCE for a Loop-3 test. See 4-59.

Speed Change

This option allows to locally and/or remotely change the speed from nominal to back-up and conversely.

The speed cannot be changed if the remote DCE:

- Has the DSRS option
- Already runs at the requested speed

Configuration

The PKD being connected to a given DCE, the local DCE or the remote DCE configuration settings may be:

- Scrolled and displayed
- Updated.

Some fields are modifiable by the CE only, some other fields are read-only (for example, model).

If vital fields have been modified, returning to background causes a self-test to take place.

Below are the various configuration fields for local LIC5s:

- DCE address
- DCE type
- Modulation (IBM native/CCITT)
- Network configuration (primary/control/secondary/tributary)
- Transmit clock (internal/received)
- Fast multipoint
- 9600 trellis coded
- Preemphasis
- Long training sequence
- RFS delay
- Auto self test
- Anti streaming
- Transmit level (from 0 to -15)
- Carrier detector sensitibity (low/normal)
- Network services (LPDA-2 enabled/disabled)
- Line quality threshold (from 0 to 15)
- Receive level threshold (from 0 to -43)
- Second backup speed (7200/4800): CCITT only
- Default speed
- Buzzer control
- Machine level
- LIC EC level
- Microcode EC level

Contact Sense/Operate

These facilities are not available on LIC5s, but on remote 586Xs only. They are:

- Open the 'contact operate' relay
- Close the 'contact operate' relay
- Get the status of the 'contact operate' and 'contact sense'.

Commands

The following commands can be executed in CE mode only:

- Send a 1004 Hz tone on the telephone line.
- Load default configuration (transmit level not changed).
- Update the configuration (all fields may be updated).
- Address a specific DCE via its serial number.
- Long timer (10 minutes) for LLAP.
- Contact sense/operate (remote only)

All the above commands are reset at:

- Power OFF
- DCE re-initialization.

Buzzer Control

Each time a valid key is pressed there is a brief beep. The absence of beep means that the key is either irrelevant to the current protocol or has not been taken into account by the keypad hardware.

Contentions

A request to execute an LPDA-2 command can come from:

- The local host
- The remote via the telephone line
- The panel.

Contentions are solved on a first request/first to be served basis.

From the time the GO key is released until the end of the test, the DCE does not answer commands either from the line or from the DTE.

While executing a non-disruptive command the DCE does not answer LPDA requests from the host or from the line.

Re-synchronization is inhibited for remote commands.

Unsolicited Messages

These messages appear on the screen, without any operator intervention. If a PKD operator session is in progress the unsolicited messages are delayed. They can appear only when the screen displays background information. For complete information, refer to the *Configuration and Integration Guide*.

CMD FROM LINE (2 s)
CMD FROM DTE (2 s)
REM MODEM FAILED
Stays on screen until the operator presses EXIT. This message is not displayed if the PKD was not present when the condition occurred.
REM PWR LOSS In point-to-point, this message remains until CD goes ON or the operator presses EXIT. It appears as soon as the PKD is present if CD is still 0.
CONFIG FROM LINE
When the DCE is being configured from the line or from the host.
CONFIG FROM HOST
Disappears at end of configuration, or if a power loss or failure tone is detected. If end of configuration has not been received the message stays on the screen during 5 mm. This message appears as soon as the PKD is present if the condition still holds.
CONFIG MISMATCH
Configuration error.
KEY n STUCK When the indicated key appears to be pressed during more than 5 s. The message stays 10 s then the control panel is reinitialized. This indicates a mechanical or electrical problem.
aa LIC5 FAILED At power ON, the initial self-test failed. If the operator presses GO, the DCE attempts to start.
TEST FROM HOST A test from the 3745 has been initiated.
WRONG SLOT The cassette has been plugged in a wrong position.
TEST FAILED A host self-test has failed.
SELF TEST FAILED A self-test failed after a configuration change.
TEST OK A self-test requested by the host was successful.
SELF TEST OK A self-test was successful after a configuration change.
TEST OK NOWRP A manual self-test without tel wrap plug was successful.
TEST OK WRAP A manual self-test with tel wrap plug was successful.

PT2/3

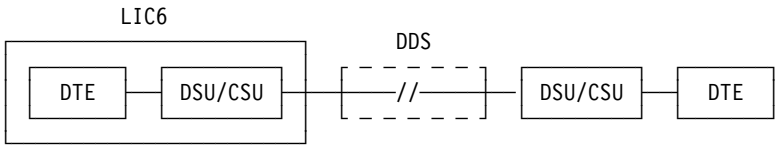
A 10-pin connector is available on the LIC5 panel to connect a PT2/3 used to investigate and record control and data signals.

LIC Type 6 DSU/CSU Function

DSU/CSU stands for: data service unit/channel service unit, which is in LIC6, the equivalent of the DCE function of a LIC5.

Connection to US DDS

The DSU/CSU allows DTE-to-DTE communication through the digital data service (DDS) in the US.



Limited Distance Connection

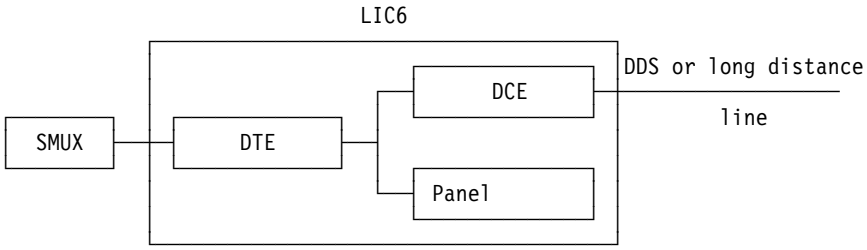
The DSU/CSU also allows DTE-to-DTE communication through private limited distance lines. Even though the customer-owned line is only two metallic pairs, the data is encoded and decoded as for DDS (protocols, rules, and so on).

Note: The LIC6 offers no local area data channel (LADC) attachment facility.

Maintenance Approach

Same as LIC5; see page 4-61.

Data Flow



Logic part:

- DTE serializer/deserializer
- DCE microprocessor and signal converter
- DCE ROS, RAM, and EEPROM.

Analog part:

- DCE coder/decoder
- DCE transmit/receive filters
- DCE line transformers.

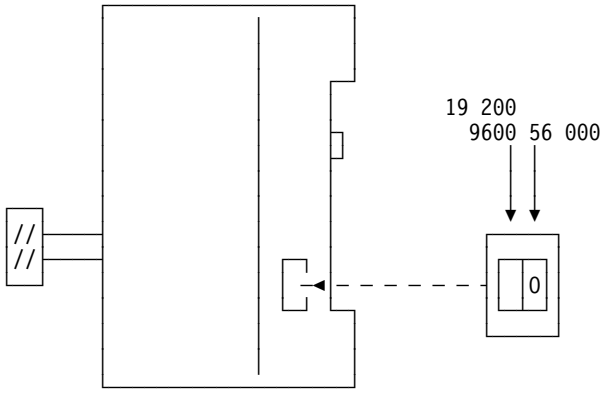
Speeds

Each LIC6 houses one DCE which can operate at the following speeds, depending on the network it is connected to:

- US digital data service network (DDS)
  - 56 000 bps
  - 19 200 bps
  - 9600 bps
- Non-switched 4-wire limited distance lines
  - 56 000 bps
  - 19 200 bps
  - 9600 bps.

Speed Setting

The speed is set at installation time from a microswitch on the LIC6 card.



In V.35-like mode only one speed is available from the switch: 56 000 bps.

In V.24-like mode two speeds are available from the other position of the switch: 19 200 and 9600 bps. One of these two speeds must be set from the PKD at installation time.

The speed setting cannot be changed either by NetView or by the MOSS.

Configurations

LIC6 DSU/CSUs are compatible with IBM 5822-10 DSU/CSUs. They operate in:

- Point-to-point and multipoint when connected to DDS
- Point-to-point only when connected to a limited distance line.

Configuration Options

The different ways of setting the CNM functions are:

CNM Function	Settable by:		
	NetView	PKD	MOSS
Manual Command	No	Yes	No
Local Wrap (Loop 3)	No	Yes	Yes
Local Self Test	Yes	Yes	Yes
LPDA-2	No	No	No

Data Format

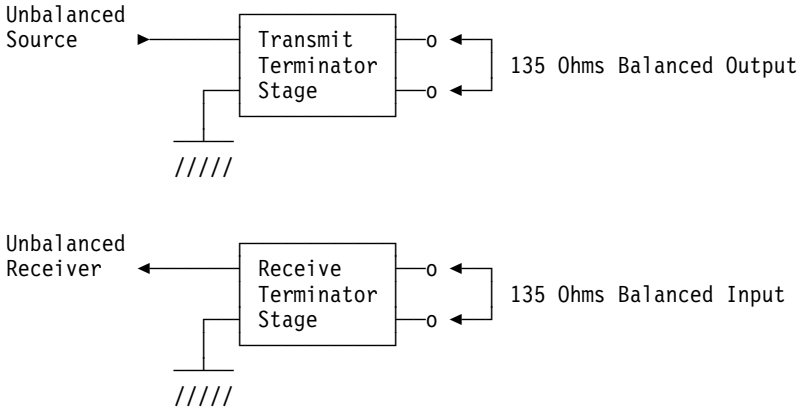
Synchronous, binary serial.

Modulation Technique

Bipolar, return-to-zero.

DSU/CSU to Line Interface

LIC6 interfaces the DDS/LDM through balanced impedances matching the networks (both input and output circuitries may be regarded as 2-port networks).



The circuits are not damaged:

- Under open circuit condition
- By a short circuit between the leads
- By a short circuit from either lead to ground.

The DC isolation between input and output leads with regard to ground is greater than 20 MΩ.

Surge Protection

Primary protection

A line surge protection (carbon block or gas tube) should also be provided by the line connector before the DCE wall plug.

Secondary protection

One protection device connected from tip to ring and two capacitors, from tip to frame ground, and from ring to frame ground.

This limits the maximum voltage to 80 V peak (line-to-line).

Transit Time

The transit time is the time that elapses between the input of a bit in the local transmitter and the output of this bit from the remote receiver, assuming a zero transmission delay over the telephone line.

Transmitter and receiver refer to the V.24 interface.

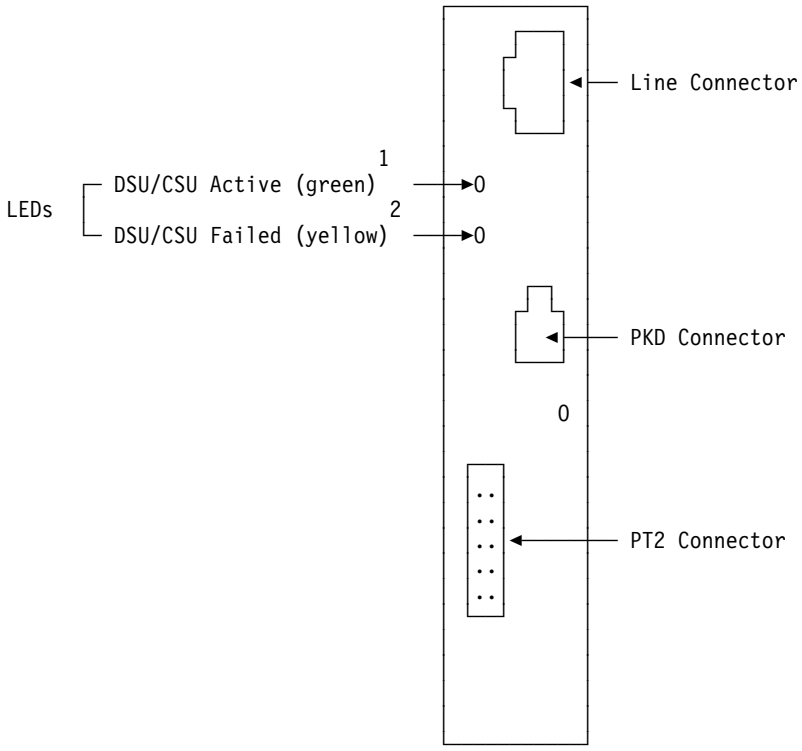
	Transmission Speed (bps)		
	56 000	**19 200**	**9600**
Transit Time (ms)	35	33	33

RFS Delay

The RFS delay is from 7 to 20 bit-time for LIC6 in any configuration. It must be added to the transit time to evaluate the turn-around time.

- 9600 bps: 2.5 ms
- 19 200 bps: 1.5 ms
- 56 000 bps: 0.5 ms

LIC Type 6 Panel



1 lit	DTR is ON (green LED)
2 lit	Severe local DCE error is detected (yellow LED)
1 and 2 flashing	LIC card plugged in a wrong place

Line Specifications

- DDS network: refer to DDS documentation
- Limited distance connection: the line specification depends on the length and the size of the wires.

Lengths and Gauges

Below are the maximum lengths in km (and miles) for the most common gauges used:

Transmission speeds (bps)	Wire Diameter / mm (Gauge)			
	0.4 (26)	**0.5 (24)**	**0.6 (22)**	**0.8 (20)**
56 000	4.2 (2.6)	6.0 (3.7)	8.1 (5.0)	13.7 (8.5)
19 200	5.8 (3.6)	7.9 (4.9)	10.2 (6.3)	15.7 (9.7)
9600	7.3 (4.5)	9.8 (6.0)	12.6 (7.8)	18.7 (11.6)

Note: The most commonly used lines are 0.4 and 0.6 mm.

The distances given in the above table (in kilometers and miles) are calculated for 34 dB of attenuation at the Nyquist frequency and associated with the following line parameters:

Line ic capacitor 50 nF / km
Line ic inductance 650 μHenry / km
Line ic resistor 44/(DxD) in μΩ / km with D = line diameter in mm
Load impedance 135 μΩ (resistive).

Using an IBM cabling system type 1 (cable PN 4716748) or type 6 (cable PN 4716743) the expected distances will be:

- 4 km up to 19200 bps
- 3 km at 56000 bps.

On loops which meet the noise requirements defined in the *Bell PUB 62310* the bit error rate will not exceed 4/100 000.

At data rate over 19 200 bps, lines with a diameter greater than 0.6 mm will increase the group delay distortion.

Options and Configurations

The LIC6 is **not** configurable via LPDA-2 commands.

The speed option (V.35/V.24) is set from a switch on each LIC6 card but the speed option (19 200/9600) is set from the PKD. See “Speed Setting” on page 4-87.

The options are set in a non-volatile PROM, except for microcode and machine EC level.

The table below shows the options available for local LIC6 to both customer and CE.

Options	Local LIC6
Point-to-point / Multipoint	Yes
DSU/CSU - limited distance	Yes
Timing source	Yes
Network services[1]	Yes
Byte 1 (speed V.35/V.24)	Switch
Speed 19 200/9600	Yes
DCE address	Read-only
Anti streaming	No
TC enabled	No
Buffer enable	Yes
Serial number	No
Machine EC level	No
Microcode level	Yes

Point-to-Point/Multipoint

LIC6 can be 'primary', 'control', 'secondary', or 'tributary'.

DSU-CSU/LD

Defines attachment to DDS network, or limited-distance connection.

Timing Source

The receive clock provided to the host by the LIC6 is always recovered from the received signal.

The transmit clock can be provided to the host by the LIC6 in two different modes:

- Internal clock generation within the LIC6: this mode gives better performances in LDM connections
- Network clock used to generate transmit clock (synchronous mode).

Network Services

- If selected (default option), the LIC6 intercepts and executes LPDA-2 commands
- If disabled, the LIC6 ignores LPDA-2 commands
- Since LPDA-2 commands flow into the LIC6 like other pieces of data, the disable option may be selected if there is a chance that the LPDA-2 header may be erroneously detected in the data bit stream. The LPDA-2 header is guaranteed unique for the following data transmission protocols:
  - SDLC NRZI
  - BSC USACII or EBCDIC.
  - ALC.

DCE Address

- Control and primary LIC6s: always 01
- Tributary and secondary LIC6s: any value.

[1] If the option 'network services' is selected on the local LIC6; the option 'network services' or 'LPDA-2 enable' must be selected on the remote DSU/CSU.

Speed Control

See “Speed Setting” on page 4-87.

Host Support

Host support for LIC6s is NetView, using LPDA-2 functions. See *LPDA Description* manual, SY33-2064 for LPDA-2 protocols, commands, and formats.

Two sets of commands are available for:

- Problem determination
- Testing from the TSS.

Problem Determination Commands

Supported commands are:

- DSU/CSU status
- Line status
- Transmit/receive test.

TSS Commands

Two commands can be initiated by the 3745 TSS (FESA) to test the LIC6s:

- CCITT loop-3 (with or without line wrap block)
- Self-test.

CCITT Loop-3

This test is initiated by the 3745 TSS (FESA) on the DTE interface. It is the same as for LIC5. See page 4-77.

Self-Test

This test is the same as for LIC5. See page 4-77.

DDS Loop

This test is initiated by the DDS link via a bipolar code violation or a DC line current polarity reversal, as defined in the preliminary *ATT PUB 62310* dated september 1983. It consists in a wrap at the DTE interface:

1. Detect bipolar code violation or current polarity reversal
2. Raise TI
3. Set the 'modem busy' bit ON in DTE registers
4. Drop CD and RFS, DSR kept ON
5. Force data to MARK at the host side, while looping data back from DDS
6. Detect end of bipolar code violation and current polarity reversal
7. Drop TI and reset the 'modem busy' bit.

The test lasts as long as a code violation or polarity reversal is detected. It runs only if the LIC6 is in operate mode.

Alarm Tone Detection

A failure signal is sent when a hard internal failure is detected, provided that network services are enabled. This signal contains a long sequence of bipolar zeroes. However, LIC6s detect both:

- Remote power OFF tones
- Remote failure tones.

Tone Characteristics

Speed Data speed

Duration

- Power OFF: 126 zeroes
- Failure: 252 zeroes

End-to-end passthrough delay

Varies from 32 to 64 bit-time depending on the configuration.

Tone Reception

The LIC6 receiving the alarm signal detects the alarm pattern and interprets the information as a remote failure or power OFF. This information is kept in storage and is reported to the NCP on request.

DSU/CSU Configuration

DSU/CSU (LIC6 or 5822-10) configuration is only achieved locally by keying a set of commands from the IBM 5869 PKD connected to the relevant LIC6.

Portable Keyboard Display (PKD)

See “Portable Keypad Display (PKD)” on page 4-79.

Lamp Test

See page 4-80.

Background Information

This is the default information that appears on the screen in normal mode.

From left to right:

- 3745 line physical (at logical in case of LIC swap) ADDRESS: 2 characters
- Line quality irrelevant = X: X from 0 to F (0 is the best)
- Operate OFF = X: L=leased, W = local wrap via TC, D = DDS loop test
- RTS OFF = 0 ON = 1
- RFS OFF = 0 ON = 1
- CD OFF = 0 ON = 1
- RD blinks on TD activity, indicates also speed of transmission: F = full, B = backup
- TD blinks on RD activity, indicates also speed of reception: F = high, B = low.

Notes:

1. 'WRAP' is displayed instead of DSU/CSU address and line quality if a local manual loop back test is running.
2. Transitions between 0 and 1 on the screen indicate that activity is taking place on the lead.

   If there is no activity the actual status is displayed.

DSU/CSU Information

When the background information is displayed, the operator can request the local DSU/CSU main information, as follows:

Press key ERASE: 'ttt ccc nn mmm' appears on display

ttt Type of functioning

- 56 000 bps
- 19 200 or 9600 bps

ccc Transmit clock option

- INT for internal (from local)
- NC for network clocking (from remote)

nn Network configuration

- PP for point-to-point primary
- PS for point-to-point secondary
- MC for multipoint control
- MT for multipoint tributary

mmm Connection mode

- DDS for connections to DDS network
- LDM for limited distance connections

As long as the operator keeps pressing the ERASE key, the DSU/CSU information is displayed. Release the ERASE key to return to background display. This operation is not data disruptive.

POR - Bring Up Information

Same as for LIC5; see page 4-81.

Keying Procedures

See page 4-81.

Command Rejection

Same as for LIC5; see page 4-81.

Note:

- 'DTE ONLY' command rejection not available.
- 'DDS LOOP ACTIVE' brings a command rejection.

Digital Test

See page 4-213.

Local Loop Back

This command prepares the DCE for a Loop-3 test. See page 4-210.

Speed Change

Only for 19 200/9600 bps. See 'Speed Setting', page 4-87.

Configuration

The PKD being connected to a given LIC6, the **local** DSU/CSU configuration settings may be:

- Scrolled and displayed
- Updated.

Some fields are read-only (for example, machine level).

If vital fields have been modified, returning to background causes a self-test to take place.

Below are the various configuration fields for LOCAL LIC6s:

- DSU/CSU address
- Network configuration (primary/control secondary/tributary)
- DSU/CSU type (V.35/V.24)
- Transmission speed
- Transmit clock (internal/network)
- Mode (DDS/Limited distance)
- Network services (enabled/disabled)
- Machine level (EC level).

Buzzer Control

Same as for LIC5; see page 4-84.

Contentions

Same as for LIC5; see page 4-84.

Note: If a function is selected while a loop (loop-3 or DDS loop) is being executed, a message (BUSY TC ON or DDS LOOP ACTIVE) appears on the screen.

If TC raises after selection but before execution BUSY TC ON is displayed.

Unsolicited Messages

These messages appear on the screen, without any operator intervention. If a PKD operator session is in progress the unsolicited messages are delayed.They can appear only when the screen displays background information. For complete information, refer to the *Configuration and Integration Guide.*

LDM LINE DOWN or DDS LINE DOWN
Lack of receiver timing or error on received block

DDS OOS or DDS OOF
DDS out frame or DDS out of service indication

CMD FROM LINE (2 s)

CMD FROM DTE (2 s)

REM DSU/CSU FAILED
Stays on screen until the operator presses EXIT. This message is not displayed if the PKD was not present when the condition occurred.

REM PWR LOSS In point-to-point, this message remains until CD goes on or the operator presses EXIT. It appears as soon as the PKD is present if CD is still 0.

KEY n STUCK	When the indicated key appears to be pressed during more than 5 s. The message stays 10 s then the operator panel is reinitialized. This indicates a mechanical or electrical problem.
aa LIC6 FAILED	At power ON, the initial self-test failed.
DEFAULT CONFIG	Operator intervention is required to reconfigure the DSU/CSU.
INV PATTERN RCV	Invalid pattern received (ex: a DDS pattern into LDM mode)
TEST FROM HOST	A test from the 3745 has been initiated.
WRONG SLOT	The cassette has been plugged in a wrong position.
MAND DDS LOOP	A mandatory DDS loop from DDS has been initiated (reversal polarity loop)
OPT DDS LOOP	A optional DDS loop from DDS has been initiated (bipolar code violation loop)
TEST FAILED	A manual self-test failed or a host self-test failed.
SELF TEST FAILED	A self-test failed after a configuration change.
TEST OK	A self-test requested by the host is successful.
SELF TEST OK	A self-test is successful after a configuration change.
TEST OK NOWRP	A manual self-test without tel wrap plug is successful.
TEST OK WRAP	A manual self-test with tel wrap plug is successful.
DEFAULT CONFIG	Operation intervention is required to reconfigure the CSU/CSU.

Manual Tests

The following manual tests are all initiated from the PKD:

	Data Disruptive
Local loop back	Yes[1]
Local self test	Yes[1]
Digital test (transmit/receive test)	Yes[1]

[1] Run continuously until 'EXIT' is pressed.

Descriptions of the above manual tests are given later in this chapter, under 'Problem Determination Aids' for LIC5s and LIC6s.

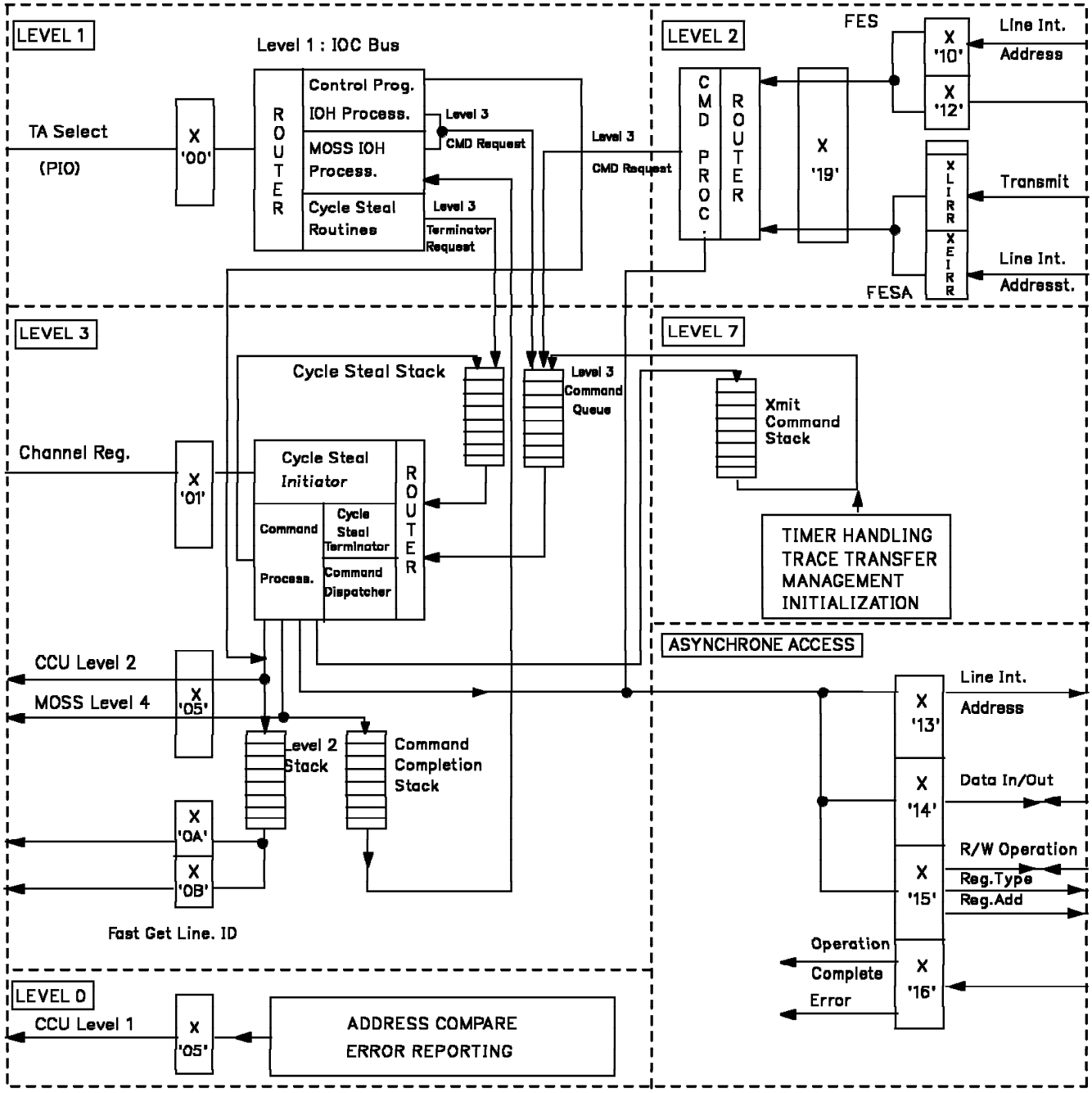
PT2/3

A 10-pin connector is available on the LIC6 panel to connect a PT2/3 used to investigate and record control and data signals.

Scanner Microcode

The scanner microcode:

- Manages the data buffers in the control storage for the transmitted and received data
- Supports the link protocols
- Controls the line interfaces
- Provides service facilities under the control of the NCP/EP or the MOSS.



Line Operating Modes

The microcode operates the lines in one of the following modes:

- Normal mode
- Character mode
- Burst mode
- Service mode.

The operating mode is selected on a line-by-line basis and the scanner may run all four modes at the same time.

Normal Mode

The microcode normally uses this mode to transfer data in a burst of 16, 32 or 64 characters (cycle steal).

The scanner interrupts the CP on a message basis. The supported link protocols are:

SDLC

- Half-duplex or duplex
- CRC management
- Zero-bit insertion and deletion
- Flag abort and idle detection
- NRZ/NRZI encoding and decoding
- Echo suppression
- Address compare.

BSC

- Half-duplex
- EBCDIC (EP mode)
- ASCII (EP mode)
- EBCDIC transparency (EP mode)
- ASCII-7 transparency (EP mode)
- Control character recognition
- CRC management
- VRC/LRC management (ASCII)
- Synchronization character insertion and deletion
- Time out on continuous synchronization.

X.21

- Leased lines
- Switched lines (CCITT 80/84).

Autocall

- NCP/EP
- Automatic call origination.

Character Mode

The data transfer is achieved character by character. The supported link protocols are:

BSC

- No control character recognition
- No CRC management
- No synchronization character insertion

- No time out on continuous synchronization

Start-stop

- Start bit insertion and deletion
- Five through eight information bits
- Insertion of one or two stop bits

Burst Mode

This mode supports the start-stop protocol only. It is similar to character mode, except that the characters are exchanged by bursts of 16, 32 or 64 characters between the scanner and the CCU.

The detection of the ending character is performed by the scanner microcode.

Service Mode

In service mode, the scanner executes the commands sent from the MOSS. The scanner may be connected or disconnected.

Microcode Levels

The microcode operates on five levels numbered 0, 1, 2, 3, and 7 (levels 4, 5, and 6 are not used).

Microcode Interaction with the Control Program

The scanner microcode operates with the CCU control program (in normal mode, character mode, or burst mode) using:

- Reserved areas in CCU main storage.
- Reserved areas in scanner storage.
- Instructions (IOH or IOHI) to move control information between the CCU and the scanner.
- Commands (specified in register R1 of the associated IOH/IOHI instruction) to start a line, or start a line with initialization.

PIO is used to transfer commands to the line interfaces (4 bytes) and to get the line identification and error status (2 bytes).

AIO is used to transfer data, parameters, and status between the scanner and CCU storages in cycle steal mode.

The scanner interrupts the control program on level 2 for normal operation, and on level 1 for error reporting.

Reserved CCU Storage Areas

In the CCU main storage, three types of area are reserved for communication with the scanners:

- Parameter/status areas
- Line vector table
- Data buffers.

Parameter/Status Area (PSA)

For each line interface (transmit or receive), the control program reserves one parameter/status area. A duplex line has two PSAs, a half-duplex line one PSA. The scanner accesses the PSAs by cycle steal.

The PSA is divided into two areas:

1. The parameter area (16 bytes, 4 words), used to transfer control parameters from the CCU to the scanner.
2. The status area (12 bytes, 3 words), used to transfer the command status from the scanner to the CCU.

The 28 bytes (7 words) making up the PSA must be contiguous, but may be located anywhere in main storage.

Line Vector Table (LNVT)

The line vector table consists of 2048 locations, two for each of the 1024 lines in the controller. There are two entries per line: one for the transmit interface (even address), another one for the receive interface (odd address). For a half-duplex line, the first LNVT entry points to the unique PSA used for both the transmit and receive interfaces. The second entry is not used (except during wrap processing).

One LNVT address is defined, per scanner using the set LNVT high/low commands (no default address).

For the trace LNVT (TLNVT), address X'1000' is defined as the default address.

The TLNVT is updated by the set TLNVT high/low commands.

Data Buffers

Those are areas reserved for the temporary storage of data and other information in transit through the controller. They are accessed by the scanner in cycle steal mode. The address of the buffers to be used by the scanner is part of the parameter area of the PSA. The format of the buffers depends on the control program (NCP or EP).

Buffer format (no prefix-offset for the EP):

Byte	Contents
	Prefix
0-3	Address of the next buffer in the chain
4-5	(Not used)
6	Offset value in bytes
7	Buffer byte count
	Offset
Up to 256	Data (varies with control program)

For the first buffer in a chain, the offset and byte count are provided by the PSA.

For the other buffers:

- In transmit operations, the link pointer, offset, and byte count are taken from the buffer prefix.
- In receive operations, the link pointer is taken for the buffer prefix, the offset is zero, and the byte count is provided to the scanner by the set mode information.

Parameter/Status Area

The PSAs of CCU storage are duplicated in the scanner control storage.

The parameters related to the line interface (parameter area) are transferred from the CCU to the scanner with the command; the status of the line after execution of the command (status area) is transferred from the scanner to the CCU.
All transfers are made by cycle steal.

For description of the status of the line, refer to “Miscellaneous Status Fields” on page 4-191

Scanner Address Description

There are two ways to address the scanner:

- One for the get line identification PIO (it is a broadcast PIO).
- One for the other PIOs.

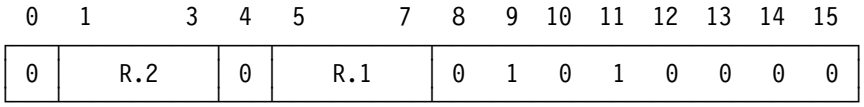
PIOs which are not 'get line ID' are recognized by comparing UC bus byte 0 bits 5, 6, and 7 with the physical address wired on the board and which represents the group address. Moreover one out of two scanners is selected by byte 0 bit 2 or 3 which are also wired on the board according to the scanner position.

Note: MMIO coming from the MOSS uses the same addressing circuit. The difference with the PIO is byte 1 bit 4.

CCU Instructions

The CCU IOH/IOHI instructions are used to move control information between the CCU and the scanner.

IOH Format

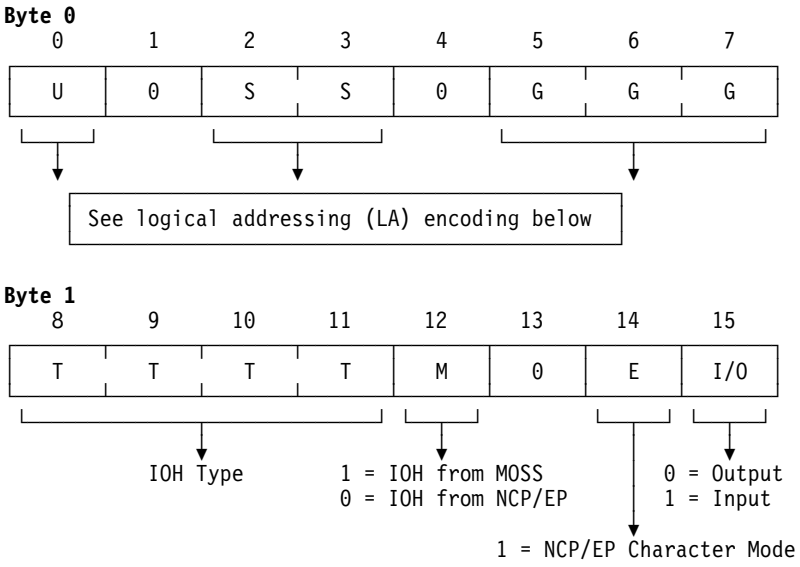


This input/output instruction (IOH) transfers the contents of the register specified by R1 to the communication scanner, or places information coming from the communication scanner into the register specified by R1.

The scanner address, the scanner command, and the direction of data movement specified by the contents of R2 are sent at TA on the IOC buses.

For a correct execution of the instruction, R2 must be loaded as follows:

R2 Contents at TA Time



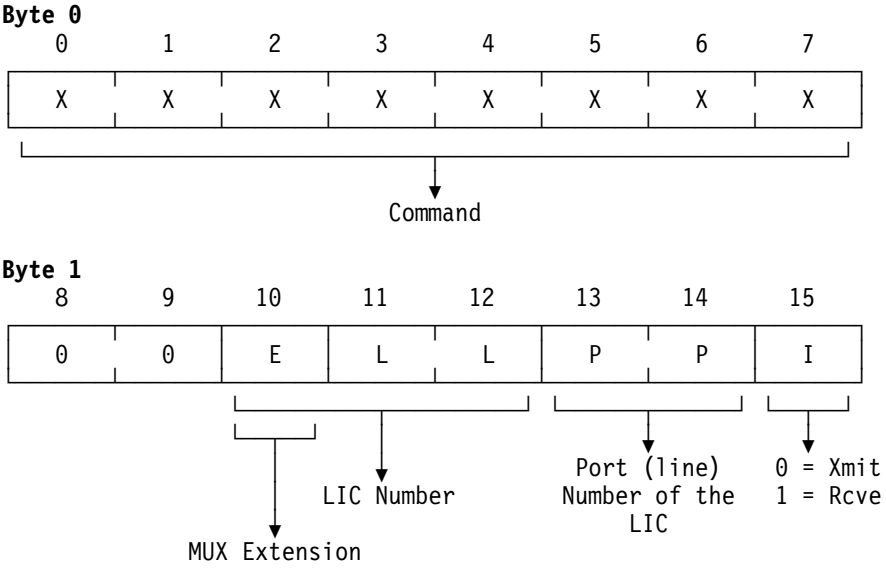
TA Byte 0 Contents of IOH/IOHI at TA Time

Logical Addresses	TA Byte 0							
	0	1	2	3	4	5	6	7
	U	0	S	S	0	G	G	G
LA 1	0	0	0	1	0	0	0	0
LA 2	0	0	1	0	0	0	0	0
LA 3	0	0	0	1	0	0	0	1
LA 4	0	0	1	0	0	0	0	1
LA 5	1	0	0	1	0	0	0	0
LA 6	1	0	1	0	0	0	0	0
LA 7	1	0	0	1	0	0	0	1
LA 8	1	0	1	0	0	0	0	1
LA 9	0	0	0	1	0	0	1	0
LA 10	0	0	1	0	0	0	1	0
LA 11	0	0	0	1	0	0	1	1
LA 12	0	0	1	0	0	0	1	1
LA 13	1	0	0	1	0	0	1	0
LA 14	1	0	1	0	0	0	1	0
LA 15	1	0	0	1	0	0	1	1
LA 16	1	0	1	0	0	0	1	1

Logical Addresses	TA Byte 0							
	0	1	2	3	4	5	6	7
	U	0	S	S	0	G	G	G
LA 17	0	0	0	1	0	1	0	0
LA 18	0	0	1	0	0	1	0	0
LA 19	0	0	0	1	0	1	0	1
LA 20	0	0	1	0	0	1	0	1
LA 21	1	0	0	1	0	1	0	0
LA 22	1	0	1	0	0	1	0	0
LA 23	1	0	0	1	0	1	0	1
LA 24	1	0	1	0	0	1	0	1
LA 25	0	0	0	1	0	1	1	0
LA 26	0	0	1	0	0	1	1	0
LA 27	0	0	0	1	0	1	1	1
LA 28	0	0	1	0	0	1	1	1
LA 29	1	0	0	1	0	1	1	0
LA 30	1	0	1	0	0	1	1	0
LA 31	1	0	0	1	0	1	1	1
LA 32	1	0	1	0	0	1	1	1

R1 Contents at TD Time

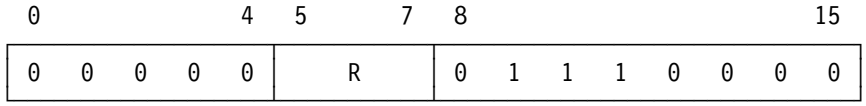
The R1 contents hereafter is sent only at TD time for start line and start line initial commands.



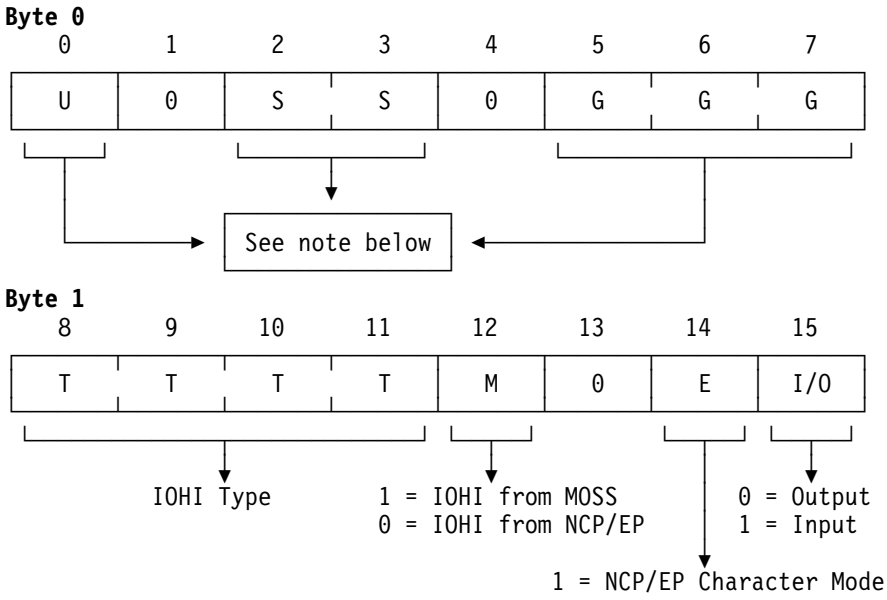
IOHI Format

At TD time, this instruction transfers the contents of register R to the scanner, or places information coming from the scanner into the register. The direction of data movement is specified by the contents of the second halfword sent at TA time.

First Halfword



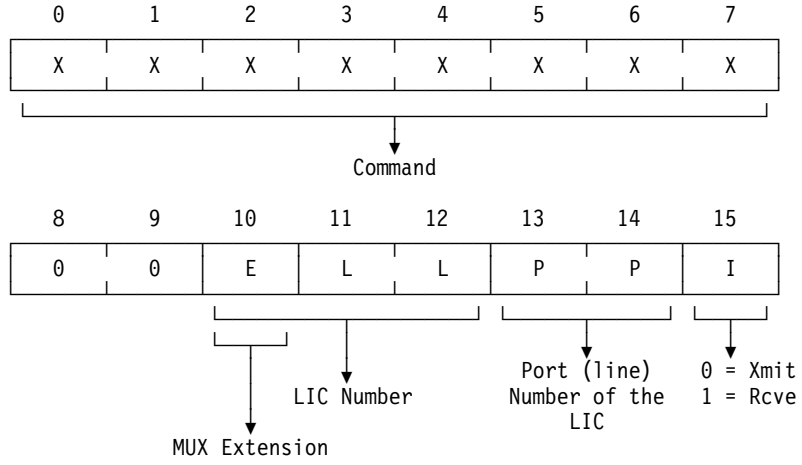
Second Halfword The second halfword is sent at TA time on the IOC buses.



Note: See “TA Byte 0 Contents of IOH/IOHI at TA Time” on page 4-104.

R Contents at TD Time

The contents of R are sent at TD time, only for start line and start line initial commands.



IOH/IOHI Instruction (from NCP/EP) Summary

IOH/IOHI Byte 1[2]	Instruction	Description
00	Start line	CCU output instruction
10	Start line initial	Output initialization interface
11	Get error status	CCU level 1 input instruction
01	Fast get line ID	CCU level 2 input instruction
20/30	Set LNVT high/low	LNVT relocation
21	Get cmd reject status	CCU level 1 input instruction
31	Get microcode checkers	CCU level 1 input instruction
50/60	Set trace LNVT high/low	Output instruction
F2	Automatic dump	

Start Line

This instruction is used to start a line operation when the PSA address is already known to the scanner. The scanner uses the line interface address to locate the PSA address following the ICB, cycle steals the PSA contents from the CCU storage, and executes the command.

Start Line Initial

This instruction is used the first time a line is addressed from the control program.

Get Error Status

This instruction is issued to the scanner that requested a CCU interrupt level 1. R1/R contains the error status.

Fast Get Line Identification

Before raising a level 2 interrupt to the IOC, the microcode loads the two external registers X'0A' and X'0B' with the line ID, and sets X'05' bit 7 ON. The get line ID is sent to the scanner at TD time and the IOC bus gets the contents of the X'0A' and X'0B' registers (R1/R contents).

Set LNVT High/Low

This instruction is used to provide a scanner with the LNVT address for its lines.

'Set line vector table low' modifies bytes 0 and 1 of the LNVT address.

[2] IOH: byte 1
IOHI: byte 1 of second halfword

IOH/IOHI Instruction (from MOSS) Summary

IOH/IOHI Byte 1[3]	Instruction
08	Start MOSS
09	Get command completion
18	Run JIB checkout
19	Get error status
28	Set MOSS area high
29	Get JIB checkout results
38	Set MOSS area low
39	Get scanner status
48	Reset

Commands

Commands are used by the start line and start line initial instructions. The command code is given by bits 0 through 7 of register R1/R of the IOH/IOHI instruction. Once a scanner has received a command from the control program, the command remains outstanding until the scanner ends the command execution and requests a CCU interrupt level 2. The halt and halt immediate commands may be issued at any time, even if another command is outstanding.

The commands are organized in the following subsets:

Common Commands

Common commands can be issued by the NCP or the EP in normal or character mode. Instructions issued in character mode have the character mode bit (bit 14 of the second halfword) set to 1 in the instruction.

Commands	Codes (hex)
Set mode	01
Enable	02
Disable	03
Monitor incoming call	04
Dial (normal mode only)	05
Change	06
Raise DTR	08
Flush data	09
Reset-D	0B
Reset-N	0C
Halt	F0
Halt immediate	F1

NCP Commands

NCP commands can be issued by the NCP on SDLC, BSC, or X.21 lines working in normal mode.

[3] IOH: byte 1
IOHI: byte 1 of second halfword

Commands	Codes (hex)
V.25 bis call request V.25 bis monitor incoming call V.25 bis clear request	0D 0E 0F
SDLC transmit control SDLC transmit data SDLC transmit continue SDLC receive monitor SDLC receive SDLC receive continue	10 11 1D 12 13 14
X.21 call request X.21 monitor incoming call X.21 clear request	15 16 17
NCP BSC control NCP BSC transmit NCP BSC transmit continue NCP BSC receive NCP BSC receive continue	18 19 1A 1B 1C

EP Commands

EP commands can be issued by the EP on BSC lines operating in normal mode.

Commands	Codes (hex)
EP BSC transmit initial EP BSC transmit SYN EP BSC transmit data EP BSC poll EP BSC receive EP BSC receive continue EP BSC prepare EP BSC monitor for phase EP BSC ADPREP EP BSC search	20 21 22 23 24 25 26 27 28 29

Character Mode Commands

Character mode commands can be issued by the NCP or EP on BSC or start-stop lines (both working in character mode).

Command	Code (hex)
Write ICW	40

Burst Mode Commands

Burst mode commands can be issued by the NCP or EP on start-stop lines.

Command	Code (hex)
Start-stop transfer	41

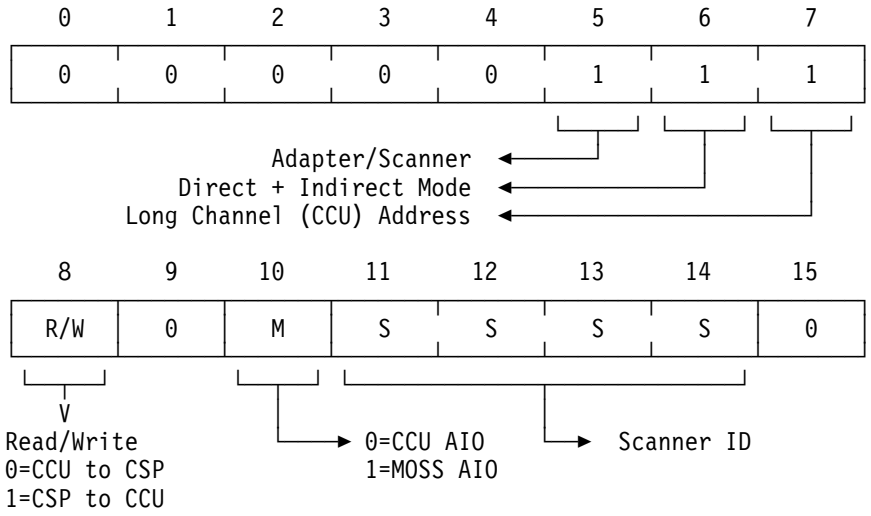
Miscellaneous Commands

These commands are used for DCE testing and for line tracing in all protocols. Commands F4 and F5 are issued by the NCP when a scanner time out occurs.

With a modem testing command (2B), the microcode can request the status of local or remote 386x and 58xx modems, or their attached lines (for more description, refer to the 386x and 586x documentation).

Commands	Codes (hex)
386X and 58xx modem test	2B
Trace	2C
Stop trace	2D
Wrap	2E
F4 dump ICB	F4
F5 dump ICB and halt I	F5

Cycle Steal Control Word (CSCW) Format



IOC 1	X 0 M S	S S S 0	IOC 2
LA 1	x 0 x 0	0 0 0 0	LA 5
LA 2	x 0 x 0	0 0 1 0	LA 6
LA 3	x 0 x 0	0 1 0 0	LA 7
LA 4	x 0 x 0	0 1 1 0	LA 8
LA 9	x 0 x 0	1 0 0 0	LA 13
LA 10	x 0 x 0	1 0 1 0	LA 14
LA 11	x 0 x 0	1 1 0 0	LA 15
LA 12	x 0 x 0	1 1 1 0	LA 16
LA 27	x 0 x 1	0 0 0 0	LA 21
LA 18	x 0 x 1	0 0 1 0	LA 22
LA 19	x 0 x 1	0 1 0 0	LA 23
LA 20	x 0 x 1	0 1 1 0	LA 24
LA 25	x 0 x 1	1 0 0 0	LA 29
LA 26	x 0 x 1	1 0 1 0	LA 30
LA 27	x 0 x 1	1 1 0 0	LA 31
LA 28	x 0 x 1	1 1 1 0	LA 32

Microcode Interaction with FES

The scanner microcode operates with the FES hardware using:

- Reserved areas in the control storage
- FES storages (RAM A, RAM B, RAM C, and inbound/outbound RAM)
- Commands.

The asynchronous path through the CSP external registers is used for transferring commands, initializing the lines, and managing the modems and timers.

Cycle stealing is used for the transmission of data, parameters, and status information between the control storage and the FES storages (in two-byte burst).

The FES interrupts the microcode at level 2 in normal operation (for example, end of message), and for error reporting.

Reserved Scanner Storage Areas

- FES Parameter/Status
- Line Interface Buffers.

FES Storages

RAM A

RAM A is devoted to the character service function of the scanner base. Four halfwords are assigned to each line interface (receive and transmit).

Receive

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	New PDF	SCF
1	Old PDF	Interrupt request
2	Control storage addressing	
3	Scanner base ctrl. parameters	Timer

Transmit

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Timer Control	SCF
1	Next PDF	Interrupt request
2	Control storage addressing	
3	Scanner base control (parameters)	

Parallel data field (PDF)

On the receive line interface, the old PDF and the new PDF contain the next two characters to be loaded into the control storage. On the transmit line interface, the next PDF contains the last character received from the control storage.

Secondary control field (SCF)

The SCF in RAM A is a duplication of the SCF in RAM B. It is used by the character service function to know the status of the bit service function after character deserialization and serialization.

The SCF gives the second byte of the status transferred to the CSP at burst end (the first byte is given by the scanner base control).

Interrupt request

This field reports the interrupt or error conditions that occurred during data reception or transmission. The field contents are transferred to register X'10' to indicate the cause of the interrupt.

Control storage addressing

This field contains the address of the line interface buffers in the control storage. It is used during cycle steal transfers between the FES and the CSP.

Scanner base control

This field contains the parameters provided by the microcode to the scanner base layer for processing the burst according to the link protocol. Some parameters of the scanner base control are duplicated in the PCF (RAM B).

At burst end, the scanner base control gives the first byte of the status to be transferred to the CSP (the second byte is given by the SCF).

Timer The timer fields are used by the BSC protocol:

- On the receive interfaces, to check that two SYN characters are separated by less than three seconds
- On the transmit interfaces, to insert a SYN character every second in the transmitted data.

The timer fields can also be used by the microcode to generate time outs.

RAM B

RAM B is devoted to the bit service function of the front-end layer. Four halfwords are assigned to each line interface (receive and transmit).

Receive

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	SDF	SCF
1	PDF	PCF
2	Spare	Spare
3	SYN 1	SYN 2

Transmit

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	SDF	SCF
1	PDF	PCF
2	DLE	Spare
3	SYN	Spare

Serial data field (SDF)

On the receive line interface, the SDF is used to deserialize the bits received from the line, to form a character. On the transmit line interface, the SDF is used to serialize the character into bits for transmission over the line. The work of the SDF is controlled by the SCF.

Parallel data field (PDF)

On the receive line interface, the PDF contains the last character deserialized from the SDF. On the transmit interface, the next character to be serialized is in the SDF.

Secondary control field (SCF)

This field is used as a working zone to control the character serialization and deserialization in the SDF. At burst end, it gives the status of the bit service function.

Primary control field (PCF)

The PCF is used as a communication zone between RAM A and RAM B, and duplicates some parameters of the scanner base control field. On the receive line interface, the PCF contains the parameters to be used for deserialization. On the transmit line interface, the PCF contains the parameters to be used for serialization.

Synchronization

These fields contain the SYN character(s) to be used during data transmission in BSC.

On the receive line interface, the SYN character is used as a reference for detection of the SYN character received from the line. Two SYN characters are needed in BSC protocol, one in BSC-like protocols (usually non-standard, and non-IBM BSC protocols).

On the transmit line interface, the SYN character is stacked for transmission over the line once per second.

Data link escape (DLE)

This field contains the DLE character used in BSC transmission. Sequences containing the DLE character initiate and terminate the transparent text, and provide an active control character within the transparent text.

RAM C

RAM C is devoted to the line service function of the front-end layer. Four halfwords are assigned to each line interface (receive and transmit).

Receive

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Set mode	Control
1	BCC2 (see note)	BCC1 (see note)
2	Modem-in pattern	Mask
3	Spare	Spare

Note: Not used in start-stop protocol.

Transmit

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Set mode	Control
1	BCC2 (see note)	BCC1 (see note)
2	Modem–out immediate	Mask
3	Modem–out stacked	Mask

Note: Not used in start-stop protocol.

Set mode

This field contains the link protocol parameters specific to the line interface.

Control This field contains the parameters provided by the microcode to the line service function for processing the burst according to the link protocol.

In BSC ASCII or EBCDIC, bit 7 of the set mode field is used as an additional bit of the control field.

Modem-in

This field contains the status of the line interface wires activated from the modem. It is compared with the modem-in information coming from the LIC to detect any modem change.
The modem-in status depends on the interface type: V.24, V.25, X.21, or V.35. The modem change indication (bits 6 and 7) causes an interrupt request to the CSP via register X'10'.

Modem-out

The modem-out immediate field contains the interface configuration that is supplied to the modem via the LIC registers. The modem-out information depends on the interface type: V.24, V.25, X.21, or V.35. Modem-out stacked contains the next modem-out pattern that will be transmitted when bit 15 of the PCF is set on.

The modem-out field of the RAM is compared with the modem-out echo coming from the LIC to detect any failures in the modem drivers of the LIC (LIC driver check).

Mask This field is used by the microcode to select the bits of the modem-in or modem-out field that must be checked for modem change or LIC driver check.

Block check character (BCC)

These fields (BCC2 and BCC1) are used for cyclic redundancy checking in SDLC and BSC protocols. They accumulate the block check characters during transmission or reception. The block check character is reset at the beginning of the block; block check accumulation is then performed until the end of the block or message.

On a receive line interface:

- In BSC protocol, the accumulated BCCs are compared with the received BCCs for error detection.
- In SDLC, the result of the accumulation performed during message reception (including the BCCs) must be X'F0B8'.

On a transmit line interface, the accumulated BCCs are transmitted at the end of the block or message.

Commands

The scanner microcode uses commands to operate the FES. All commands are transferred via external registers X'13', X'14', X'15', X'16' and X'17'.

Receive and Transmit Commands

The microcode sets the FES RAMs for receive and transmit operations through the FES asynchronous path, using external registers X'13', X'14', X'15', and X'16', then starts the FES by loading bit 1 of the scanner base control field.

Reset/Freeze Command

This command is transmitted to the FES via external register X'17'. Depending on the setting of the bits in the register, the components of the FES may be reset or frozen.

Microcode Interaction with MOSS

When the scanner is in service mode, the scanner microcode operates with the MOSS microcode, using:

- Reserved areas in CCU main storage (mailboxes and data areas) as described in Chapter 2, "Central Control Unit" (CCU) and Chapter 8, "Maintenance Operator Subsystem" (MOSS).
- Reserved areas in scanner control storage.

The scanner interrupts the MOSS at level 4 for normal operation and error reporting. Cycle stealing is used to transfer (via the mailboxes in CCU storage) the data, parameters, and status between scanner and MOSS storages.

Control information is exchanged via MOSS I/O instructions.

Control Block Relationship

The following figure shows the relationship between the control blocks in CCU main storage, CSP control storage, FESL storage, and the LIC registers.

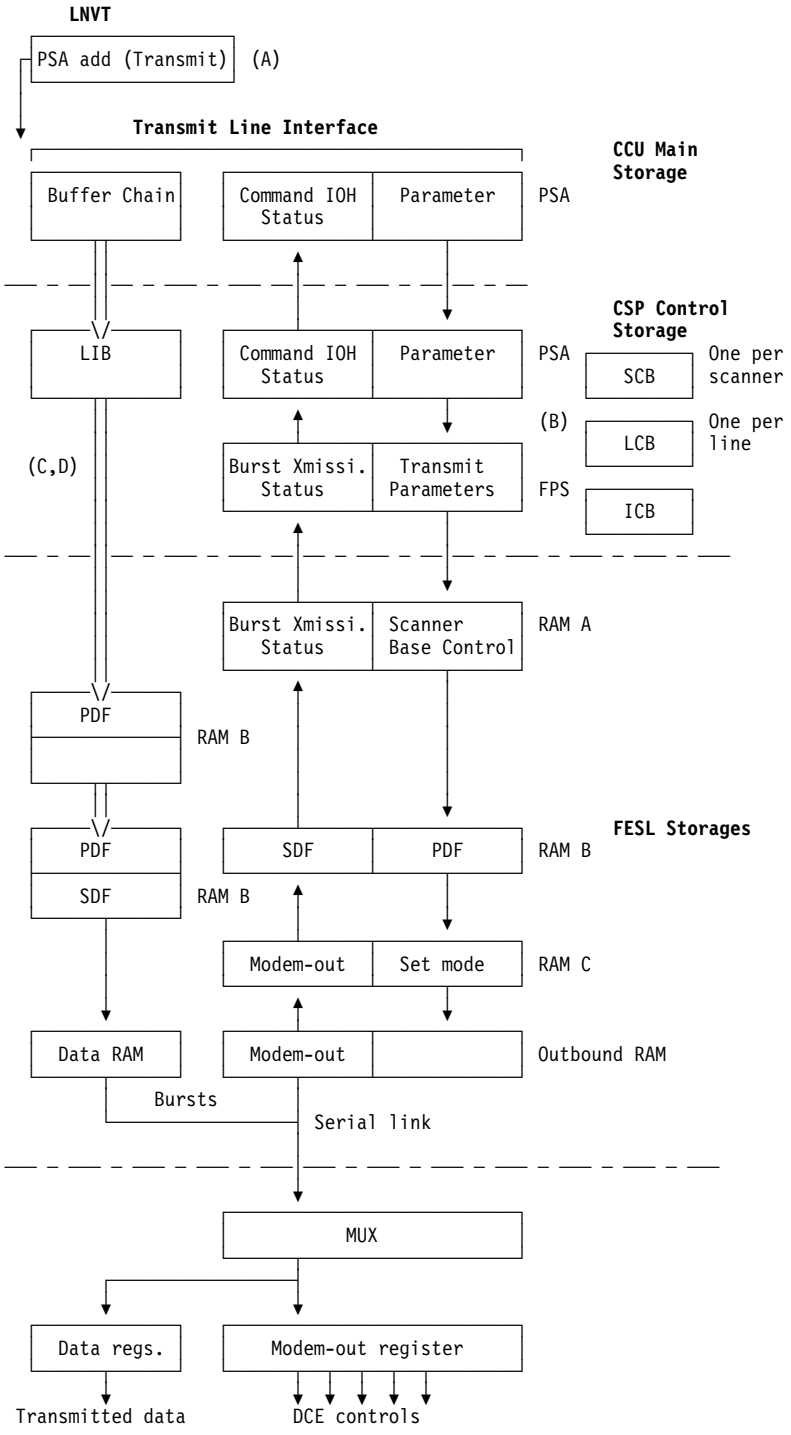
Data Transfers

For a duplex line, the control blocks are related as follows:

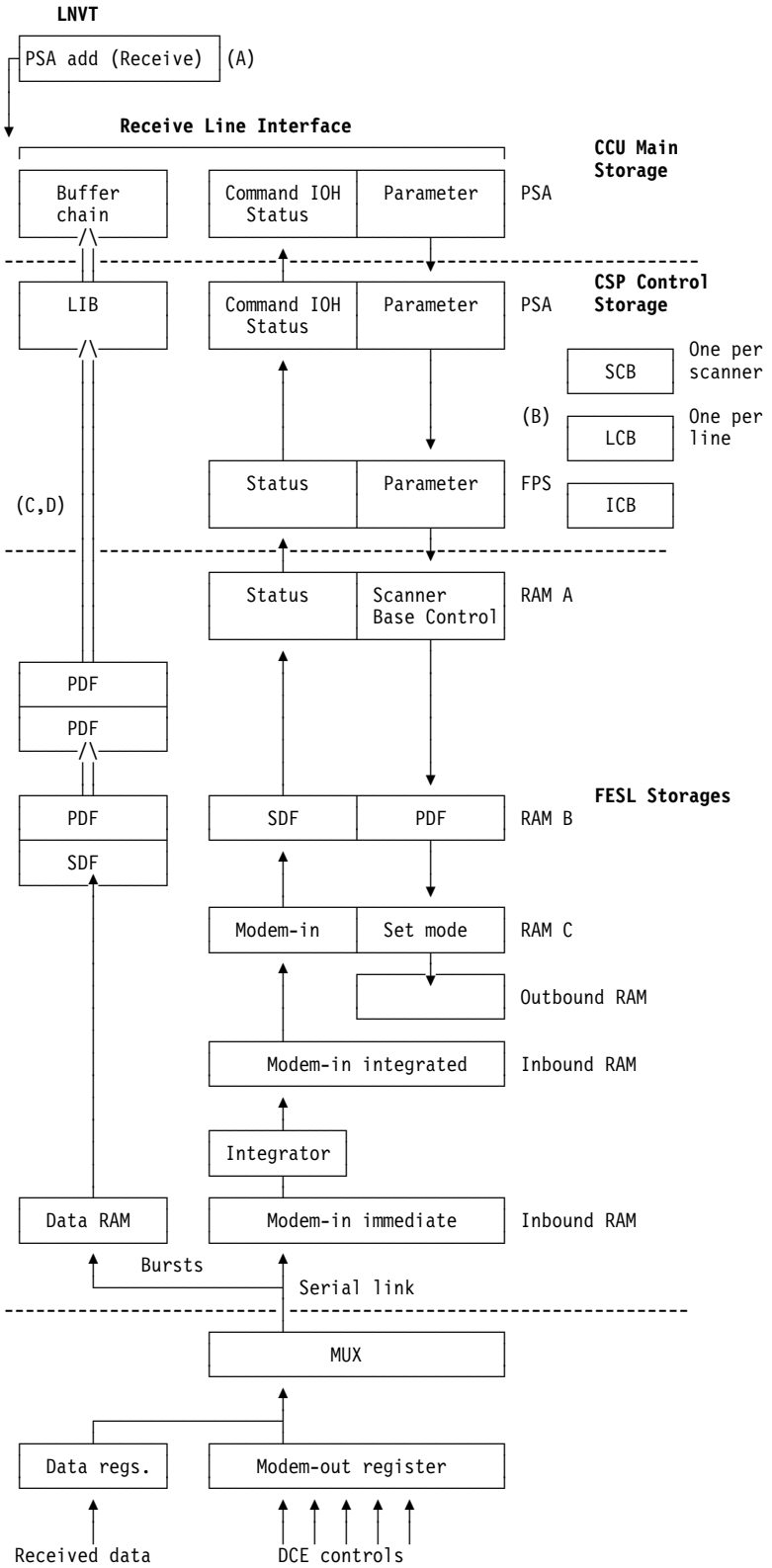
- The LNVT addresses two PSAs, one for transmit, the other for receive.
- The line parameters given in the PSA are transferred to the line control block (LCB) at scanner initialization.
- The transmitted data transits through the parallel data field (PDF) from the CCU transmit buffer to the transmit line interface.
- The received data transits through the PDF from the receive line interface to the CCU receive buffer.

For a half-duplex line, only one PSA is addressed and the transmit and receive line interfaces are related to the same PSA (the transmit one).

Transmit Data Transfer Flows



Receive Data Transfer Flows



Scanner Status After the IML

At the end of scanner IML it is possible to get from the CCU storage, the status of the scanners associated with their mailbox.

The 16-byte mailboxes are located from CCU storage address 3F8000 (for 4MB storage) or 7F8000 (for 8MB storage). The status of the scanners just IMLed are in the last two bytes of the mailbox. These values must be displayed before any mailbox exchange between the CCU storage and the corresponding scanner (for example: CCU functions). Below are the possible statuses of the scanner after an IML:

Values	Description
X'nnFF'	No answer from scanner following the MOSS command 'nn'
X'C900'	Normal status IML OK
X'C904'	Adapter interface check
X'C908'	FES error reporting path check
X'C90F'	MUX address different between CDF and return values from the scanner
X'C910'	FES internal error
X'C920'	MUX error
X'C940'	FES failing to answer
X'C980'	AIO error
X'C9F0'	Bypass bit different between CDF and return values from the scanner

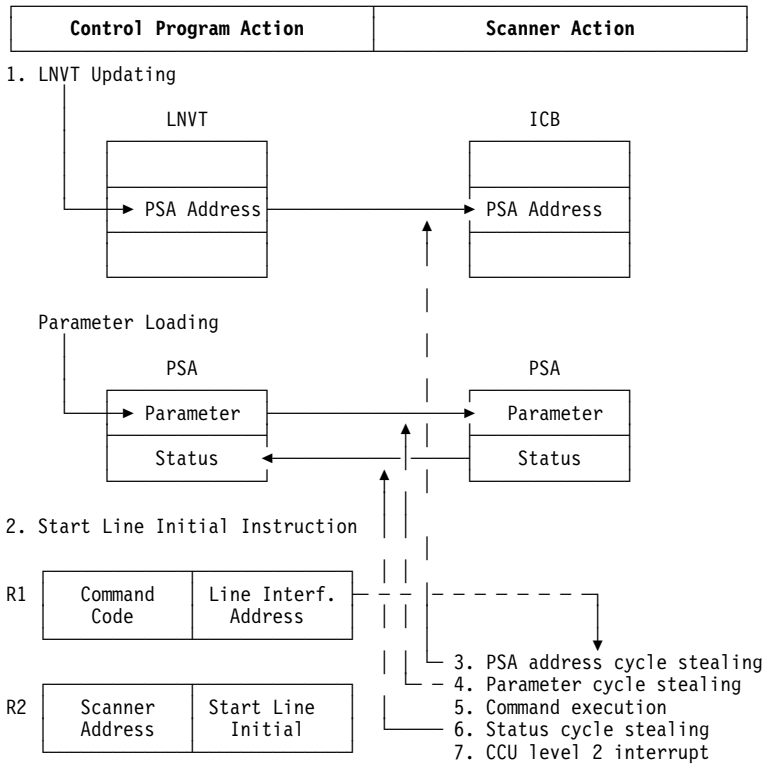
Figure 4-3. Values of the Last Two Bytes of the Mailboxes after IML (LSS)

Instruction Operation

Start Line Initial

The operating sequence for the start line initial instruction is:

1. The control program updates the PSA address in the LNVT (after IPL or when a new PSA is used), and loads the command parameters in the PSA of the line interface to be addressed.
2. The control program issues a start line initial instruction; the contents of R1 are transmitted via the IOC bus to the scanner, according to the contents of R.2.
3. From the line interface address, the scanner identifies the LNVT entry to get the PSA address for the subsequent start line instruction(s).
4. The scanner cycle steals the parameters from the PSA.
5. The scanner executes the command according to the command code and the parameters.
6. When the command has been executed, the scanner prepares the status and cycle steals it into the status area of the PSA.
7. The scanner interrupts the CCU at level 2.

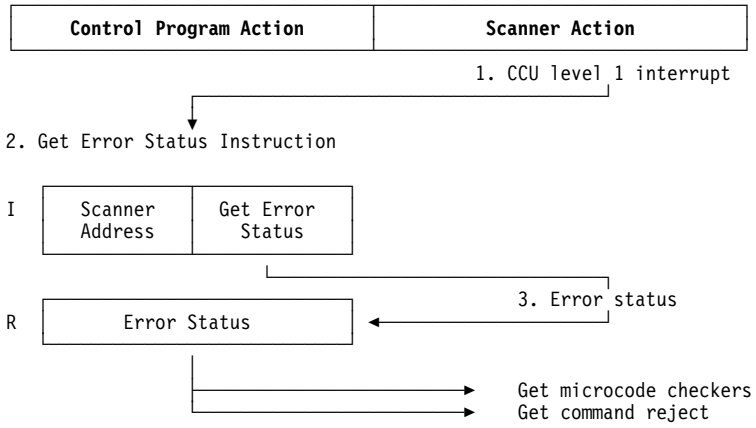


Get Error Status

The operating sequence for the get error status instruction is:

1. The scanner interrupts the control program at level 1.
2. The control program issues a get error status instruction to all scanners to determine which scanner raised the interrupt level 1.

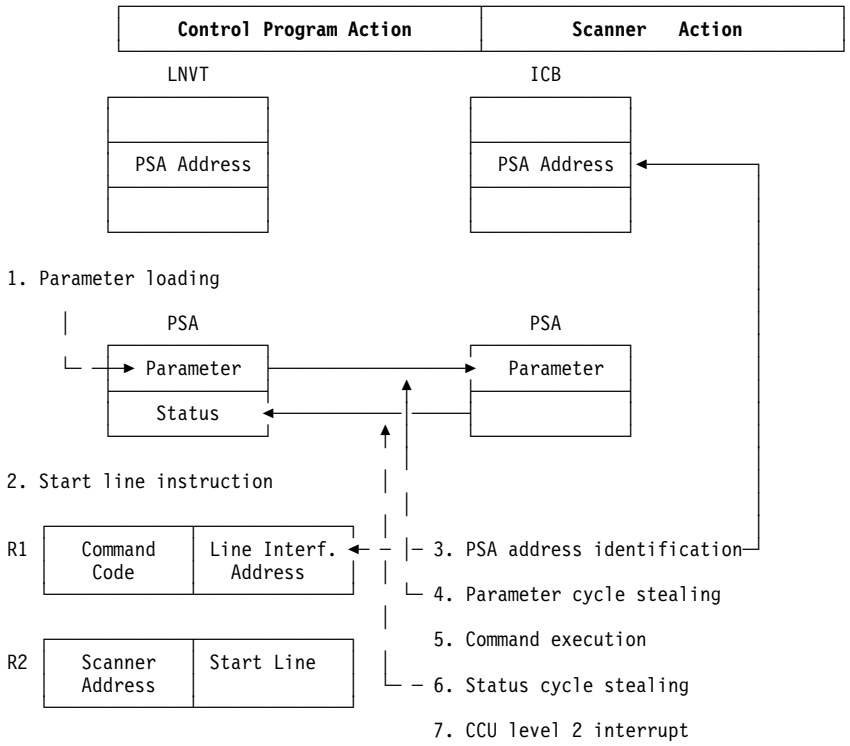
   The scanner that returns a non-zero response is the scanner determined to be the one in error.
3. The scanner loads register R with the error status.



Start Line

The operating sequence for the start line instruction is:

1. The control program loads the parameters of the command into the PSA of the line interface to be addressed.
2. The control program issues a start line instruction; the contents of R.1 are transmitted via the IOC bus to the scanner, according to the contents of R.2.
3. From the line interface address, the scanner identifies the PSA address in the ICB.
4. The scanner cycle steals the parameters from the PSA.
5. The scanner executes the command according to the command code and the parameters.
6. When the command has been executed, the scanner prepares the status and cycle steals it into the status area of the PSA.
7. The scanner interrupts the CCU at level 2.

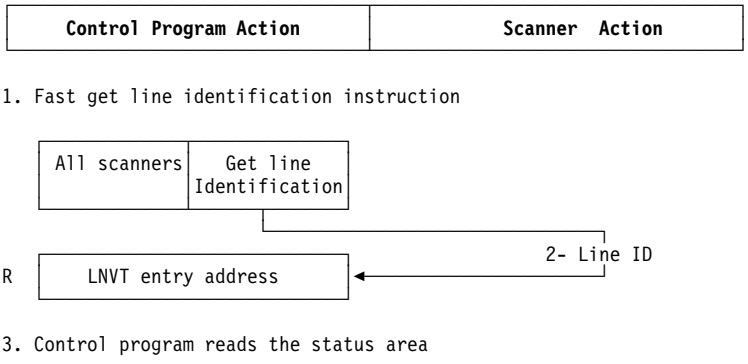


Fast Get Line Identification

The operating sequence for the fast get line identification instruction is as follow:

1. The control program issues a fast get line identification to all the scanners.

   The first scanner on the bus chain which raises interrupt level 2 will be serviced first.
2. The scanner returns the line ID to the CCU control program.
3. The control program reads the status area from the PSA.



External Registers Description

Note: References are hereunder made to ping and pong buffers. See Figure 4-2 on page 4-20 and definition on page4-21 for details.

X'00': IOC Bus Control 1

This register indicates to the scanner microcode the type of exchange that is performed with the CCU: PIO ('TA select' ON) or AIO ('cycle steal select' ON). It also controls the operation of the pong buffer.

The bits are not checked for parity. They have the following meaning:

Bit	Function
0	TA time select
1	Cycle steal select
2	(Not used)
3	Channel address valid halfword
4	ETX, ETB, ENQ (ASCII)
5	ETX, ETB, ENQ (EBCDIC)
6	Pong buffer busy
7	Pong buffer end-of-chain

Bit 0 Set at TA time of a PIO read/write operation when the scanner has decoded its address and no parity error has been detected. It is reset by the microcode.

Bit 1 Set when the scanner has detected the 'cycle steal grant' tag ON. It is reset by the microcode.

Bit 3 Automatically set ON when the microcode sets ON the extended channel address valid halfword (external register X'01' bit 4). It is reset at the same time as the pong buffer busy bit.

Bit 4 Set when an ETX, ETB, and ENQ ASCII character is decoded in the ping or pong buffer during a data transfer from the IOC bus to the scanner. It is reset at the beginning of the channel grant transfer.

Bit 5 Same as for bit 4 for EBCDIC characters.

Bit 6 Set by hardware to indicate to the microcode that the pong buffer is busy.
It is automatically reset when the valid halfword or end-of-chain tag drops.

Bit 7 Set when the last data halfword is to be received into or sent from the pong buffer.

It is automatically reset when the end-of-chain has been sent to the CCU, or by a PIO selection (TA time).

X'01': IOC Bus Control 2

This register controls the cycle steal operation on the IOC bus and the ping buffer operation. The bits are not checked for parity.

They have the following meaning:

Bit	Function
0	(Not used)
1	Channel request ready
2	Channel request
3	Ping buffer selected
4	Extended channel address valid halfword
5	Disconnect mode (CCU PIO disabled)
6	Ping buffer busy
7	Ping buffer end-of-chain

Bit 1 Set by the microcode after the cycle steal control word and cycle steal address have been loaded into the ping and pong buffers.

It is reset by the cycle steal grant tag when cycle stealing starts.

Bit 2 Set and reset at the same time as bit 1. It is used to define the priority level associated with the request (see also external register X'05' bit 5).

Bit 3 Set when the ping buffer is connected to the IOC bus.

It is reset when the pong buffer is connected.

Bit 4 Set by the microcode when more than 16 bits of address are required.

It is reset at the same time as the ping buffer busy bit.

Bit 5 Set and reset by the microcode. When ON, this bit prevents any PIO operation from the CCU and level 1 or 2 interrupt requests from the scanner (disconnect mode).

PIO operations initiated from the MOSS are, however, still accepted. When set OFF, this bit indicates connect mode.

Bit 6 Set by hardware to indicate to the microcode that the ping buffer is busy.

It is automatically reset when the valid halfword or end-of-chain tag drops.

Bit 7 Set when the last data halfword is to be received into or sent from the ping buffer.

It is automatically reset when the end-of-chain has been sent to the CCU, or by a PIO selection (TA time).

X'02': IOC Bus Service

This register reflects the status of the IOC bus service tags to the microcode, and indicates the IOC bus check when parity errors are detected on the data. The bits are not checked for parity.

They have the following meaning:

Bit	Function
0	Read/write (input/output IOH) 0=write, 1=read
1	IOC bus check
2	Cycle steal grant
3	I/O tag
4	Halt
5	TA tag
6	TD tag
7	Interrupt priority check

Bit 0 Reflects the status of the read/write bit (IOC bus byte 1 bit 7) of a PIO or cycle steal operation:

OFF Indicates a write operation.
ON Indicates a read operation.

Bit 1 Set when the TA and TD tags are active at the same time, or a data parity check occurs.

Bit 2 Used by the microcode to read the status of the cycle steal grant on the IOC bus.

Bit 3 Used by the microcode to read the status of the I/O tag on the IOC bus.

Bit 4 Set when the halt tag is active. When the bit is ON, the IOC bus status is frozen, a level 0 interrupt to the CSP occurs, and the IOC tag drivers are disabled.

Bit 5 Used by the microcode to read the status of the TA tag on the IOC bus.

Bit 6 Used by the microcode to read the status of the TD tag on the IOC bus.

Bit 7 Set when the priority latch, the disable IOC bus latch, the halt latch, or the reset latch is set. No level 0 interrupt is requested.

During diagnostics, this register is isolated from the IOC bus. All bits except bit 7 can be set and reset by the microcode. Bit 4 means TD tag.

X'03': CSP Error

This register reports the CSP errors. The bits are not checked for parity.

Bit	Description	Result in
0	Unexpected adapter acknowledge	Hard Stop
1	Control storage data write check	
2	Processor check	
3	External register address check	
4	Control storage address check	
5	Local storage address check	
6	Adapter interconnection check	Level 0
7	Level 0 adapter interrupt check	

Bit 0 Set when an acknowledge signal is erroneously received from the FESL while one external register in the CSP address range is accessed.

Bit 1 Set when a parity check is detected during a control storage write operation. It is reset by the microcode.

Bit 2 Set when the error line is active in the CSP.

Bit 3 Set when a parity check is detected on the external register address bus.

Bit 4 Set when a parity check is detected in the control storage address bus (CS address check) or when a double bit error is detected.

Bit 5 Set when a parity check is detected in the local storage address bus.

Bit 6 Set when the acknowledge signal from the FESL is not received.

Bit 7 Set when a CSP interrupt level 0 is requested by the FESL.

X'04': Miscellaneous/Adapter Address

This register provides the microcode with miscellaneous IOC bus controls. The bits are not checked for parity.

They have the following meaning:

Bit	Function
0	Timer pulse read
1	Programmed reset (Reset 1)
2	Latch and FESL reset (Reset 2) (POR)
3	Disable hardstop
4	Valid byte
5	IOC bus disable
6	Adapter address
7	Cycle steal request

Bit 0 Reflects the status of the 100 ms timer pulse.

Bit 1 Set when a programmed reset command is decoded at the IOC data bus level.

Reset 1 and Reset 2 Encoding

Rest 1 Bit	Reset 2 Bit	Function Performed
0	1	Power ON reset
0	1	Programmed reset
1	1	Tag reset

Bit 3 Set by a programmed reset command or a general reset from the CCU. It disables the CSP hardstop, and is reset by the microcode.

Bit 4 Indicates that the last data transferred is a byte.

Bit 5 Set at power ON reset or by the microcode. When it is ON, the IOC bus is disabled and external register X'02' is isolated from the IOC bus.

Bit 6 Used by the microcode to address the FESL.

Bit 7 Reflects the status of the cycle steal request at the IOC bus.

X'05': External Interrupt Request/Priority

This register controls the MOSS and CCU interrupts requested by the CSP. The CCU interrupts are reported via the data bytes of the IOC bus. The bits are not checked for parity.

Bit	Function
0	MOSS interrupt request (level 4)
1	CCU level 1 interrupt request
2	CCU level 2 interrupt request
3	Level 1 interrupt wrap read
4	Level 2 interrupt wrap read
5	Level 2 and cycle steal priority
6	Diagnostic priority compare
7	Line ID to CCU

Bit 0 Used by the CSP microcode to request an interrupt to the MOSS. It is reset by the CSP microcode.

Bit 1 Causes a level 1 interrupt to the CCU.

Bit 2 Causes a level 2 interrupt to the CCU.

Bit 3 Gives the state of the level 1 interrupt to the CCU.

Bit 4 Gives the state of the level 2 interrupt to the CCU.

Bit 5 Set by the microcode to indicate a high priority level associated with the level 2 or cycle steal request.

Bit 6 Reflects the output of the level 2/cycle steal priority compare circuit.

Bit 7 Handles the process of the fast get line ID. It prevents the microcode to load a new line ID in the X'0A' and X'0B' register if the line ID is is not yet processed.

It is set by microcode after the loading of the line ID in registers X'0A' and X'0B'.

This bit can be set and reset by microcode.

X'07': Sync/Configuration Data Set

This register can be used for clock check. It also provides the scanner configuration to the microcode. The bits are not checked for parity.

Bit	Function
0	Channel request bit
1	100-ms interval timer
2	Sync 1
3	ECC disable
4	Fast get line ID selection
5	ROS extension
6	EC level bit 0
7	EC level bit 1

Bit 0 Set by the microcode to prevent any PIO operation at the beginning of a cycle stealing operation.

Bit 1 Set by the 100-ms timer pulse from the CCU.

Bit 2 Set by the microcode and causes a 200-ns pulse to be sent on the top connector side). This pulse is used for maintenance purposes by the diagnostics.

Bit 3 When ON allows to get 16 data bits from the storage with the ECC mechanism inactive.

The ECC disable is active this bit is ON and bit 4 is OFF.

Bit 4

ON Allows the selection of the fast get line ID function.
OFF The microcode get line ID function is invoked instead of the fast get line ID.

Bit 5 When ON, allows to use the the ROS over four Kbytes for diagnostic.

Bits 6 and 7
These two bits are used to record the EC number and are incremented after each new EC.

X'0A' and X'0B': Line Address Byte 0 and Byte 1

These two registers store the line address put on the IOC bus at TD time, during the get line ID operation. They are loaded by the microcode before the level 2 interrupt is sent to the CCU.

The parity is provided by the scanner processor.

Inhibit data check signal is raised when the registers are read. X'0A' Register Contents (Line Address Byte 0).

Bit	Function
0	Line ID byte 0 bit 0)
1	Line ID byte 0 bit 1)
2	Line ID byte 0 bit 2) High byte
3	Line ID byte 0 bit 3)
4	Line ID byte 0 bit 4) of line ID
5	Line ID byte 0 bit 5)
6	Line ID byte 0 bit 6)
7	Line ID byte 0 bit 7)

X'0B' Register Contents (Line Address Byte 1)

Bit	Function
0	Line ID byte 1 bit 0)
1	Line ID byte 1 bit 1)
2	Line ID byte 1 bit 2) Low Byte
3	Line ID byte 1 bit 3)
4	Line ID byte 1 bit 4) of line ID
5	Line ID byte 1 bit 5)
6	Line ID byte 1 bit 6)
7	Line ID byte 1 bit 7)

X'10': Extended Interrupt Request

This register reports FES interrupts when X'12' bits 0 and 1 are ON. The CSP can only read this register. The bits are not checked for parity if bit 0 is on.

If X'10' bit 0 is:

ON The contents of the X'10' reports errors detected by FESL.
OFF The contents of the X'10' reports other interrupt conditions.

Bit 0 = 0: Various Conditions

Bit	Function
1	Overrun or underrun
2	Time out (transmit)
3	Modem change
4	Ending configuration/transparency Ending/end of transmission
5-6	(Not used)
7	Forced to 1

Bit 0=1: Errors

Bit	Function
1	FES/FESA error
2	(Not used)
3	FES internal error
4	CSP/FES error
5-7	(Not used)

X'12': Interrupt Request

This register contains the address of the line interface that requested a CSP interrupt. The bits are checked for parity.

Bit	Function
0-1	Data/read X'10'
2	Line interface address bit 0
3	Line interface address bit 1
4	Line interface address bit 2
5	Line interface address bit 3
6	Line interface address bit 4
7	Line interface address bit 5 (see note below)

Bits 0 and 1

Set by hardware to indicate that X'10' contains interrupt information and must be read immediately afterwards.

Bits 2 through 7

Contain the line interface address.

Note: Bit 7 is set OFF for a transmit line interface, and ON for a receive line interface.

X'13': Line Interface Address (Read/Write)

This register is set by the microcode during CSP asynchronous operations (read or write) in the FESL inbound and outbound RAMs, to specify the line interface address. The bits are checked for parity.

Bit	Function
0-1	(Not used, set to 00)
2	Card address 0
3	Card address 1
4	Card address 2
5	Line interface address bit 0
6	Line interface address bit 1
7	FESA register addressing bit X (see Note below)

Note: This bit is bit 'X' for the “FESA Inbound/Outbound RAMs Addressing” on page 4-33.

Bits 2 through 7

Contain the line interface address (card address bits 0, 1, 2 and line address bits 0, and 1). Bit 7 is set OFF for a transmit line interface (outbound), set ON for a receive line interface (inbound).

X'14': Data In/Out

This register is used by the microcode for transferring data to be loaded into, or coming from the FESL, the MUX or the LICs during asynchronous operations.

The bits are checked for parity.

They are not described because the X'14' register is used as a data buffer.

In write operations relative to the FESA, the MUX or the LICs, bit 7 must be set to zero.

X'15': Asynchronous Operation Command

This register is used by the microcode to specify to the FESL RAMS (A, B, C, or FESA inbound/outbound) the asynchronous operation to be executed.

Depending on the value of bits 1 and 2, the RAM A, B, C are addressed (00, 01, 11) or the FESA RAMS inbound/outbound are addressed (11). The bits are checked for parity.

Bits 1 and 2 = 00, 01 or 10

Bit	Function
0	OFF = read, ON = write operation
1-2	RAM A, B, C, or FESA RAMs to be accessed
3	OFF = byte 0, ON = byte 1
4-5	00, 01, 10, 11 (Halfword 0, 1, 2, 3)
6-7	(Not used)

Bit 0 Set by the microcode to indicate a write operation. It is reset to indicate a read operation.

Bits 1 and 2
Set by the microcode to indicate:

01 RAM A access
00 RAM B access
10 RAM C access
11 FESA RAMS inbound/outbound access

Bit 3 Set by the microcode to indicate FES RAM access:

0 Even byte
1 Odd byte.

Bits 4 and 5
Set by the microcode to indicate FES RAM halfword displacement address:

00 Halfword 0
01 Halfword 1
10 Halfword 2
11 Halfword 3

If bits 4 and 5 are set to 11, the diagnostic register of the FESL is accessed.

Bits 1-2 = 11

Bit	Function
0	OFF = read, ON = write operation
1-2	If 11: FESA RAMs to be accessed
3	Bits 'I' of the FESA register addressing (if bits 1-2=11)
4-5	Bits 'R,R' of the FESA register addressing (if bits 1-2 = 11) (see note below)
6-7	(Not used)

Note: See “FESA Inbound/Outbound RAMs Addressing” on page 4-33

Bit 0 Set by the microcode to indicate a write operation. It is reset to indicate a read operation.

Bits 1 and 2
Set by the microcode to indicate:

01 RAM A access
00 RAM B access

10 RAM C access
11 FESA, MUX, LIC or FES diagnostic register

Bit 3 Set by the microcode to indicate FES RAM access:

0 Even byte
1 Odd byte.

For the other cases, refer to “FESA Inbound/Outbound RAMs Addressing” on page 4-33 (bit 'I').

Bits 4 and 5
Set by the microcode to indicate FES RAM halfword displacement address.

For the other cases, refer to “FESA Inbound/Outbound RAMs Addressing” on page 4-33 (bits 'R, R').

Bits 4 and 5 are set to 11 to access the diagnostic register of the FES.

X'16': Asynchronous Operation Status

This register gives the status of the last asynchronous operation initiated by the microcode. It can be reset by a microcode write operation. In a read operation, if bit 1 is equal to 1, the bits are not checked for parity.

Bit	Function
0	Data exchange not complete
1	Error during data exchange
2-3	(Not used)
4	FES/FESA error
5	FES internal error
6-7	(Not used)

Bit 0 Set by hardware during asynchronous operations when the microcode specifies a command via register X'15'. It is reset when the operation is complete.

Bit 1 Set by hardware when an error occurs during data byte processing.

Bits 4 and 5
When bit 1 is set, bits 4 and 5 indicate the type of error that occurred.

Bits 1, 4, and 5 can be reset either by the microcode or when the asynchronous operation that follows is executed without error.

X'17': FES General Commands

This register receives the FES general commands sent from the CSP. The bits are not checked for parity.

Bit	Function
0	Reset FES latches and disable CSP/FES interface
1	Reset FES storage
2	Freeze state
3	(Not used)
4	FES storage reset error
5	FESL card EC number
6	Set to 0
7	FESL card EC number

Bit 0 Set by the microcode to reset the FES latches and disable the CSP/FES. The FES RAM information is not reset. This command resets the FESA, the MUX, and the LICs.

Bit 1 Set by the microcode to reset the FES storage or set by the hardware after 'reset adapter'. It is set OFF by hardware when the reset is completed.

Bit 2 Set by the microcode to stop the FES scanning at the end of the current line process by the scanner base. All storage and register information is kept. Resetting bit 2 restarts the scanning.

Bit 4 Set by the hardware to report any error detected during FES storage reset, or FES synchronous work.

Bits 5 and 7
FESL card EC number set by the hardware.

Bit 6 Set to 0 by the hardware (FESL identification)

X'19': CSP Interrupt Request

This register contains pending CSP interrupt requests. The bits are not checked for parity.

Bit	Function
0	Set level 0
1	Set level 1
2	Set level 2
3	Set level 3 (PCI)
4	Set level 4 (PCI)
5	Set level 5 (PCI)
6	Level 2
7	Level 2 FESA

Bits 0 through 5
Set by the hardware or the microcode to request an interrupt from the CSP.

- When several interrupt requests are presented at the same time, the highest unmasked level is taken into account.
- When all bits 0 through 5 are OFF, the microcode runs at level 7.

Bit 6 This bit is set ON when the level 2 interrupt request line coming from the FESL is active. It is reset by the microcode.

Bit 7 This bit is set ON when the level 2 interrupt request line coming from the FESA is active. It is reset by the microcode.

This bit can be set by the microcode.

X'1A': Current CSP Interrupt Level

This register contains the current CSP interrupt level and stacks this level when a level 0 occurs.

The bits are checked for parity and have the following meaning:

Bit	Function
0	Current level stack parity bit
1	Current level stack bit 0)
2	Current level stack bit 1) if level 0
3	Current level stack bit 2)
4	Current level parity bit
5	Current level bit 0
6	Current level bit 1
7	Current level bit 2

Bits 0 through 3
Set by the hardware to stack the current interrupt level when a CSP level 0 interrupt occurs.

Bits 4 through 7
Represent the current interrupt level.

X'1B': Address Compare Control

This register controls the address compare function of the CSP. The bits are not checked for parity.

Bit	Function
0	Address compare hit if 4/5/6/7
1	Address compare hit if 6/7
2	(Not used)
3	(Not used)
4	Instruction/data fetch
5	Data storage
6	Cycle steal fetch
7	Cycle steal storage

Bit 0 Set by the hardware when the control storage address compares with the address contained in external registers '1C' and '1D', and if any X'1C' or X'1D' bit 4-7 is ON.

When ON, this bit requests a level 0 interrupt from the CSP.

Bit 1 Set by the hardware when the control storage address compares with the address contained in external registers '1C' and '1D', and if any X'1C' or X'1D' bit 6-7 is ON. Bit 0 is set at the same time.

Bit 4 Set by the microcode to ask for an address compare during instruction or data fetch. Bit 0 is set ON if the address compare is detected.

Bit 5 Set by the microcode to ask for an address compare during a data storage instruction.

- Bit 0 is set ON if the address compare is detected.
- Bit 5 is reset by the microcode.

Bit 6 Set by the microcode to ask for an address compare during a cycle steal fetch.

Bits 0 and 1 are set ON if the address compare is detected.

Bit 7 Set by the microcode to ask for an address compare during cycle steal store.

Bits 0 and 1 are set ON if the address compare is detected.

X'1C': Address Compare Byte 0

This register contains byte 0 of the address to be compared with the actual control storage address.

The bits are checked for parity.

Bit	Function
0	Main storage address high 0
1	Main storage address high 1
2	Main storage address high 2
3	Main storage address high 3
4	Main storage address high 4
5	Main storage address high 5
6	Main storage address high 6
7	Main storage address high 7

X'1D': Address Compare Byte 1

This register contains byte 1 of the address to be compared with the actual control storage address.

The bits are checked for parity.

Bit	Function
0	Main storage address low 0
1	Main storage address low 1
2	Main storage address low 2
3	Main storage address low 3
4	Main storage address low 4
5	Main storage address low 5
6	Main storage address low 6
7	Main storage address low 7

X'1E': CSP Interrupt Masks

This register uses masks to control CSP interrupts.

The bits are checked for parity.

Bit	Function
0	Mask interrupt level 0
1	Mask interrupt level 1
2	Mask interrupt level 2
3	Mask interrupt level 3
4	Mask interrupt level 4 (Not used)
5	Mask interrupt level 5 (Not used)
6	(Not used)
7	Master mask

Bits 0 through 5
Control the masking of levels 0 through 5.

Bit 7 Masks all levels except level 0 and the current level.

X'1F': Local Storage Address

This register contains the primary (bits 0 through 3) and secondary (bits 4 through 7) local storage address.

The bits are checked for parity.

Bit	Function
0	Primary local storage address: (primary page)
1	Bit 0
2	Bit 1
3	Bit 2
	Bit 3
4	Secondary local storage address: (secondary page)
5	Bit 0
6	Bit 1
7	Bit 2
	Bit 3

FES RAM A Description

RAM A Receive

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	New PDF	SCF
1	Stacked PDF	Interrupt request
2	Control storage addressing	
3 3	Scanner base control parameters	Timer

Parallel Data Field (PDF)

The stacked PDF and the new PDF contain the next two characters to be loaded into the control storage of the CSP.

Secondary Control Field (SCF)

Bit	Function
8	End 1
9	Character service request
10	Overrun detected
11	Modem-in change detected
12	End 2
13	End 3
14	(Not used)
15	Timer forced to 3 s (BSC)

Bits 8, 12, and 13

Set by hardware to indicate to the microcode the status of the receive operation.

They are coded as follows, depending on the protocol:

Protocol	End Bit 1 2 3	Meaning
All	0 0 0	Data valid
Start-stop	1 0 0	Stop check
SDLC	0 0 1 0 1 1 1 0 1 1 0 0 1 1 0	Flag valid Flag off boundary Data check Abort Idle

Protocol	End Bit 1 2 3	Meaning
BSC	1 1 1 0 1 1 1 1 0 X 0 1 1 0 0	Force timer to 0 Normal text Transparent text Quit control or text Data check

Bits 9 and 10

Bit 9 is set by the front-end layer to request character service from the scanner base layer.

Bit 10 is set by the hardware to indicate an overrun condition (too many characters received) to the microcode. Bits 9 and 10 are associated as follows to indicate:

00 No scanner base operation
01 Overrun during character deletion (BSC)
10 Character service request
11 Overrun with characters lost

Bit 11 Set by the hardware to indicate a modem-in change.

Bit 15 In BSC, is set by the hardware to force the timer to three seconds to check that the SYN characters are separated by less than three seconds.

It is reset by the hardware.

Interrupt Request

Bit 8 = 0: Level 2 Interrupts (no error)

Bit	Function
9	Overrun
10	(Not used)
11	Modem-in change detected
12	End bit present in SCF
13	Interrupt pending
14	(Not used)
15	Forced to 1

Bit 8 = 1: Errors

Bit	Function
9	FES/FESA error
10	(Not used)
11	FES internal error
12	CSP/FES interface error
13	Interrupt pending
14-15	Forced to 0

Bit 8 Set by the hardware to indicate an error condition. It is OFF for other CSP level 2 interrupt conditions.

Bit 9 Set by the hardware to indicate an overrun when bit 8 is 0, or an FES or FESA error when bit 8 is 1.

Bit 11 This bit is set ON by the hardware to indicate a modem-in change when bit 8 is 0, or an FES internal error when bit 8 is 1.

Bit 12 Set by the hardware to indicate that an end bit is present in the SCF when bit 8 is 0, or to indicate a CSP/FES interface error when bit 8 is 1.

Bit 13 Set by the hardware to indicate to the scanner base that an interrupt is to be processed.

Note: Bits 8 through 15 are reset by the scanner base when the interrupt has been processed.

Control Storage Addressing

Bit	Function
0-1	Buffer length
2-4	Set to 010
5-10	Buffer starting address
11-13	Burst number
14-15	Halfword number

Bits 0 and 1

Set by the microcode to indicate the buffer length:

00 32 bytes (4 bursts)
01 64 bytes (8 bursts)
10 128 bytes (16 bursts)
11 256 bytes (32 bursts)

Bits 2 through 4

PN of starting address, set to 010 by the microcode.

Bits 5 through 8, 9 or 10

Set by the microcode to indicate the buffer starting address to the FESL for cycle stealing.

Bits 9, 10 or 11 through 13

Used by the FES to increment the burst number.
The assignment of bits 5 to 13 depend on the specified buffer length (bits 0 and 1).

Bits 14 and 15

Used by the FES to increment the halfword number.
There are four halfwords (8 bytes) in one burst.

Scanner Base Control

This field is first loaded by the microcode to start the receive operation and to provide parameters for the current burst.

Then, parameters for the following bursts are taken from the parameter/status area of the CSP control store by cycle stealing, and loaded into this field by the hardware.

Parameters (Bit 0 = 0: Burst valid)

Bit	Function
1	Start receive operation
2	Interrupt requested
3	EP mode
4	Stacked PDF pointer
5-7	Burst length (in bytes)

Status (Bit 0 = 1: Burst not valid)

Bit	Function
1-7	Invalid information

Bit 0

OFF The current burst is free and valid for data cycle steal. The scanner base control field contains valid parameters in bits 1 through 7.

ON The current burst has not been processed by the microcode, and is not valid. The scanner base control field contains old status information in bits 1 through 7; this information is invalid.

Bit 1 Set by the microcode to start the receive operation in the scanner base layer. It is reset by the hardware.

Bit 2 Set to indicate that a level 2 interrupt must be raised to the CSP at the end of the burst.

Bit 3 Set to indicate that the line is working in emulation program mode.

In this mode, no interrupt level 2 to CSP is raised when the end bits is 011 or 110.

Bit 4 Set by the hardware to indicate that the stacked PDF is full. It is reset by the hardware.

Bits 5 through 7

Indicate the burst length in bytes.

Timer

Bit	Function
8	Timer active
9	Timer mode (100 ms/2 ms)
10	Clock service phase
11-15	Timer value

Bit 8 In BSC, set by the hardware to start the timer, and reset to stop the timer.

In other protocols, it can be set by the microcode to start the timer, and reset by the hardware at time out.

Bit 9 Set by the microcode to indicate the unit of time to be used for the timer:

0 100 ms
1 2 ms

Bit 10 Set by the hardware and, used for internal processing of the timer. It is reset by the hardware.

Bits 11 through 15

In BSC, set and incremented by the hardware to:

- Manage the insertion of a SYN character every second in transmit
- Check for the occurrence of the SYN character every 3 seconds (or less) in receive. This field is reset by the hardware at the end of the operation.

In other protocols, bits 11 through 15 can be set by the microcode to provide the timer value according to the unit specified via bit 9.

RAM A Transmit

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Timer control	SCF
1	Next PDF	Interrupt request
2	Control storage addressing	
3	Scanner base control (parameters)	

Timer Control

Bit	Function
0	SYN insertion
1-7	(Not used)

Bit 0 Set by the microcode in BSC to allow the hardware to insert a SYN character every second in the transmitted data.

Secondary Control Field (SCF)

Bit	Function
8	(Not used)
9	Character service request
10	Underrun detected
11	Modem-in change detected
12	EOT sent
13	Transparency ending
14-15	(Not used)

Bits 9 and 10

- Bit 9 is set by the front-end layer to request character service from the scanner base layer.
- Bit 10 is set by the hardware to indicate an underrun condition (lack of characters) to the microcode.

When the FESL is in the underrun condition:

SDLC Abort followed by a continuous transmission of flags.
BSC SYN characters are transmitted
Start-stop
Mark bits are transmitted.

Bits 9 and 10 are associated to indicate:

00 No scanner base operation
01 Underrun without operation
10 Character service request
11 Underrun with cycle steal

Bit 11 Set by the hardware to indicate a modem-in change.

Bit 12 Set by the hardware to indicate that the EOT character has been transmitted.

Bit 13 Set by the hardware to indicate end of transparent text.

Next PDF

The next PDF contains the last character fetched from the control storage (and the next to be transmitted).

Interrupt Request

Bit 8 = 0: Level 2 interrupts (no error)

Bit	Function
9	Underrun
10	Time out
11	Modem-in change detected
12	Transparency ending or EOT
13	Interrupt pending
14	(Not used)
15	Forced to 1

Bit 8 = 1: Errors

Bit	Function
9	FES/FESA error
10	(Not used)
11	FES internal error
12	CSP/FES interface error
13	Interrupt pending
14	Forced to 0
15	Forced to 0

Bit 8 Set by the hardware to indicate an error condition. It is OFF for the other CSP level 2 interrupt conditions.

Bit 9 Set by the hardware to indicate an underrun when bit 8 is 0, or an FESL or LIC error when bit 8 is 1.

Bit 10 Set by the hardware to indicate that the timer has reached the time out, when bit 8 is 0.
Not used when bit 8 is 1.

Bit 11 Set by the hardware to indicate a modem-in change when bit 8 is 0, or an FES internal error when bit 8 is 1.

Bit 12 Set by the hardware to indicate the end of the transparent text (BSC) when bit 8 is 0, or to indicate a CSP/FES interface error when bit 8 is 1.

Bit 13 Set by the hardware to indicate to the scanner base that an interrupt is to be processed.

Bits 8 through 15 are reset by the scanner base when the interrupt has been processed.

Control Storage Addressing

Bit	Function
0-1	Buffer length
2-4	Set to 010
5-10	Buffer starting address
11-13	Burst number
14-15	Halfword number

Bits 0 and 1

Set by the microcode to indicate the buffer length:

00 32 bytes (4 bursts)
01 64 bytes (8 bursts)
10 128 bytes (16 bursts)
11 256 bytes (32 bursts)

Bits 2 through 4

PN of starting address, set to 010 by microcode.

Bits 5 through 8, 9 or 10

Set by the microcode to indicate the buffer starting address to the FESL for cycle stealing.

Bits 9, 10 or 11 through 13

Used by the FESL to increment the burst number.
The assignment of bits 5 to 13 depends on the specified buffer length (bits 0 and 1).

Bits 14 and 15

Used by the FESL to increment the halfword number.
There are four halfwords (8 bytes) in one burst.

Scanner Base Control

Parameters (Bit 0 = 0: Burst valid)

Bit	Function
1	Start transmit operation
2	Interrupt requested
3	Modem-in change detected
4	Stacked PDF pointer
5-7	Burst length (in bytes)
8	Send CRC / start at mark
9	Start on odd byte
10	(Not used)
11-12	Transmit operation specification
13	Option protocol
14	Start timer
15	Send modem-out stacked

Bit 1 Set by the microcode to start the transmit operation. It is reset by the hardware.

Bit 2 Set to indicate that a CSP level 2 interrupt must be requested at the end of the burst.

Bit 3 Set by the hardware to indicate a modem-in change during data transmission. The modem-in status will be examined at the next CSP interrupt.

Bit 4 Set by the hardware to indicate that the stacked PDF is available for next character request. It is reset by the hardware.

Bits 5 through 7
Indicate the burst length in bytes.

Bit 8 When ON, it causes the CRC to be sent at the end of the burst (SDLC) or forces the start bit at mark (start-stop).

Bit 9 When ON, it causes transmission to start with the odd byte of the first halfword of the current burst.

Bits 11 and 12
Specify the transmit operation as follows:

00 Normal
01 End of message
10 Transmit continuous
11 End of message with turnaround

Bit 13 Specifies the following protocol options:

SDLC No zero insert
SS Transmit break
BSC Transparency end

Bit 14 When ON, starts the timer at burst end or end of transmission.

Bit 15 When ON, requests the modem-out stacked pattern to be sent on the line interface at end of burst.

FES RAM B Description

RAM B Receive

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	SDF	SCF
1	PDF	PCF
2	Spare	Spare
3	SYN 1	SYN 2

Serial Data Field (SDF)

This field is used for the deserialization of the bits received from the 'receive data' line via the LIC.

Secondary Control Field (SCF)

Bit	Function
8	End 1
9	Bit counter 2
10	Bit counter 1
11	Modem-in change detected
12	End 2
13	End 3
14	Bit counter 0
15	(Not used)

Bits 8, 12 and 13

Set by the hardware to indicate to the microcode the end of data transfer. They are coded according to the next table, depending on the protocol:

Protocol	End Bit 1 2 3	Meaning
All	0 0 0	Data valid
Start-stop	1 0 0	Stop check
SDLC	0 0 1 0 1 1 1 0 1 1 0 0 1 1 0	Flag valid Flag off boundary Data check Abort Idle
BSC	1 1 1 0 1 1 1 1 0 X 0 1 1 0 0	Force timer to 0 Normal text Transparent text Quit control or text Data check

Bit 9, 10, and 14
Set by the hardware to count the bits in the SDF.
They are reset by the hardware at the end of the character.

Bit 11 Set by the hardware to indicate a modem-in change.

Parallel Data Field (PDF)

This field contains one character after deserialization.

Primary Control Field (PCF)

Bit	Function
8	End 1
9	Character service request
10	Overrun detection
11	Modem-in change detected
12	End 2
13	End 3
14	Start receive operation
15	Force timer to 3 seconds (BSC)

Bits 8, 12, and 13
Indicate the end of data transfer and are coded according to the next table, depending on the protocol:

Protocol	End Bit 1 2 3	Meaning
All	0 0 0	Data valid
Start-stop	1 0 0	Stop check
SDLC	0 0 1 0 1 1 1 0 1 1 0 0 1 1 0	Flag valid Flag off boundary Data check Abort Idle
BSC	1 1 1 0 1 1 1 1 0 X 0 1 1 0 0	Force timer to 0 Normal text Transparent text Quit control or text Data check

Bits 9 and 10
Set by hardware to indicate:

- **00** Not used
- **01** Overrun during character deletion (BSC)
- **10** Character service
- **11** Overrun with characters lost

Bit 11 Set by the hardware to indicate a modem-in change.

Bit 14 Set by the hardware to memorize the start bit set in RAM A (scanner base control bit 1), to start the receive operation.

Bit 15 Set by the hardware to force the timer to 3 seconds, for BSC SYN character monitoring. It is reset by the hardware.

Synchronization

This field contains the SYN characters used during reception of BSC characters.

These characters vary depending on the protocol: in BSC ASCII, they are X'16', in BSC EBCDIC they are X'32'.

RAM B Transmit

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	SDF	SCF
1	PDF	PCF
2	DLE	Spare
3	SYN	Spare

Serial Data Field (SDF)

This field is used to serialize the character to be transmitted over the transmit data line via the LIC.

Secondary Control Field (SCF)

Bit	Function
8	Send CRC or force start at mark
9	Bit counter 2
10	Bit counter 1
11	Modem-in change detected
12	End of transmission
13	SDLC : no zero insert BSC : transparency end SS : transmit break
14	Bit counter 0
15	Send modem-out stacked

Bit 8 Set by the hardware to memorize that the CRC is to be sent at the end of the burst (SDLC) or that the start bit must be forced at mark (start-stop).
It is reset by the hardware.

Bit 9, 10, and 14
Set by the hardware to count the bits in the SDF. They are reset by the hardware at the end of the character.

Bit 11 Set by the hardware to indicate a modem-in change and prevent starting the transmission until the modem-in status is processed by the micro-code.

Bit 12 Set by the hardware to memorize the end of transmission. It is reset by the hardware.

Bit 13 Set by the hardware to memorize the selected protocol options.

Bit 15 Set by the hardware to memorize that the modem-out stacked pattern is to be sent on the line interface. It is reset by the hardware.

Parallel Data Field (PDF)

This field contains one character before serialization.

Primary Control Field (PCF)

Bit	Function
8	Send CRC or force start at mark
9	Character service request
10	Underrun detection
11	Modem-in change detected
12	End of transmission
13	SDLC : no zero insert BSC : transparency end SS : transmit break
14	Start transmit operation
15	Send modem-out stacked

Bit 8 Set by the hardware to memorize that the CRC is to be sent at the end of the burst (SDLC) or that the start bit must be forced at mark (start-stop).
It is reset by the hardware.

Bit 9 Set by the hardware to request a new character.

Bit 10 Set by the hardware to report underrun.

Bit 11 Set by the hardware to indicate a modem-in change and prevent starting the transmission until the modem-in status is processed by the micro-code.

Bit 12 Set by the hardware to memorize the end of transmission. It is reset by the hardware.

Bit 13 Set by the hardware to memorize the selected protocol options.

Bit 14 Set by the hardware to memorize the start bit set in RAM A (scanner base control bit 1), to start the transmit operation.

Bit 15 Set by the hardware to memorize that the modem-out stacked pattern is to be sent on the line interface. It is reset by the hardware.

Data Link Escape (DLE)
This field contains the data link escape (DLE) character used in BSC transmission.

Synchronization (SYN)
This field contains the SYN characters used during the transmission of BSC characters.

These characters vary depending on the protocol; in BSC ASCII they are X'16', in BSC EBCDIC they are X'32'.

FES RAM C Description

The fields of the FES storage RAM C are described bit-by-bit in this section.

Line Type Identification

In the following descriptions, use bits 0, 1, and 2 of the set mode byte to select the right RAM C description.

Set Mode	RAM C Description
00x	BSC ASCII
01x	BSC EBDCIC
100	BSC normal
101	Start-stop
11x	SDLC

SDLC Receive

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Set mode	Control
1	BCC2	BCC1
2	Modem-in pattern	Mask
3	Spare	Spare

Set Mode

Bit	Function
0-1	Line protocol: SDLC
2	Interrupt on first flag
3	Non-zero delete option
4	NRZI
5-7	Ones counter

Bits 0 and 1
Set to 11 by the microcode to indicate that the line uses the SDLC protocol.

Bit 2 Set by the microcode to request a CSP level 2 interrupt when the first SDLC flag is detected.

Bits 3 Set by the microcode to indicate the zero delete option:

0 Zero delete option
1 Non-zero delete option

Bit 4 Set by the microcode to indicate the non-return to zero inverted (NRZI) option:

0 No NRZI option
1 NRZI option

Bits 5 through 7

Set by the hardware to count the 1 bits received in order to detect SDLC flags, abort characters, and idle characters.

Control

Bit	Function
8	(Not used)
9	Character phase
10	First bit time
11-12	SDLC state
13	Last line state
14-15	Line state

Bit 9 Set by the hardware when the first character is detected. It is reset by the hardware when the ending flag is received.

It may be set ON by the microcode to request the bit service function to return all incoming bits in bytes, without taking true character boundaries into account.

Bit 10 Set by the hardware when the first bit of a character is detected. It is reset by the hardware when the last bit is detected.

Bits 11 and 12

Initialized by the microcode and updated by the hardware to indicate the SDLC state:

00 Data phase
01 First flag detected
10 Abort detected
11 Idle detected

Bit 13 Updated by the hardware to indicate the last state of the data bit on the line: 0 or 1. It is used with the NRZI option only.

Bits 14 and 15

Initialized by the microcode and updated by the hardware to indicate the line state in the FES:

00 Inhibited
01 Diagnostic mode
10 Modem without data
11 Modem and data

Block Check Character (BCC)

These fields (BCC1 and BCC2) are used for CRC checking (SDLC- BSC) or for synchronization search (BSC).

Modem-In

Bit	Function
0	V.24: Data set ready V.25: Power indication X.21: (Not used)
1	V.24: Ready for sending V.25: Data line occupied X.21: Indication

Bit	Function
2	V.24: Ring indicator V.25: Present next digit X.21: Controlled not ready state
3	V.24: Receive line signal detector V.25: Abandon call and retry X.21: Steady state detect
4	V.24: Test indicator V.25: Call origination status X.21: Clear to confirm by FESA
5	V.24: Received data V.25: (Not used) X.21: Receive
6-7	Modem-in change detected

Bits 0 through 5

Modem-in status.

Bits 6 and 7

Set when a change is detected with respect to the mask pattern.

Other changes are no longer detected until the microcode has processed the new modem-in pattern and reset bits 6 and 7.

Mask

Bit	Function
8-13	Mask bits
14	Start conditional
15	No modem change report in receive

Bits 8 through 13
Set by the microcode to monitor the modem-in pattern for changes. A mask bit set to 1 means 'look for a change'.

Bit 14 Set by the microcode to start the receive operation only if the modem is ready.

Bit 15 Set by the microcode to select the transmit line interface for modem-in change reporting. No modem-in change is reported on the receive line interface.

SDLC Transmit

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Set mode	Control
1	BCC2	BCC1
2	Modem—out immediate	Mask (00)
3	Modem—out stacked	Mask (00)

Set Mode
As for receive, except bit 3 which is Not used.

Control

Bit	Function
8	(Not used)
9	Modem-in change detected
10	First bit time
11	Underrun
12	BCC1 sent
13	Last line state
14-15	Line state

Bit 9 Set by the hardware to memorize a modem-in change during data transmission for reporting to the microcode by a level 2 interrupt.

Bit 9 is reset by the hardware after processing.

Bit 10 Set by the hardware when the first bit of a character is transmitted. It is reset by the hardware at the end of the bit time.

Bit 11 Set by the hardware to memorize an underrun condition. It is reset by the hardware when the underrun condition disappears.

Bit 12 Set by the hardware to indicate that BCC1 is being transmitted. It is reset by the hardware when BCC2 is sent.

Bit 13 Updated by the hardware to indicate the last state of the data bit on the line: 0 or 1. It is used with the NRZI option only.

Bits 14 and 15
Initialized by the microcode and updated by the hardware to indicate the line state:

00 Inhibited
01 Diagnostic mode
10 DCE without data
11 DCE and data

Block Check Character (BCC)

These fields (BCC1 and BCC2) are used for CRC computation.

Modem-Out

Bit	Function
0	V.24: Data terminal ready V.25: Digit signal 8 X.21: (Not used)
1	V.24: Request to send V.25: Digit signal 4 X.21: Control
2	V.24: New synchronization V.25: Digit signal 2 X.21: (Not used)
3	V.24: Data rate selector V.25: Digit signal 1 X.21: Transmit enable
4	V.24: Modem test V.25: Call request X.21: (Not used)
5	V.24: Modem-out not synchronized/diag clock V.25: Digit present X.21: Modem-out not synchronized/diag clock
6-7	Counter

Bits 0 through 5
Modem-out status.

Bits 6 and 7
Incremented each time a modem-out pattern is sent to the FESA.

Mask

Bit	Function
8-13	(Not used)
14	Start conditional
15	(Not used)

Bit 14 Set by the microcode to start the transmit operation only when the modem is ready.

BSC Receive

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Set mode	Control
1	BCC2	BCC1
2	Modem-in pattern	Mask
3	Spare	Spare

Set Mode: BSC, Normal

Bit	Function
0-2	Line type: BSC normal
3-4	(Not used)
5	One SYN character
6-7	Character length

Bits 0 through 2
Set to 100 by the microcode to indicate that the line type is BSC normal.

Bit 5 Set by the microcode to indicate that the hardware must synchronize on only one character. When OFF, it indicates that two SYN characters must be searched.

Bits 6 and 7
Set by the microcode to indicate the character length:

00 Five bits
01 Six bits
10 Seven bits
11 Eight bits

Set Mode: BSC, ASCII or EBCDIC

In BSC ASCII or EBDCIC mode, the data is exchanged character by character.

Bit	Function
0-1	Line type: BSC, ASCII or EBCDIC
2-3	ITB/EIB encoding
4-5	CRC type
6	ASCII 8-bits

Bits 0 and 1

Set by the microcode to indicate the line type:

00 BSC ASCII
01 BSC EBCDIC

Bits 2 and 3

Set by the microcode to indicate the ITB/EIB status:

00 ITB is data
01 ITB mode
10 EIB mode
11 EIB mode with burst change

Bits 4 and 5

Indicate the CRC type as follows:

00 STX included
- CRC/S if ASCII
- CRC/B if EBCDIC

01 CRC/B
10 CRC/S
11 LRC with VRC (ASCII 7-bits)

Bit 6 Set by the microcode to indicate ASCII 8-bits.

Control

Bit	Function
7	D (ASCII or EBCDIC)
8	S (ASCII or EBCDIC)
9	Character phase
10	First bit time
11	C (ASCII or EBCDIC)
12-13	NX (ASCII or EBCDIC)
14-15	Line state

Bit 7 In BSC ASCII or EBCDIC, it is set by the hardware when a DLE character is detected. It is reset by the hardware.

Bit 8 In BSC ASCII or EBCDIC, it is set by the hardware when a SYN character is detected. It is reset by the hardware.

Bit 9 Set by the hardware when the first character is detected. It is reset by the hardware when no more characters are received.

It may be set ON by the microcode to request the bit service function to return all incoming bits in bytes without true character boundaries.

Bit 10 Set by the hardware when the first bit of a character is detected. It is reset by the hardware at the end of the bit time.

Bit 11 In BSC ASCII or EBCDIC, it is set by the hardware when checking the ending pad, or in case of data check. It is reset by the hardware.

Bits 12 and 13

In BSC ASCII or EBCDIC, they are set by the hardware to indicate the status of NX as follows:

00 Sync or control mode
01 Transparent text mode

10 Normal text mode
11 CRC phase

Bits 14 and 15

Initialized by the microcode and updated by the hardware to indicate the line state in the FES:

00 Inhibited
01 Diagnostic mode
10 DCE without data
11 DCE and data

Block Check Character (BCC)

These fields (BCC1 and BCC2) are used for CRC checking.

Modem-In

Bit	Function
0	V.24: Data set ready V.25: Power indication X.21: (Not used)
1	V.24: Ready for sending V.25: Data line occupied X.21: Indication
2	V.24: Ring indicator V.25: Present next digit X.21: Controlled not ready state
3	V.24: Receive line signal detector V.25: Abandon call and retry X.21: Steady state detect
4	V.24: Test indicator V.25: Call origination status X.21: Clear to confirm by FESA
5	V.24: Received data V.25: (Not used) X.21: Receive
6-7	Modem-in change detected

Bits 0 through 5

Modem-in status.

Bits 6 and 7

Set when a change is detected with respect to the mask pattern.

Other changes are no longer detected until the microcode has processed the new modem-in pattern and reset bits 6 and 7.

Mask

Bit	Function
8-13 14 15	Mask bits Start conditional No DCE change report in receive

Bits 8 through 13

Set by the microcode to monitor the modem-in pattern for changes. A mask bit set to 1 means 'look for a change'.

Bit 14 Set by the microcode to start the receive operation only if the modem is ready.

Bit 15 Set by the microcode to select the transmit line interface for modem-in change reporting. No modem-in change is reported on the receive line interface.

BSC Transmit

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Set mode	Control
1	BCC2	BCC1
2	Modem—out immediate	Mask
3	Modem—out stacked	Spare

Set Mode

Same as receive, except bit 5 which is not Not used in normal BSC.

Control

Bit	Function
7	D (ASCII or EBCDIC)
8	S (ASCII or EBCDIC)
9	Modem-in change detected
10	First bit time
11	C (ASCII or EBCDIC) or underrun (normal BSC)
12-13	NX (ASCII or EBCDIC)
14-15	Line state

Bit 7 In BSC ASCII or EBCDIC, it is set by the hardware when a DLE character is to be sent. It is reset by the hardware.

Bit 8 In BSC ASCII or EBCDIC, it is set by the hardware to control the CRC computation. It is reset by the hardware.

Bit 9 Set by the hardware to memorize a modem-in change during data transmission, for reporting to the microcode via a level 2 interrupt.

Bit 9 is reset by the hardware after processing.

Bit 10 Set by the hardware when the first bit of a character is transmitted.
It is reset by the hardware at the end of the bit time.

Bit 11 In BSC ASCII or EBCDIC, it is set by the hardware to control the CRC computation (ASCII or EBCDIC). It is reset by the hardware.

In normal BSC, it is set by the hardware to memorize an underrun condition.
It is reset by the hardware when the underrun condition disappears.

Bits 12 and 13

In BSC ASCII or EBCDIC, they are set by the hardware to indicate the status of NX as follows:

00 Sync or normal mode
01 Transparent text mode
10 Normal text mode
11 CRC phase

Bits 14 and 15

Initialized by the microcode and updated by the hardware to indicate the line state in the FES:

00 Inhibited
01 Diagnostic mode
10 DCE without data
11 DCE and data

Block Check Character (BCC)

These fields (BCC1 and BCC2) are used for CRC computation.

Modem-In

Bit	Function
0	V.24: Data set ready V.25: Power indication X.21: (Not used)
1	V.24: Ready for sending V.25: Data line occupied X.21: Indication
2	V.24: Ring indicator V.25: Present next digit X.21: Controlled not ready state
3	V.24: Receive line signal detector V.25: Abandon call and retry X.21: Steady state detect
4	V.24: Test indicator V.25: Call origination status X.21: Clear to confirm by FESA
5	V.24: Received data V.25: (Not used) X.21: Receive
6-7	Modem-in change detected

Bits 0 through 5

Modem-in status.

Bits 6 and 7

Set when a change is detected with respect to the mask pattern.

Other changes are no longer detected until the microcode has processed the new modem-in pattern and reset bits 6 and 7.

Mask

Bit	Function
8-13 14 15	Mask bits Start conditional No DCE change report in receive

Bits 8 through 13

Set by the microcode to monitor the modem-in pattern for changes. A mask bit set to 1 means 'look for a change'.

Bit 14 Set by the microcode to start the receive operation only if the DCE is ready.

Bit 15 Set by the microcode to select the transmit line interface for modem-in change reporting. No modem-in change is reported on the receive line interface.

Start-Stop Receive

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Set mode	Control
1	Spare	Spare
2	Modem—in pattern	Mask
3	Spare	Spare

Set Mode

Bit	Function
0-2	Line type: Start-stop
3	(Not used)
4	Stop length
5	(Not used)
6-7	Character length

Bits 0 through 2

Set to 101 by the microcode to indicate the line type start-stop.

Bit 4 Set by the microcode to indicate the stop length:

0 One bit
1 Two bits

Bits 6 and 7

Set by the microcode to indicate the character length:

00 Five bits
01 Six bits
10 Seven bits
11 Eight bits

The start and stop bits are not counted in the character length.

Control

Bit	Function
8	(Not used)
9	Character phase
10	First bit time
11-12	(Not used)
13	Stop phase
14-15	Line state

Bit 9 Set by the hardware when the start bit is detected. It is reset by the hardware at the character end.

It may be set ON by the microcode to request the bit service function to return all incoming bits without true character boundaries.

Bit 10 Set by the hardware when the first bit of a character is detected. It is reset by the hardware at the end of the bit time.

Bit 13 Set by the hardware to indicate that stop bits are being sent. It is reset by the hardware.

Bits 14 and 15

Initialized by the microcode and updated by the hardware to indicate the line state in the FES:

00 Inhibited
01 Diagnostic mode
10 Modem without data
11 Modem and data

Modem-In

Bit	Function
0	V.24: Data set ready V.25: Power indication X.21: (Not used)
1	V.24: Ready for sending V.25: Data line occupied X.21: Indication
2	V.24: Ring indicator V.25: Present next digit X.21: Controlled not ready state
3	V.24: Receive line signal detector V.25: Abandon call and retry X.21: Steady state detect
4	V.24: Test indicator V.25: Call origination status X.21: Clear to confirm by FESA
5	V.24: Received data V.25: (Not used) X.21: Receive
6-7	Modem-in change detected

Bits 0 through 5
Modem-in status.

Bits 6 and 7
Set when a change is detected with respect to the mask pattern.

Other changes are no longer detected until the microcode has processed the new modem-in pattern and reset bits 6 and 7.

Mask

Bit	Function
8-13	Mask bits
14	Start conditional
15	No DCE change report in receive

Bits 8 through 13
Set by the microcode to monitor the modem-in pattern for changes. A mask bit set to 1 means 'look for a change'.

Bit 14 Set by the microcode to start the receive operation only if the DCE is ready.

Bit 15 Set by the microcode to select the transmit line interface for modem-in change reporting. No modem-in change is reported on the receive line interface.

Start-Stop Transmit

Hw	Byte 0 (Even address)	Byte 1 (Odd address)
0	Set mode	Control
1	Spare	Spare
2	Modem—out immediate	Mask
3	Modem—out stacked	Spare

Set Mode

Same as receive. see page 4-165.

Control

Bit	Function
8	(Not used)
9	Modem-in change detected
10	First bit time
11	Underrun
12	(Not used)
13	Stop phase
14-15	Line state

Bit 9 Set by the hardware to memorize a modem-in change during data transmission, for reporting to the microcode via a level 2 interrupt.

Bit 9 is reset by the hardware after processing.

Bit 10 Set by the hardware when the first bit of a character is transmitted. It is reset by the hardware at the end of the bit time.

Bit 11 Set by the hardware to memorize an underrun condition (lack of characters from the CSP). Mark bits are transmitted over the line.

It is reset by the hardware when the underrun condition disappears.

Bit 13 Set by the hardware to indicate that stop bits are being sent. It is reset by the hardware.

Bits 14 and 15

Initialized by the microcode and updated by the hardware to indicate the line state in FES:

00 Inhibited
01 Diagnostic mode
10 DCE without data
11 DCE and data

Modem-In

Bit	Function
0	V.24: Data set ready V.25: Power indication X.21: (Not used)
1	V.24: Ready for sending V.25: Data line occupied X.21: Indication
2	V.24: Ring indicator V.25: Present next digit X.21: Controlled not ready state
3	V.24: Receive line signal detector V.25: Abandon call and retry X.21: Steady state detect
4	V.24: Test indicator V.25: Call origination status X.21: Clear to confirm by FESA

Bit	Function
5	V.24: Received data V.25: (Not used) X.21: Receive
6-7	Modem-in change detected

Bits 0 through 5
Modem-in status.

Bits 6 and 7
Set when a change is detected with respect to the mask pattern.

Other changes are no longer detected until the microcode has processed the new modem-in pattern and reset bits 6 and 7.

Mask

Bit	Function
8-13 14 15	Mask bits Start conditional No modem change report in receive

Bits 8 through 13
Set by the microcode to monitor the modem-in pattern for changes. A mask bit set to 1 means 'look for a change'.

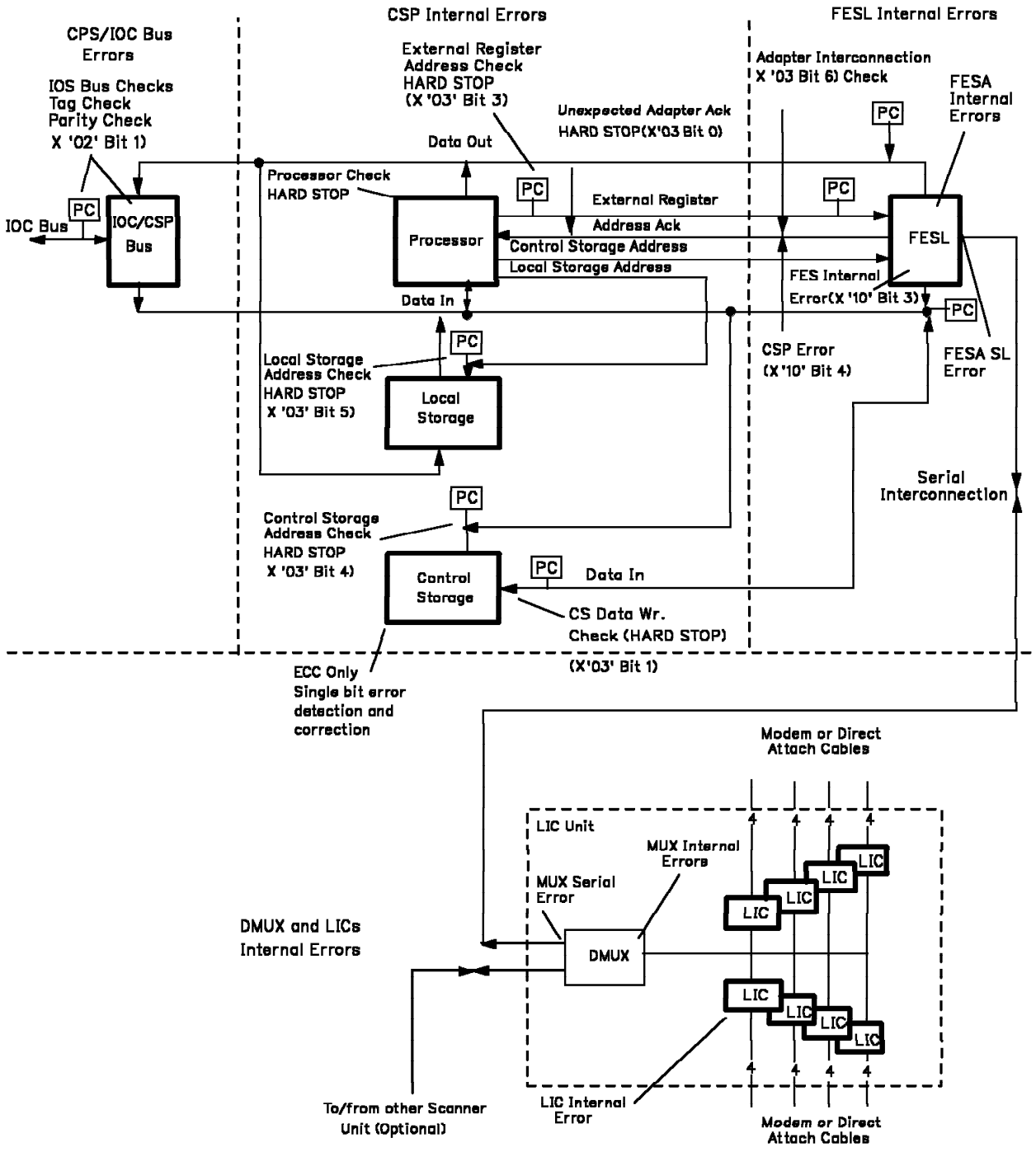
Bit 14 Set by the microcode to start the receive operation only if the modem is ready.

Bit 15 Set by the microcode to select the transmit line interface for modem-in change reporting. No modem-in change is reported on the receive line interface.

Error Detection

TSS Hardware Errors in Data Flow

This data flow summarizes the errors detected by the TSS hardware and their effect on the external registers. The errors marked 'hardstop' cause a scanner hardstop when they occur. The error information is gathered in two bytes.


CSP Internal Errors
FESL Internal Errors
CPS/IOC Bus Errors
IOS Bus Checks
Tag Check
Parity Check
X '02' Bit 1)
External Register Address Check HARD STOP (X '03' Bit 3)
Unexpected Adapter Ack HARD STOP(X'03 Bit 0)
Adapter Interconnection X '03 Bit 6) Check
FESA Internal Errors
Data Out
Processor Check HARD STOP
PC
IOC Bus
IOC/CSP Bus
Processor
External Register Address Ack
Control Storage Address
Local Storage Address
FESL
FES Internal Error(X '10' Bit 3)
Data In
Local Storage Address Check HARD STOP X '03' Bit 5)
Local Storage
CSP Error (X '10' Bit 4)
FESA SL Error
Serial Interconnection
Control Storage Address Check HARD STOP X '03' Bit 4)
Control Storage
Data In
CS Data Wr. Check (HARD STOP) (X'03' Bit 1)
ECC Only Single bit error detection and correction
Modem or Direct Attach Cables
LIC Unit
MUX Internal Errors
MUX Serial Error
LIC
DMUX and LICs Internal Errors
DMUX
To/from other Scanner Unit (Optional)
LIC Internal Error
Modem or Direct Attach Cables

TSS errors are classified as follows:

- CSP/IOC bus errors
- CSP internal errors
- CSP/FESL errors.

CSP/IOC Bus Errors

CSP/IOC bus errors are detected as follows:

By the CCU or IOC hardware:

- IOC bus check (invalid data) during PIO or AIO
- Time out during PIO or AIO
- Invalid CSCW during AIO
- Storage protection during AIO
- Address exception during AIO.

By the CSP hardware:

- IOC bus check: invalid data
- IOC bus check: invalid address.

By the scanner microcode:

- Invalid input PIO from NCP/EP
- Invalid input PIO from MOSS.

CSP Internal Errors

CSP internal errors are detected as follows:

By the CSP hardware:

- Unexpected adapter acknowledge
- Control storage data write check
- Processor check
- External register address check
- Control storage address check
- Local storage address check.

All the above errors cause a scanner hardstop.

By the scanner microcode:

- Invalid output PIO from the NCP/EP
- Invalid output PIO from the MOSS
- Invalid CSP interrupt level 0, 1, or 2 request
- Cycle steal stack overflow
- Interrupt level 2 stack overflow
- Invalid cycle steal length
- Command rejected
- Invalid IOH sequence
- Adapter interconnection check with unidentified line
- Microcode check.

Microcode Check

Internal microcode checkers are implemented in the TSS microcode, to ensure that it works properly.

When a checker is hit, the microcode builds a type 3 error status, bit 3 is set (microcode check).

The level 1 interrupt request to the CCU is raised.

The NCP issues a get error status command and, since bit 4 is ON, it issues the command 'get microcode check' (X'31').

The microcode responds with two bytes containing the identification of the checker and where it has been hit in the microcode.

With this information the NCP builds a BER 11 type 9D.

Second Byte	Checker Identification Format
01	Double enqueue
02	Fast get line ID not in use in CHHASCCU
03	Fast get line ID not in use in CHHA1NCP
04	Invalid cycle style length (not 16, 32 or 64)
05	Stack mismatch for trace (CHHASITS)
06	MOSS sends a PD18 command on Rcve interface
07	Branch to 0000 in block 7
08	Branch to 0000 in block 8
09	Branch to 0000 in block 9
0A	Branch to 0000 in block A
0B	Branch to 0000 in block B
0C	Branch to 0000 in block C
0D	Branch to 0000 in block D
0E	Branch to 0000 in block E
0F	Branch to 0000 in block F
10	ICB not found in trace table for stop trace
11	Interrupt level 2 while LA not assigned
12	Line in error while LA not assigned
13	No room or mismatch in LA table

Note: LA means logical address.

The scanner is set to disconnect mode in all cases.

CSP/FESL Errors

CSP/FESL errors are detected as follows:

By the CSP hardware:

- Adapter interconnection check with line identified.

By the scanner microcode:

- FESL failed to answer
- FESL error reporting path check.

By the FESL hardware:

- FES internal errors (see FESA Error Management below).
- FESA errors (see FESA Error Management below).

These two errors are reported to the CSP via register X'16' bit 1 without a CSP interrupt. The microcode tests register X'16' bit 1 at the end of each asynchronous operation.

The following errors are reported to the CSP on a line interface basis using a CSP interrupt level 2 via registers X'10' and X'12'.

- FES internal error
- FES/FESA error
- CSP/FESL error.

FESA Error Management

The FESA detects and reports to the CSP microcode (directly or through the FES) the errors occurring:

- At the FES-FESA interconnection
- In the FESA itself
- On the serial link
- In the MUXs
- In the LICs.

MUX, LIC, and serial link errors in the LIC unit, are reported to the FESA through the serial link.

Error Types

There are two types of error:

1. Unrecoverable errors, which may generate line drops or may disable the whole scanner.
   - Serial link solid failure
   - FES-FESA interface error
   - FESA internal error.
2. Recoverable errors, which do not significantly affect line management if the error rate is low enough:
   - LIC internal error
   - LIC overrun/underrun
   - LIC driver check
   - LIC clock failure
   - MUXs internal error
   - Serial link parity error
   - Serial link code violation error
   - Serial link sync error.

For instance:

- An error affecting the data transmission, will only need a message retry.
- Transient errors affecting the control information from FESA to/from MUXs/LICs have no effect (erroneous control slots are discarded).
- Correct control slots continuously refresh the MUX/LIC registers and the FESA inbound control RAM.

FESA Error Reporting

The FESA reports errors detected by the LICs, the MUXs, or the FESA itself in the following manners.

1. The FESA uses the LIC acknowledgement lead of the FES interface (no LIC acknowledgement means: error).
2. The FESA raises a level 2 interrupt to the CSP.

   The line address and the reason of the interrupt are available in the two FESA interrupt registers.

Note: Intermittent data bit failure may lead to intermittent error messages or messages lost (see “Intermittent Error Messages or Messages Lost” on page 4-205 for more details).

Process of LIC Errors

Checkers are implemented in the LIC to detect the following error types:

- Line interface clocks defaults
- Receive overrun and transmit underrun/overrun
- Outbound serial link parity error.

Errors detected by the LICs are stored in line error register bits 0 to 4 (inbound control RAM).

Line Error Register:

Bit	Meaning
0	LIC1s to LIC4s: receive clock failure LICs 5-6: DCE failure ('modem check')
1	LIC1s to LIC4s: transmit clock failure LICs 5-6: DCE clock failure
2	Receive data check
3	Transmit data check
4	LIC OSL parity check
5	LIC internal error
6	FESA ISL parity check

Clock failure

The LIC monitors the receive and transmit clocks of each line. Clock default is raised in the LIC when no transition has been detected on a given clock for 40 ms.

Clock failure is processed by the FESA only if the line is enabled.

Modem check

The FESA runs a level 2 interrupt to report the modem check to the CSP in case of:

- error during a self test
- error when reading the NVRAM
- unrecoverable error in normal mode.

Data check

The FESA raises a level 2 interrupt to report the data check to the CSP, only if the line is enabled.

Note: Intermittent data bit failure may lead to intermittent error messages or messages lost (see “Intermittent Error Messages or Messages Lost” on page 4-205 for more details).

LIC outbound serial link parity check

The reporting is done by an FESA level 2 interrupt to the CSP.

LIC internal error (or LIC not plugged)

The reporting is done by not sending a LIC acknowlege to the FES.

LIC inbound serial link parity check

The reporting is done by sending an FESA level 2 interrupt to the microcode, each time the error is detected by the FESA on an enabled line.

LIC driver check

The checking of the LIC drivers (at the DCE interface), by echo checking on the modem-out and the transmit data leads, is performed in the LIC, which sends to the FESA a driver check pattern for each line, every 4 ms.

In this pattern, 'all zeros' means: no error, a 'one' points out the defective driver.

- Bits 0 to 4 are assigned to the modem-out control lead drivers.
- Bit 5 is assigned to the transmit data bit driver (except in V.25: digit present echo).
- The FESA reports driver failures to the CSP microcode by means of level 2 interrupts for enabled lines.
- The driver check is reported only when modem-out remains unchanged for more than 4 ms.

DMUX/SMUX Errors

Errors detected by the MUXs are reported to the FESA on the serial link in the MUX status register.

MUX Status Register

Bit	Meaning
0	MUX present
1	OSL sync missing
2	OSL parity check
3	(Not used)
4	OSL code violation check
5	(Not used)
6	FESA ISL parity check

Errors are reported to the CSP by FESA level 2 interrupts for all enabled lines.

Process of FESA Errors

The FESA detects the following errors at the FES-FESA interface (FES interface errors):

- FES line/register parity error (FES synchronous or asynchronous read or write operation).
- FES control bus parity error (FES synchronous or asynchronous write operation).
- Data exchange check (reset service bit missing in FES synchronous operation)
- Other errors affecting the serial link or the FESA itself are stored in the FESA error register.

FESA Error Register

Bit	Meaning
0	FESA ISL sync missing
1	FESA ISL code violation check
2	FESA ISL counters check
3	FESA OSL counters check
4	FESA RAMs parity check

FES interface error

The FESA receives an incorrect command from the FES (synchronous or asynchronous operation), or does not receive the reset service bit from the FES.

The reporting is done by not sending a LIC acknowledge. No error bit is raised in the FESA.

FESA-ISL sync missing

Frame sync or super-frame sync is not received at the FESA ISL interface.

The FESA reports by issuing an FESA level 2 interrupt for all enabled lines (one interrupt per line).

FESA-ISL code violation check

A serial link code violation other than the frame sync is detected at the ISL interface.

FESA-ISL counters check

The error is stacked in the FESA error register until the FESA is reset. It forces 'no FESA acknowledge' on the FES interface for all lines (synchronous operation, and asynchronous operation except for read FESA error register).

FESA-OSL counters check

The FESA reports by issuing an FESA level 2 interrupt for all enabled lines (one interrupt per line).

The error forces 'no FESA acknowledge' on the FES interface each time the microcode tries to access a LIC/MUX/FESA register except for read error register).

FESA RAMs parity check

This error is stacked in the FESA error register. The error bit remains ON up to FESA reset.

The error bit forces 'no FESA acknowledge' on the FES interconnection for all lines (synchronous operation, and asynchronous operation except for read FESA error register).

DMUX/SMUX Error Detection and Reporting

Checkers are implemented in the DMUX and SMUX to detect the following errors:

- OSL synchronization error
- DMUX/SMUX internal error
- OSL parity error
- OSL violation code.

DMUX/SMUX Internal Error

The DMUX internal error detection is performed by a parity checker on the slot/line/frame counter which controls the odd parity of the sequence of counter output patterns.

Serial Link Error

Three outbound serial link checkers are housed in the DMUX:

- Serial link code violation checker
- Serial link parity checker
- Serial link synchronization error (frame sync missing and superframe sync missing).

DMUX/SMUX Error Reporting

All errors detected by any MUX, are loaded into its MUX error register for failure isolation.

For reporting operation to the FESA, the line/frame counter inbound decode activates the load of the serializer from the output MUX error register at the proper address.

The MUX error register is reset by the hardware when it is passed to the inbound serial link.

LIC Error Detection and Reporting

LIC Driver Check (Echo Check)

The driver check (echo check) is detected at LIC level, but the error reporting is controlled in the FES by the RAM C masks (refer to “Process of LIC Errors” on page 4-174 for more information).

Modem-Out Driver Check

The comparison is made between the modem-out echo and the modem-out control slots, 2.6 μs after the setting of the CCITT drivers.

Transmit Data Bit Driver Check (and Control for LIC 4)

A comparison between transmit bit echo and transmit data latch is made at middle of the data bit.

In X.21, the control (C) echo is checked like the transmit data bit echo.

Reporting Errors to the CCU

Errors on CCU I/O instructions are reported as follows:

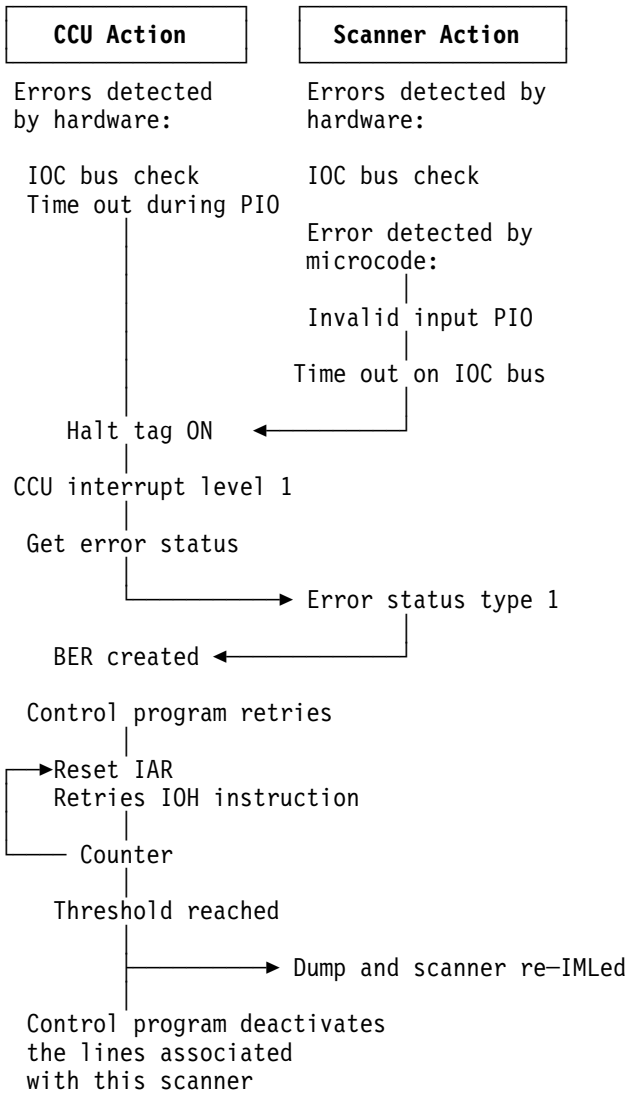
- Controller errors affecting only one specific line are identified by an error status in the response to the command, and are reported to the control program via a CCU interrupt level 2. The line affected may be disabled by the NCP or set to no-operating by the EP. The NCP under certain conditions, will retry an error reported to level 2.
- Errors affecting one scanner are identified in the error registers and are reported to the control program via a CCU interrupt level 1.

  When these errors affect all the lines connected to a scanner, the scanner is re-IMLed.

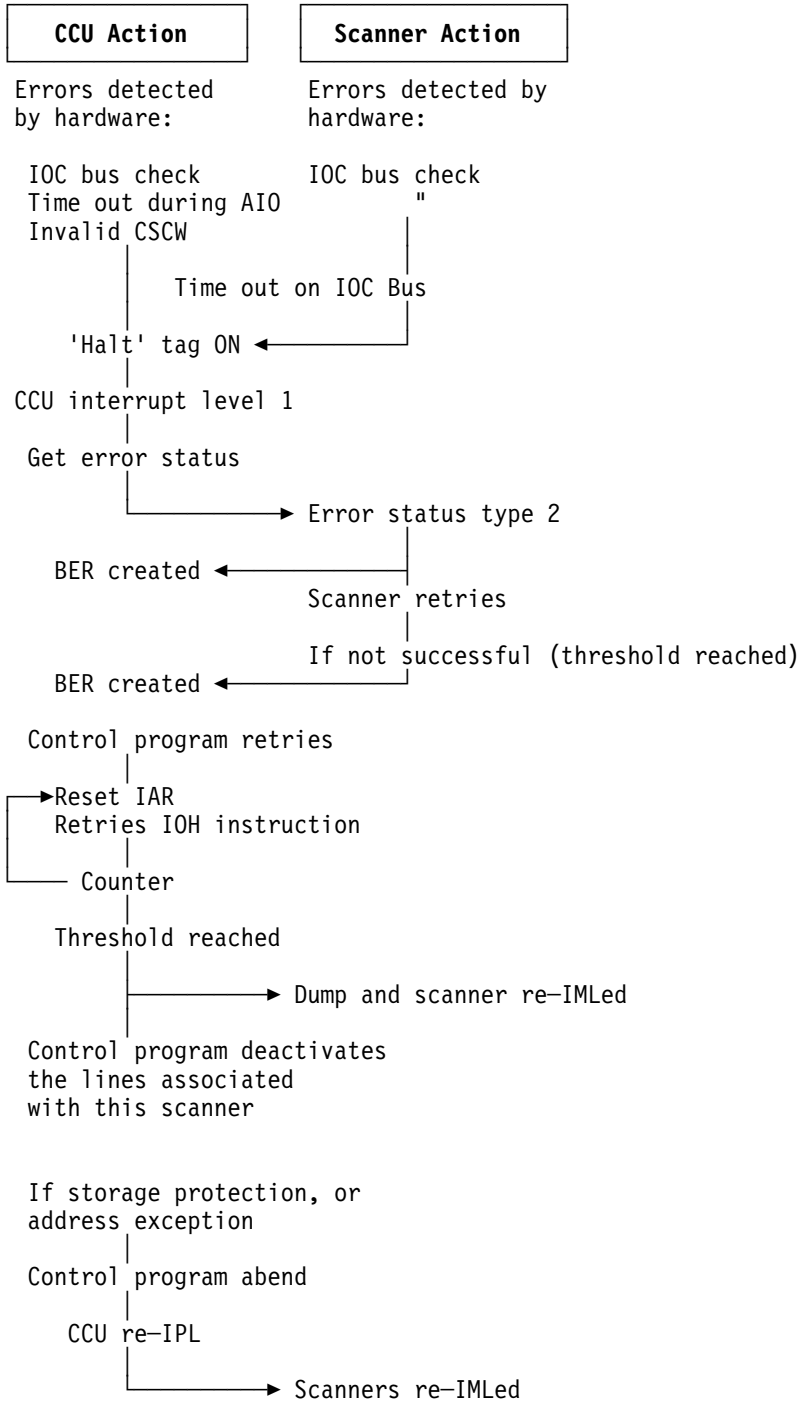
One BER is generated for each TSS error. The scanner must be in the connect mode.

CSP/IOC Bus Errors

Errors during PIO

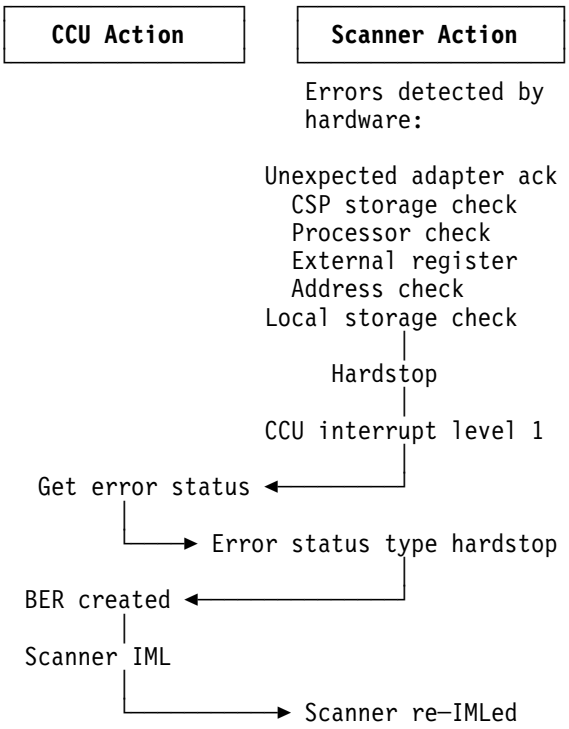


Errors during AIO

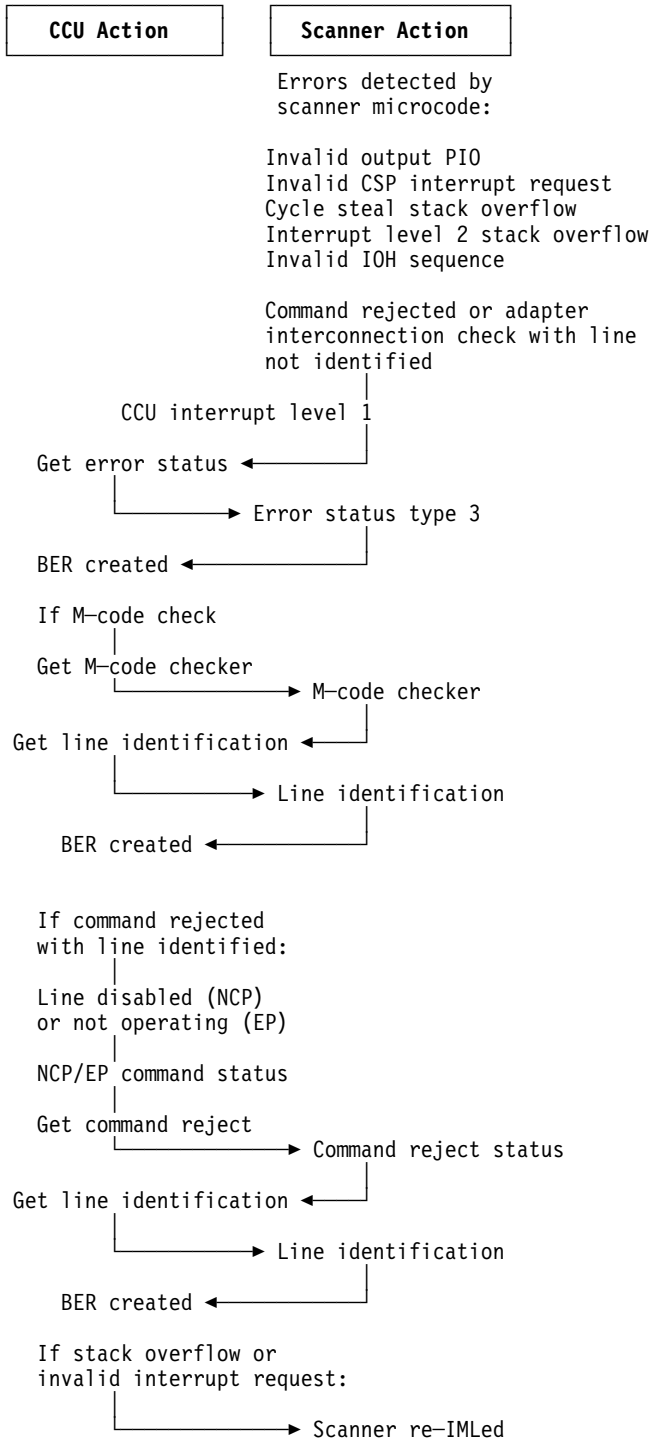


CSP Internal Errors

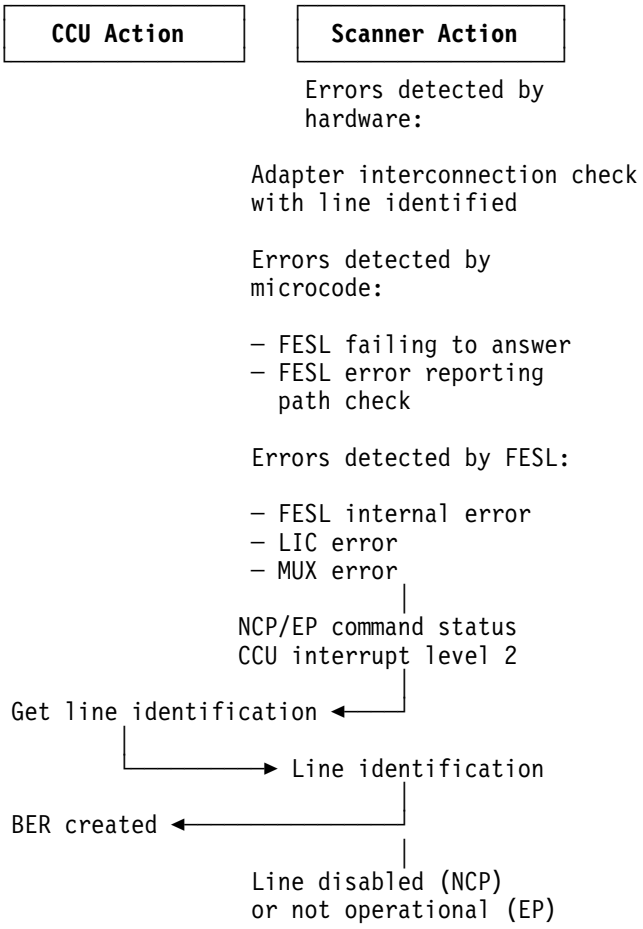
Detected by the Hardware



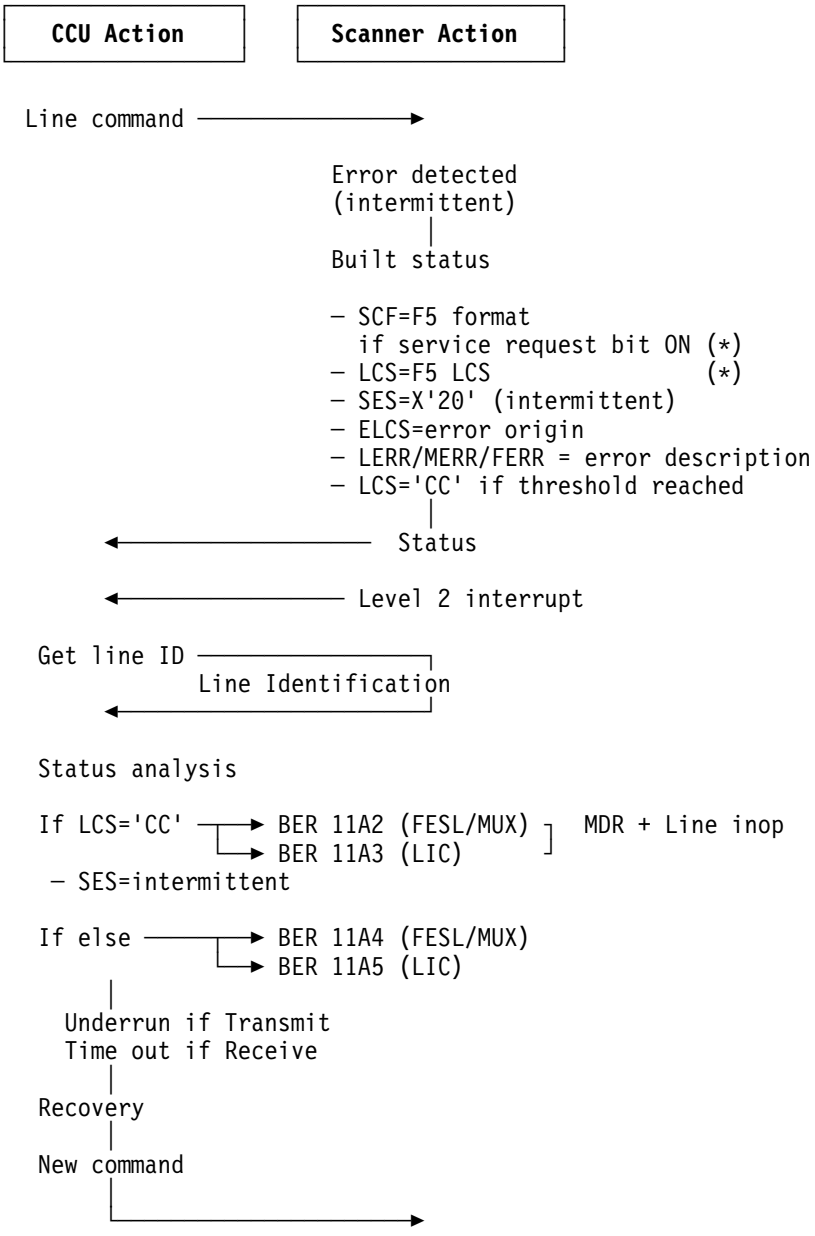
Detected by the Microcode



CSP/FESL Line Errors (Solid)

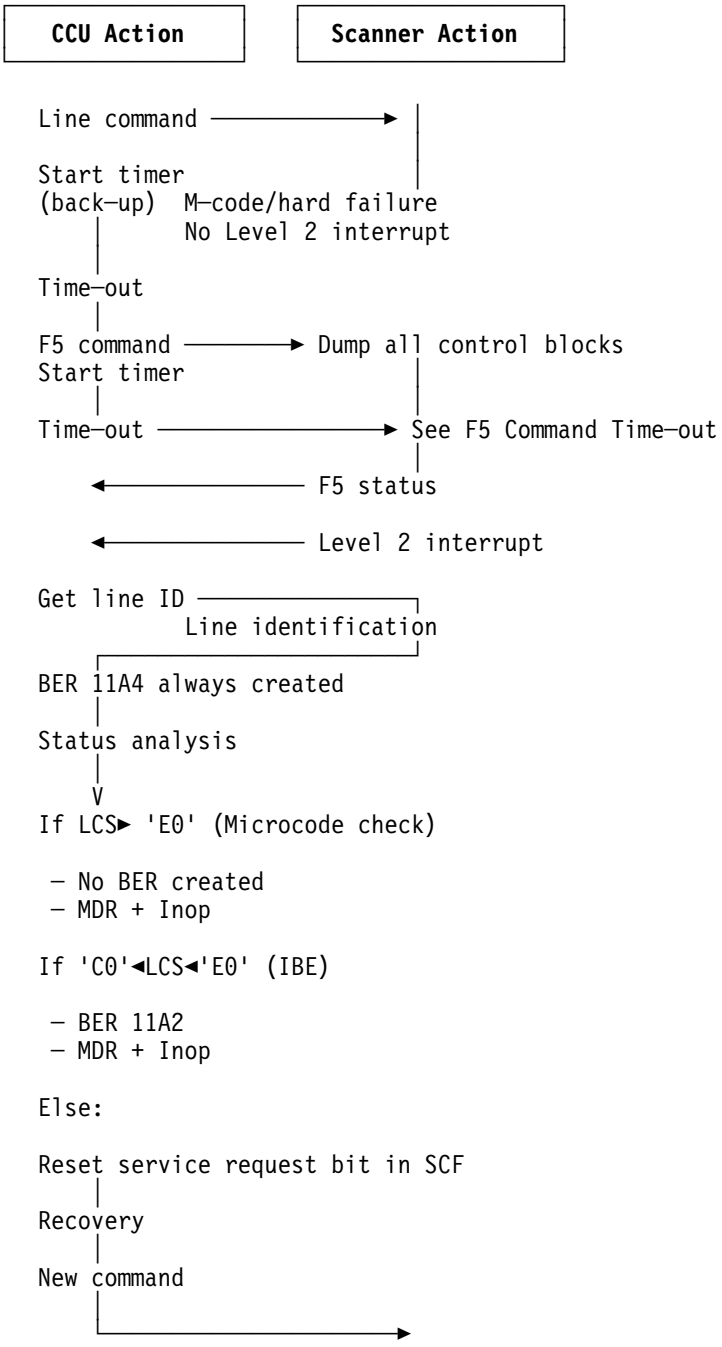


CSP/FESL Line Errors (Intermittent)



Note: (*) See F5 format

F5 Command Process



Reporting Errors to the MOSS

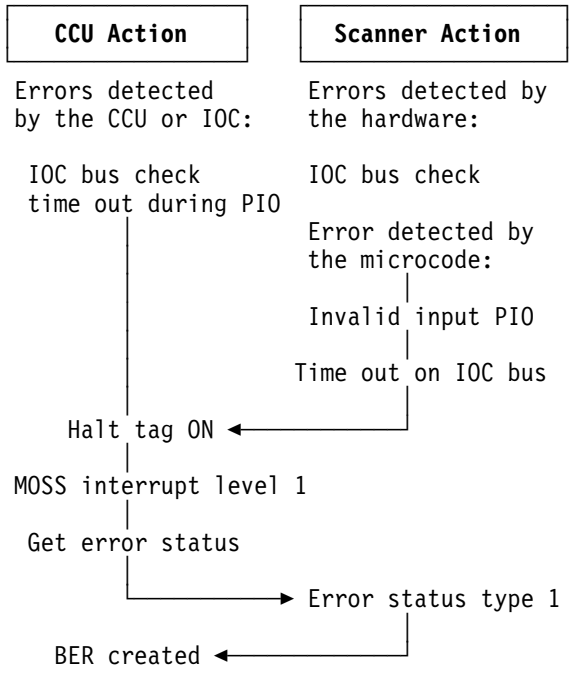
Errors on MOSS I/O instructions are reported as follows:

- Errors affecting only one specific line are identified by an error status in the response to the command, and are reported to the MOSS via a MOSS interrupt level 4.
- Errors affecting only one scanner are identified in error registers, and are reported to the MOSS via a MOSS interrupt level 1.

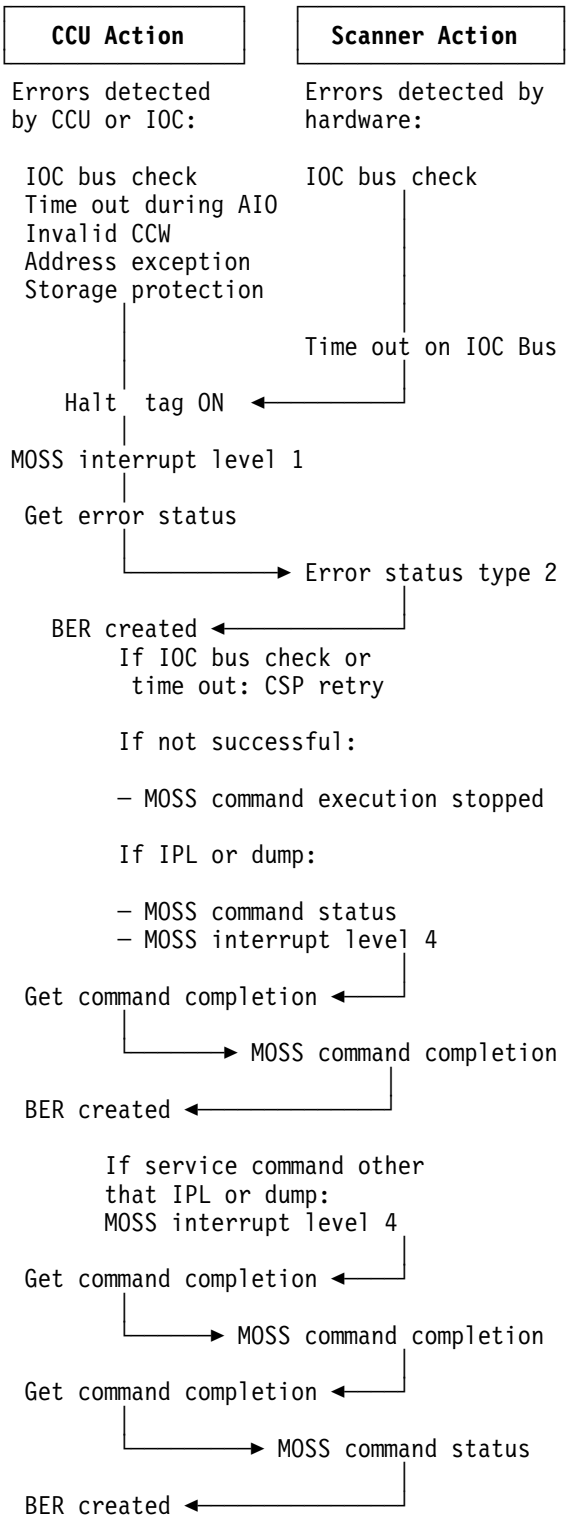
One BER is generated for each TSS error. The scanner may be in connect or in disconnect mode.

CSP/IOC Bus Errors

Errors during PIO

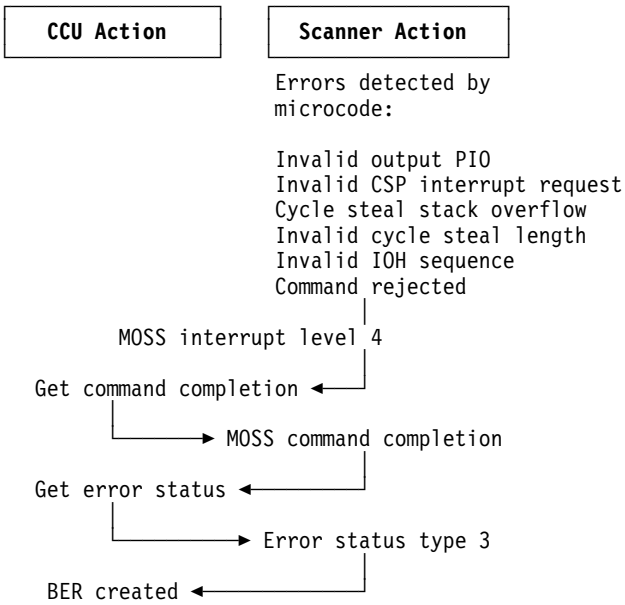


Errors during AIO

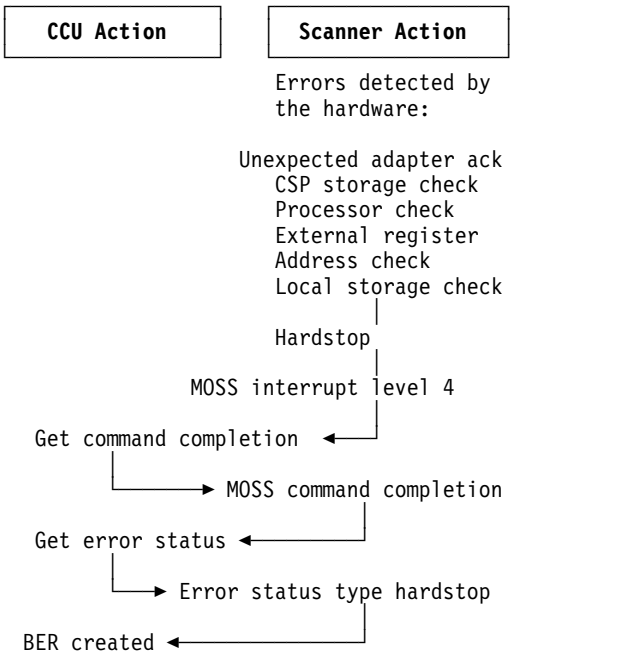


CSP Internal Errors

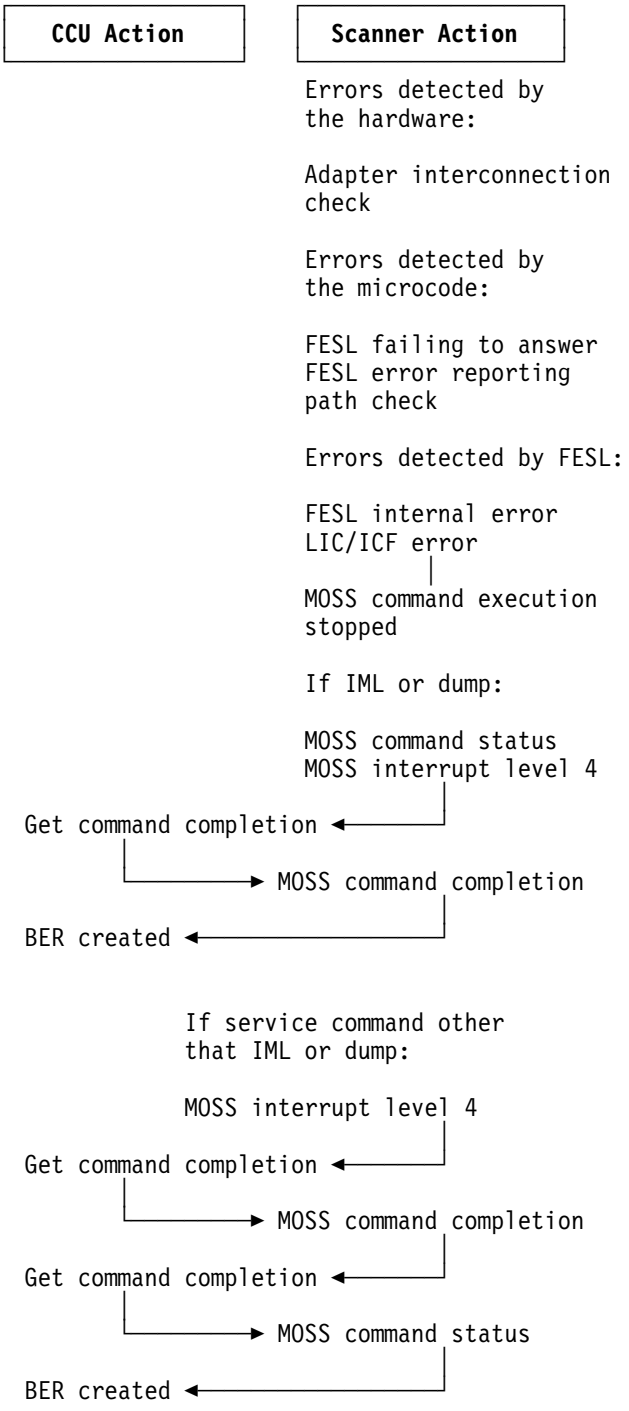
Detected by the Microcode



Detected by the Hardware



CSP/FESL Errors



Miscellaneous Status Fields

Three status fields, the status control field (SCF), the secondary status field (SES), and the line communication status field (LCS), have so many different meanings, dependant on the type of line control used, that they are grouped here for easy reference. **The differences between TSS and HPTSS are signalled as appropriate.**

Status Control Field (SCF) Bit Definition

The bits of the SCF byte describe the progress of the operation being executed.

Bit	Meaning
x	Halt/abort
. x	Service request
. . x	Scanner underrun/overrun
. . . x	Modem check
. . . . x . . .	Data stored
. . . . . x . .	End of message (EOM)
. . . . . x .	Data transmitted occured
. x	Receive sequence

Secondary Status Field (SES) Bit Definition

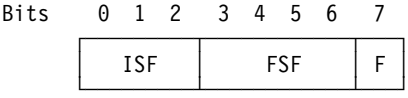
The bits of the SES byte identify errors encountered during the execution of the command.

When any bit is ON in this byte, the service request bit (bit 1) in the SCF must be OFF, except for 'modem retrain' in NCP BSC.

Bit	Meaning
x	Modem retrain
. x	Idle detection (SDLC) or format exception (NCP BSC, EP BSC)
. . x	LPDA reply received, but TI failed to come up /transient error
. . . x	Data check (SDLC, NCP BSC, EP BSC)
. . . . x . . .	Flag off boundary (SDLC) or bad PAD (NCP BSC)
. . . . . x . .	In phase (EP BSC)/TI ON (NCP BSC & SDLC)
. . . . . x .	DLE error (NCP BSC)
. x	Early flag (SDLC)/length check (NCP BSC)

Line Communication Status (LCS)

The bits of the LCS byte contain statuses applicable to the line being serviced. The byte is divided into three fields as shown below:



ISF = Initial status field
FSF = Final status field
F = Leading graphics / time out during X.21 clear

The indicator field (bit 7) specifies whether or not, leading graphics were the first characters received.

Initial Status Field (ISF) Bit Definition

The ISF (LCS bits 0 - 1) indicates essentially the type of line control that is used. The ISF is decoded as follow:

NCP BSC Receive Only: See paragraphe “Initial Status = B'0xx'” on page 4-193 for more explanation.

ISF	FSF	F	
0 1 2	**3 4 5 6**	**7**	**Meaning**
0 0 0	. . . .	.	Control mode, no text received (receive only)
0 0 1	. . . .	.	Text mode , STX is first character
0 1 0	. . . .	.	Transparent text mode, DLE STX are first char
0 1 1	. . . .	.	Header mode, SOH is first character

Special: See paragraphe “Initial Status = B'100' (Special)” on page 4-193 for more explanation.

ISF	FSF	F	
0 1 2	**3 4 5 6**	**7**	**Meaning**
1 0 0	. . . .	.	Special status

Errors: See paragraphe “Initial Status = B'110' (Internal Box Error)” on page 4-194 and paragraphe “Initial Status = B'111' (Hardware Error)” on page 4-196 for more explanation.

ISF	FSF	F	
0 1 2	**3 4 5 6**	**7**	**Meaning**
1 1 0	. . . .	.	Internal box error
1 1 1	. . . .	.	Hardware error

Final Status Field (FSF)

The FSF (LCS bits 3 - 6) gives further status information. The encoding is based upon the ISF configuration and is defined as follows:

Initial Status = B'0xx'

ISF	FSF	F	
0 1 2	3 4 5 6	7	Meaning
0 x x	0 0 0 0	x	Time out occured after reception has begun and ISF is not 000
0 x x	0 0 1 1	x	ENQ received
0 x x	0 1 0 0	x	EOT received
0 x x	0 1 0 1	x	DLE/xxx was received (xxx=any valid second character)
0 x x	0 1 1 0	x	Wrong ACK received
0 x x	0 1 1 1	x	NAK received
0 x x	1 0 0 1	x	ETX received
0 x x	1 0 1 0	x	ETB received
0 x x	1 1 0 1	x	RVI received
0 x x	1 1 1 0	x	Positive ACK (0 or 1) received
0 x x	1 1 1 1	x	WACK received

Initial Status = B'100' (Special)

ISF	FSF	F	
0 1 2	3 4 5 6	7	Meaning
1 0 0	0 0 0 0	x	Time out (nothing received); ACR, COS, DLO, or PND failed to drop; X.21 time out on ready for data
1 0 0	0 0 0 1	x	Ending condition on start/stop
1 0 0	0 0 1 0	x	X.21 time out during clear
1 0 0	0 0 1 1	x	386x/58xx test control active/X.21 time out on proceed to select
1 0 0	0 1 0 0	x	DLE-EOT disconnect sequence received
1 0 0	0 1 0 1	x	Lost data
1 0 0	0 1 1 0	x	Poll entry too long
1 0 0	1 1 0 0	x	EOT transmitted
1 0 0	1 1 0 1	x	X.21 call progress signal (CPS) error
1 0 0	1 1 1 0	x	Disconnected/X.21 DCE clear received
1 0 0	1 1 1 1	x	Connected

Notes:

1. When a special status occurs, the line is set to the disable state.
2. For X.21, if 'DTE clear' or 'DCE clear' confirmation is required, the 'X.21 time out during clear' flag (bit 7) is added to the final status to indicate the result of the clear operation. Bit 7 is set to zero if the clear was successful, and to one if it was not.

Initial Status = B'110' (Internal Box Error)

ISF	FSF	F	
0 1 2	3 4 5 6	7	Meaning
1 1 0	0 0 0 0	x	AIO error
1 1 0	0 0 0 1	x	Adapter check
1 1 0	0 0 1 0	x	Scanner interconnection error
1 1 0	0 0 1 1	x	Scanner failed to answer
1 1 0	0 1 0 0	x	Scanner internal error
1 1 0	0 1 0 1	x	Multiplex failure
1 1 0	0 1 1 0	x	Transient counter overflow
1 1 0	0 1 1 1	x	LIC / ICF error
1 1 0	1 0 0 0	x	No interrupt from scanner
1 1 0	1 0 0 1	x	Command rejected
1 1 0	1 0 1 0	x	Trace already active
1 1 0	1 0 1 1	x	Scanner error reporting path check
1 1 0	1 1 0 0	x	Invalid level 2 interrupt
1 1 0	1 1 0 1	x	Modem already in test mode
1 1 0	1 1 1 1	x	Line not accessible

Notes:

1. For NCP operations, the line is set to the disable state.
2. For NCP operations on duplex lines, the command on the failed interface is ended; the LCS indicates the cause of the error, and a level 2 interrupt is raised to the CCU. The command on the other interface is cleared; no ending status is set, and no interrupt is raised to the CCU.
3. For EP operations, the line is set to the NO-OP state.
4. After hardware error, the only commands accepted for that line is 'enable', 'monitor incoming call', or 'dial' (if autocall interface).

Initial Status = B'110' (Internal Box Error HSS)

The code is the value of the LCS bits 0 to 7 (fields ISF, FSF, F).

Code **Description**

C0 AIO error indicates a hardware error during an adapter-initiated operation (cycle-steal).

C2 Adapter interconnection check indicates a FESH hardware error.

C4 CSP interconnection error indicates a CSP/FESH interconnection hardware error.

C6 FESH failed to answer to a microprogram-initiated operation.

C8 FESH internal error indicates hardware error in the FESH detected by the FESH itself.

CE Local attach clock failure (F5 only).
This is returned as an F5 command status if the local attach clock has failed while in use.

D0 No interrupt from FESH indicates that the FESH has failed to respond to a microcode request.

D2 Command rejected indicates that the command issued by the control program has been rejected by the CSP.

D4 Trace already active indicates that the SIT is already running on this interface.

D8 Invalid FESH level 2 interrupt indicates that an unexpected CSP level 2 interrupt from the FESH has occurred.
DC ELCS is valid.
DE Line not accessible indicates that one of the two possible lines is already active and a set mode is received for the other line.

Extended Line Communication Status (ELCS) (Initial Status=B'110') for HSS

When the LCS = X'DC', additional statuses, as on internal box errors, may be found in byte 4 of the status area. These additional statuses are:

Code	Description
02 (a)	SCTL/DMA internal error
04 (e)	SCTL/DMA interconnection error
06	Combination of (f) and (g)
08 (3)	DMA time out on write
0A (1)	DMA interconnection error in write
10 (c)	SCTL/DMA storage protect/address exception
12 (b)	SCTL/DMA logical error
14 (f)	DMSW main bus parity check
16	Combination of (f) and (h)
18 (4)	DMA time out on read
1A (2)	DMA interconnection error on read
22 (d)	Storage unrecoverable error/SCTL internal error
24	Combination of (e) and (f)
28 (g)	DMSW parity check on primary/secondary bus
2A (5)	DMA bus driver fault
34	Combination of (e), (f) and (g)
3A (6)	DMA burst count error
44	Combination of (2), (e), (f) and (g)
4A (h)	DMSW driver fault
5A	Combination of (1), (e), (f), and (g)
6A	Combination of (2) and (g)
7A	Combination of (2) and (h)
9A	Combination of (5), (e), (f) and (g)
AA	Combination of (6) with any of (a) through (h)
BA	Combination of (1) through (6) with any of (a) through (h) which are not listed above.

Initial Status = B'111' (Hardware Error)

Detailed descriptions of hardware errors:

ISF	FSF	F	
0 1 2	3 4 5 6	7	Meaning
1 1 1	0 0 0 1	x	CTS dropped during command/modem retrain
1 1 1	0 0 1 1	x	RLSD failed to drop on disable command (not used by NCP)
1 1 1	0 1 1 1	x	DSR dropped during command/ external clock error (F5)
1 1 1	1 0 0 1	x	TI/CTS failed to come up
1 1 1	1 0 1 0	x	DSR failed to come up
1 1 1	1 0 1 1	x	No cable installed or wrong cable
1 1 1	1 1 0 0	x	TI/DSR and/or CTS failed to drop (on disable and transmit data commands on half-duplex lines without duplex facilities
1 1 1	1 1 0 1	x	X.21 disconnected DCE clear receive, with or without time out
1 1 1	1 1 1 0	x	Autocall check

Notes:

1. For NCP operations, the line is set to the disable state.
2. For NCP operations on duplex lines, the command on the failed interface is ended; the LCS indicates the cause of the error, and a level 2 interrupt is raised to the CCU. The command on the other interface is cleared; no ending status is set, and no interrupt is raised to the CCU.
3. For EP operations, the line is set to the NO-OP state.
4. After hardware error, the only commands accepted for that line is 'enable', 'monitor incoming call', or 'dial' (if autocall interface).

Initial Status = B'111' (Hardware Error HSS)

The code is the value of the LCS bits 0 to 7 (fields ISF, FSF, F).

Code Description

E2 CTS dropped indicates clear to send failed during transmission.

EE V.35 DSR dropped/X.21 DCE not ready, or external clock failure indicates that DSR failed for V.35 connection, or that the DCE is not ready for an X.21 connection in response to an F5 command.

F2 CTS failed to come up. Clear to send did not rise after request to send was set.

F4 DSR failed to come up. Data set ready did not rise after data terminal ready was set.

F6 No cable installed. There is no cable connected to the modem.

F8 DSR/CTS failed to drop on a disable. On a disable command, data set ready or clear to send did not drop.

FA X21 DCE not ready. An X.21 DCE not ready state was detected.

Note: In all cases of internal box errors and hardware errors, the line is disabled by the CSP. The command on the failed interface is ended (LCS contains the error and a level 2 interrupt request is raised to the CCU).

The command on the other interface is cleared without any ending status or level 2 interrupt request to the CCU.

After such an error the only commands that are accepted on the line are 'set mode' or 'enable'.

Error Status Description

To display the scanner external registers covered by error status type 1, refer to TSS functions (refer to the *3745 Service Functions*, SY33-2055).

Error Status Type 1 (Two Bytes)

Error status type 1 is built by the scanner microcode when a halt signal is received from the CCU via the IOC bus during a PIO operation.

The PIO may be issued from the CCU or from the MOSS.

Error status type 1 is reported on CCU or MOSS interrupt level 1 by the CCU or IOC hardware.

Byte 0

Bit	Function
0	Read/write (X'02' bit 0)
1	IOC bus check (X'02' bit 1)
2	(Not used)
3	I/O tag (X'02' bit 3)
4	Halt (X'02' bit 4)
5	TA tag (X'02' bit 5)
6	TD tag (X'02' bit 6)
7	(Not used)

Byte 1 (CCU)

Bit	Function
0	TA time select (X'00' bit 0)
1	(Not used)
2	(Not used)
3	(Not used)
4	(Not used)
5	(Not used)
6	(Not used)
7	Invalid input IOH

Byte 1 (MOSS)

Bit	Function
0	TA time select (X'00' bit 0)
1	(Not used)
2	Disconnect mode
3	(Not used)
4	(Not used)
5	(Not used)
6	Invalid input IOH type on IML cmd
7	Invalid input IOH type (not IML cmd)

Error Status Type 2 (Two Bytes)

Error status type 2 is built by the scanner microcode when a halt signal is received from the CCU via the IOC bus during an AIO operation.
The AIO may be issued from the control program or the MOSS.

Error status type 2 is reported on CCU or MOSS interrupt level 1 requested by the CCU or IOC hardware.

Byte 0

Bit	Function
0	Read/write (X'02' bit 0)
1	IOC bus check (X'02' bit 1)
2	Cycle steal grant (X'02' bit 2)
3	I/O tag (X'02' bit 3)
4	Halt (X'02' bit 4)
5	(Not used)
6	TD tag (X'02' bit 6)
7	(Not used)

Byte 1 (CCU)

Bit	Function
0	(Not used)
1	Cycle steal select (X'00' bit 1)
2	(Not used)
3-7	Line interface address bits 0-4

Byte 1 (MOSS)

Bit	Function
0	(Not used)
1	Cycle steal select (X'00' bit 1)
2	(Not used)
3	(Not used)
4-7	Last IOH TD byte 0 bits 0-3

Error Status Type 3 (Two Bytes)

Error status type 3 is built by the scanner microcode when an invalid output PIO, an invalid interrupt request, or an invalid IOH sequence is detected.

The output PIO may be issued from the control program or the MOSS.

Error status type 3 is reported on CCU interrupt level 1 or MOSS interrupt level 4 requested by the scanner microcode.

Byte 0

Bit	Function
0	Error status type 3 (always on)
1-3	Invalid interrupt levels 0-2
4	Microcode checker
5	Cycle steal/CCU level 2 overflow
6	Command 2 while command 1 in process
7	Disconnect mode

Bit 1 Set to indicate an invalid CSP interrupt level 0 or an unexpected branch to address '0000' at any level.

Bit 7 Set when the disconnect mode is entered via a service command.

Byte 1 (Invalid Output IOH)

Bit	Function
0	Trace or line command reject
1	Invalid output IOH type
2-7	See note (next table)

Bit 0-1 Description

0 1 Invalid output IOH

1 0 Line command reject

1 1 Trace command reject

Note: Description of bits 2-7.

Bits	Command Reject	Trace Cmd Reject	Invalid Output IOH
0	Command reject	Trace Cmd reject	Always OFF
1	Always OFF	Always ON	Invalid output IOH
2 3 4 6 7	Line interface address 0 to 3F	Slot number 0 to F	Line interface address 0 to 1F

Error Status Type 3 Hardstop (Two Bytes)

An error status type hardstop is returned by the CSP hardware when an error causing a hardstop has been detected.

It is reported on CCU interrupt level 1 or MOSS interrupt level 4 requested by the CSP hardware.

Byte 0

Bit	Function
0	Error status type hardstop (Always OFF)
1-4	Set to 0
5	Control store data check
6	Local storage/external register parity check
7	Internal check

Bits 5 through 7

Present only if byte 1 bit 2 is set ON (CSP processor check). All zeros in bits 5 through 7 identify a hardstop forced by the scanner microcode.

Byte 1

Bit	Function
0	Unexpected adapter check (X'03' bit 0)
1	CSP storage write data check (X'03' bit 1)
2	Processor check (X'03' bit 2)
3	External register address check (X'03' bit 3)
4	CSP storage address check (X'03' bit 4)
5	Local storage address check (X'03' bit 5)
6-7	(Not used)

MOSS Command Completion (Two Bytes)

The MOSS command completion is transferred to the MOSS to identify the scanner that requested the MOSS interrupt level 4.

Byte 0

Bit	Function
0-7	Current MOSS command

Byte 1

Bit	Function
0	Scanner request
1	Command failed (MOSS command status follows)
2	Error during status transfer (AIO error)
3	Error status type 3 available (get error status must be used)
4	Address compare hit on cycle steal operation
5	AC hit occurs
6	LIC not enabled
7	(Not used)

MOSS Command Status (Two Bytes)

If an error occurs during the processing of a MOSS service, the MOSS command status is transferred to the MOSS, in addition to the usual MOSS completion.

Byte 1 bit 1 of the MOSS command completion is set ON to indicate that the command failed, and that a MOSS command status is present.

Byte 0

Bit	Function
0-7	Current MOSS command

Bit	Function
0	AIO error
1	FESL failing to answer
2	DMUX error
3	FESL internal error (X'16' bit 5)
4	FESL error reporting path check (X'17' bit 4)
5	Adapter interface check (X'03' bit 6)
6-7	(Not used)

Bits 0 and 1: Set by the microcode.

Automatic Scanner-Dump and Re-IML

During normal operation, when one scanner goes down, the 3745 provides from the MOSS, the automatic re-IML of this scanner without MOSS operator intervention.

The automatic scanner re-IML function improves the possibility to have unattended operations executed from the MOSS.

When scanner re-IML is completed and successful, the MOSS sends an alert, notifying the network operator to reactivate the corresponding lines.

Description

This function is started whenever a TSS BER is sent by the NCP on detection of scanner failure conditions.

The BERs which trigger the automatic dump and scanner re-IML are:

Type 11 ID 1E, ID 91, ID 92, ID 93, ID 95, ID 97, ID 99, ID 9A and ID 9D.

Any general re-IPL of the CCU/scanners cancels the automatic scanner dump/re-IML processing.

If a dump has been started from the MOSS console by using the TSS services for a given scanner, the MOSS operator must **disconnect** this scanner to prevent the MOSS from receiving automatic scanner dump/re-IML for this scanner.

The priority is always given to CCU requests in order not to cause NCP hang situations, it means that all BERs requesting an automatic scanner dump/re-IML will be satisfied rather than MOSS operator requests.

However, the MOSS operator can always disconnect a scanner or put the MOSS in offline state.

If the threshold of 5 dump/re-IMLs is reached for this scanner within one hour, an alarm is sent to the MOSS console and no other action is performed on this scanner.

Every hour, MOSS level 1 will reset all counters attached to the scanners installed.

In normal processing, control is given successively to the dump function then to the IML function.

Dump Function

If the dump file on the disk is empty, the scanner microcode is dumped.

As the disk can contain only one dump per CCU, all subsequent scanner dumps are ignored. The dump area will become available after a dump transfer to the host.

The MOSS operator always has the possibility to delete the file by using the utility delete function.

If the dump area is not empty, the program starts the re-IML function.

Re-IML Function

Any severe errors during the processing will stop the re-IML function for this scanner.

A BER will be logged and an A11 alert will be sent to the host, using the same mechanism which sends alerts when scanner IML failures are detected during IPL CCU/scanners phase 3.

Once scanner loading is successfully completed, a connect status is sent to the NCP, and an alert is sent to the host to tell the network operator that he may re-activate the lines attached to this scanner.

At the end of the re-IML, the scanner is ready to process IOHs from the NCP. Thus, normal operations are restarted as soon as the first line for this scanner is re-activated.

Problem Determination Aids for LIC1s to LIC4s

In addition to the TSS diagnostics, several aids are available to help in problem determination on a line, or TSS:

- Line interface display (LID) function (refer to *Advanced Operations Guide*, SA33-0097).
- Wrap tests (WTT) function (refer to “Wrap Tests Controlled From the MOSS” on page 4-207 and *Advanced Operations Guide*, SA33-0097).
- Control program procedure (CPP) function (refer to *Advanced Operations Guide*, SA33-0097).
- TSS services (refer to *3745 Service Functions* manual, SY33-2055).
- Traces: external, internal SIT traces, checkpoint trace, NCP line trace (refer to chapter 13 *Traces and Dumps* in this manual for information).
- TSS dump (refer to chapter 13 in *Traces and Dumps* in this manual for information and to *3745 Service Functions*, SY33-2055).
- Port swap (refer to *Advanced Operations Guide*, SA33-0097).

Note: The internal SIT trace and TSS dumps can be transferred via RSF to be analyzed remotely by the PST CE.

Intermittent Error Messages or Messages Lost

Intermittent error messages or messages lost without alarm or BER created, may come from an intermittent hardware failure of the LIC card or of the FESL card (data bit failure).

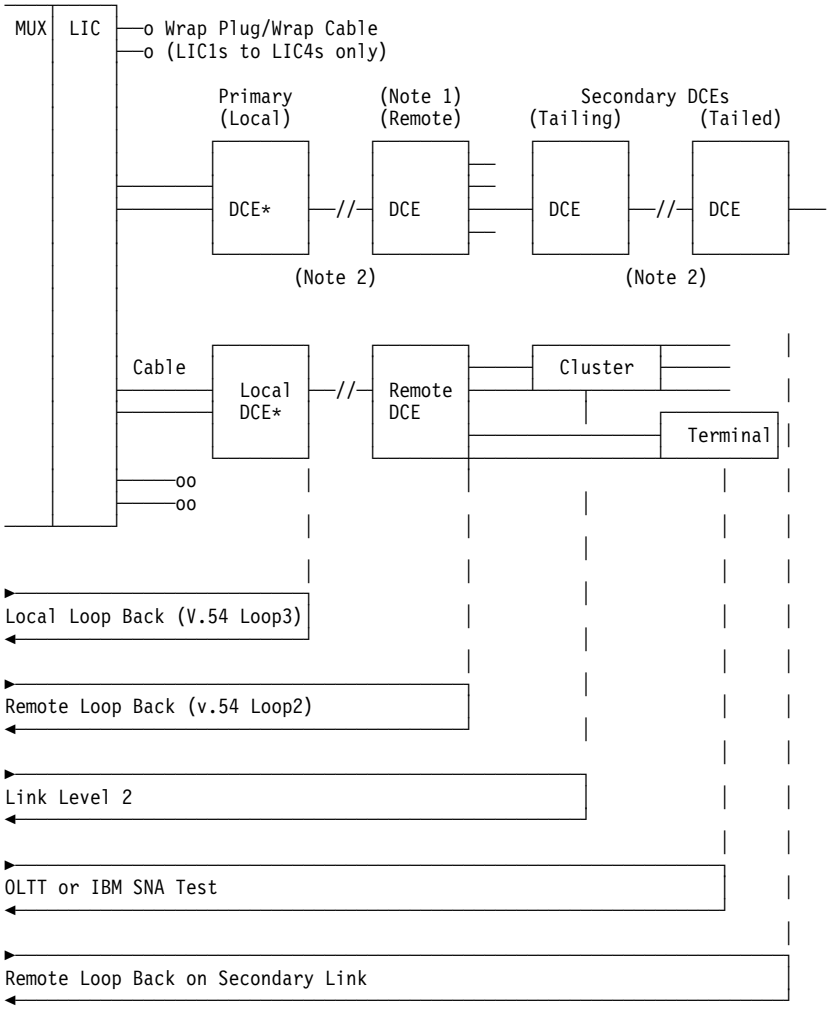
For that kind of symptom, run diagnostics to isolate the FRU:

- A LIC card hardware failure affects only the one to four lines of that LIC.
- An FESL card hardware failure, affects all lines attached.

Wrap Tests Controlled from the Host

Below are the different wrap test possibilities from the TSS to the terminal.

The wrap tests at DCE (or NTT) cable level are part of the line functions and are described in the *3745 Advanced Operations Guide*, SA33-0097.



* Standalone for LIC1s to LIC4s
Integrated for LIC5s and LIC6s.

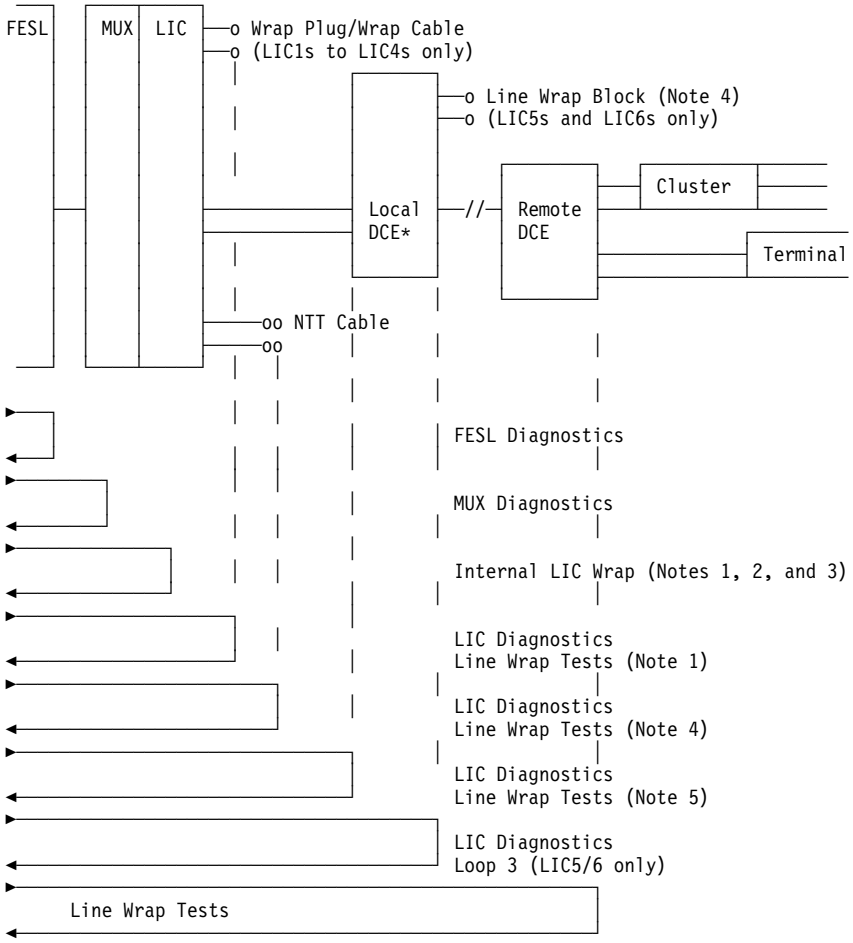
Notes:

1. The primary DCE is equipped with the data multiplexing feature or FIFO feature.
2. The telecommunication line is a 4-wire non-switched or switched line.

Wrap Tests Controlled From the MOSS

Below are the wrap tests controlled from the MOSS.

The wrap tests at DCE (or NTT) cable level are part of the line functions and are described in the *3745 Advanced Operations Guide*, SA33-0097.



* Standalone for LIC1s to LIC4s
Integrated for LIC5s and LIC6s.

Notes:

1. A line position can be plugged with a line cable, with a wrap plug (LIC type 1, 2, 4) or with a wrap cable (LIC type 3).

   When the TSS diagnostics are run, the hardware for a selected line is:

   a. Tested up to the LIC drivers.

   b. Fully tested if a wrap plug or a wrap cable is present on the selected line. Plugging a wrap plug or wrap cable selects the section 'RC'.

2. During LIC wrap mode operation, the transmit data line and the control lines are not deactivated at the DCE interface (the DCE may be power ON or OFF).
3. Although this is not a user-activated test, an 'echo-check' mechanism (inline) checks the transmitted data in wrap mode.
4. For manual intervention routines, refer to *3745 Diagnostic Description*.

5. If the cable is NTT with the connector switch set to 'operate', the test indicator (TI) signal is not forwarded to the connected DCE, so that the received pattern differs from the expected one.

Problem Determination Aids for LIC5s and LIC6s

Wrap Tests Controlled from the Host

To test the DTE part of LIC5s and LIC6s, these tests are the same as for LIC1s to LIC4s. See page 4-206.

Wrap Tests Controlled from the MOSS

To test the DTE part of LIC5s and LIC6s, these tests are the same as for LIC1s to LIC4s. See page 4-207.

In addtion, the following tests are available:

- Wrap test up to DCE output (with or without line wrap block)
- Self test (which occurs before the 'control lead wrap' command is executed)
- LIC line analysis procedures (LLAP).

See the *Advanced Operations Guide*, and the *Problem Determination Guide* for details.

Manual Tests Controlled from the PKD

To test the DCE part of the LIC5s and LIC6s, the following tests are all manually initiated from the PKD:

	Data Disruptive	LIC5	LIC6
• Local loop back	Yes[1]	*	*
• Remote loop back	Yes[1]	*	
• Local self-test	Yes[1]	*	*
• Local status	No	*	
• Remote self-test	Yes	*	
• Remote status	Yes	*	
• Digital test (xmit/receive test)	Yes[1]	*	*
• Analog test (line analysis)	Yes	*	

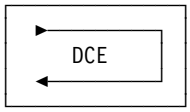
Notes:

1. The above tests run continuously until 'EXIT' is pressed. See the *Connection and Integration Guide* for details.
2. The process of the 'status bits' from the PKD is independent from the LPDA-2.

They are:

- Alarm tone received (remote DCE power loss)
- Alarm tone received (remote DCE failure)
- Carrier loss
- DCE re-initialization.

Local Loop Back (Loop-3)

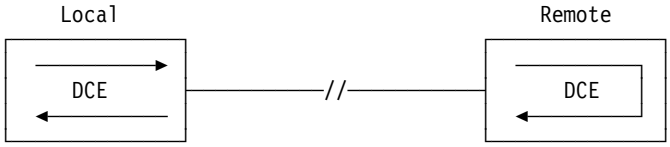


The DCE transmitter is wrapped to the DCE receiver, through the whole analog front end section, except the line driver and receiver.

The receiver is made compatible with the transmitter, that is, for a multipoint control DCE, the receiver is set to multipoint tributary.

This test is a CCITT loop-3 wrap. It is the host's responsibility to send data under RFS control, and check received data when CD is ON.

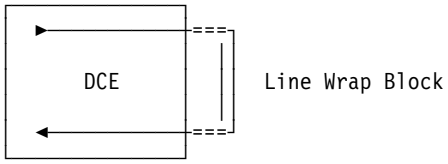
Remote Loop Back (Loop-2)



The DCE modem performs a digital loop, sending back the data it is receiving from the line. It is executed in CCITT mode only.

This test is a CCITT loop-2 wrap. It is the host's responsibility to send data under RFS control, and check received data when CD is ON.

Local Self-Test for LIC5



A line wrap block may be plugged into the line interface to allow line interface checking.

If the line wrap block is not plugged when 'local self-test' is selected from the PKD, a 'remote power loss' indication may appear at the remote DCE.

During the test execution, TI is raised at the local DTE interface, CD and RFS are dropped, and the data traffic through the DCE is interrupted.

DSR is dropped if DTR was OFF; otherwise DSR is kept ON.

During the test, the same sequence of operations is continuously repeated. The number of such cycles already performed since the beginning of the test is continuously displayed and incremented. Whenever an error is encountered, the test stops, the number of cycles is preserved, and an error code may be displayed by pressing the 'GO' key.

If during a self-test, the remote DCE sends an alarm tone, this tone is ignored by the DCE in self-test.

Local Self-Test for LIC6

This tests checks the following components/functions:

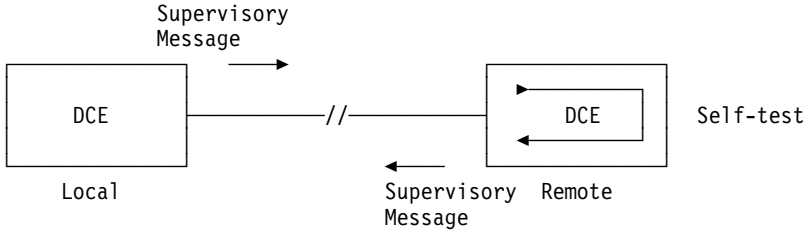
- Microprocessor
- ROS
- Internal and external RAM
- NVRAM (RAM part and configuration parameters)
- 'Read/write' registers
- DTE module
- Line loop circuitry
- SDLC adapter
- Alarm signal (transcode test)
- CSU (stress test).

This test is automatically performed at each power ON. In this case, a checking of the CMOS modules LSSD string hardware is added.

If an error is found during the tests of the configuration parameters in the NVRAM (checksum error which could be due to a virgin area), then:

1. A default configuration is transferred from the RAM to the NVRAM.
2. The indication is recorded for a future LPDA-2 report if applicable.
3. The LIC6 is put in idle mode.
4. A warning is displayed.

Remote Self-Test



A supervisory message is sent from the local DCE to the remote DCE (along with the DCE address).

On reception of this message, the addressed DCE starts a self-test (less than 5 s) and sends back the result of the test in a supervisory message.

During the test execution, 'WAIT' is displayed on the local and the remote DCEs, TI is raised, RFS and CD dropped at the local and remote DTE interfaces, and the DATA traffic through the DCEs is interrupted.

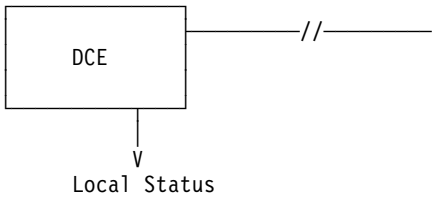
DSR drops at the local DCE, if DTR is OFF.

At the end, a report is displayed on the local DCE and normal background information is displayed on the remote DCE.

If the request causes the remote DCE to fail, the alarm tone is sent, and a report is displayed.

If a non-productive time out occurs after the request, a report is displayed.

Local Status



When initiated on the local DCE, the following information is displayed:

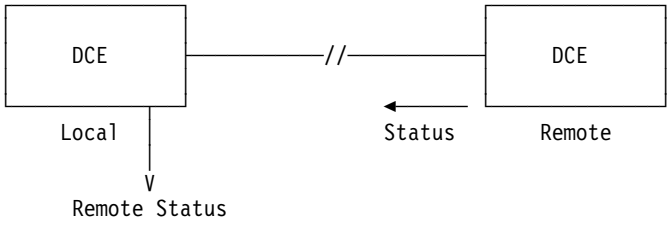
- Local line status (current quality, number of hits within the last 15 minutes, warnings logged, current receive level)
- Local DTE interface status and activity.

DATA traffic through the DCE is not interrupted. Normal operation takes place at the DTE interface and TI is NOT raised.

Then this test displays line quality and received level, until the 'STOP' key is pressed, or a 30 s time out is reached.

Any LPDA-2 command issued to the DCE from the DTE is ignored (TI is kept OFF).

Remote Status



When initiated on the local DCE, along with the remote DCE address, the following information is received (within 5 s maximum) and displayed at the local DCE in the following sequence:

- Remote line status (current quality, number of hits within the last 15 minutes, warnings logged, current receive level).
- Remote DTE interface state and transition since the last request.

During execution, TI is raised, RFS and CD dropped at the local and remote DTE interfaces, and the data traffic through the DCE is interrupted.

At local and remote DCE, DSR drops if DTR is OFF; otherwise, DSR is kept ON.

Digital Test (Xmit/Rcve) for LIC5

A loop test with a tributary station is performed in chopped carrier mode and half-duplex protocol. This protocol allows different inbound and outbound speeds in the control DCE of a multipoint network.

For each test, 16 blocks (256 bytes each) are transmitted in each direction. The blocks missed or in error are counted as erroneous.

In point-to-point, the test is run in continuous carrier operation.

During test execution, TI is raised, RFS and CD dropped at the local and remote DTE interfaces, and the data traffic through the DCE is interrupted.

DSR drops at the remote DCE, if DTR is OFF.

This test loops on local and remote error counters, until the 'STOP' key is pressed.

Digital Test (Xmit/Rcve) for LIC6

This test, which is not protocol-transparent, can be selected only if LPDA-2 is enabled. During this test, local and remote DSU/CSUs exchange predefined bit patterns.

Analog Line Analysis Test

Causes the DCE, after about 10 s, to display some parameters of a telecommunication line between two DCEs (defined as local 'L' and remote 'R').

At test initialization some parameters are already available, because they are derived from data signal and continuously carried out during normal transmission, these values are inserted into line analysis report.

The other parameters are measured during the test itself:

- Data-driven parameters:
  - Received level: 'RL'
  - Minimum received level (last 15 minutes): 'MRL'
  - Number of impulse hits (last 15 minutes): 'HIT'
  - Number of line breaks (last 15 minutes): 'LBK'

    Larger than 10 dB below average value, for a duration longer than 10 ms (typical values).
- Impairments measured during the test:
  - Line round trip delay, 'RTD'

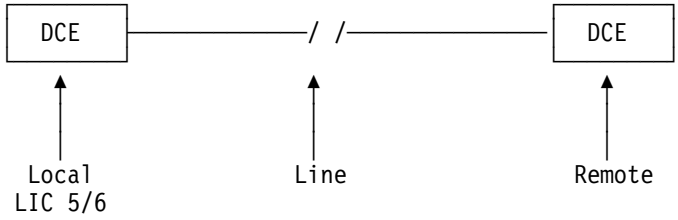
    Measured at the local side, it is the difference between command sending and acknowledgment receiving times. The measure does not include the DCEs passthrough delay.
  - Non-linear distortion 'H2' and 'H3'
  - Signal-to-noise ratio 'S/N'

    Measured from a 1004 Hz tone, into voiceband.
  - Phase jitter 'PJ'

    Phase modulation imposed by the channel to a 1004 Hz tone. Peak-to-peak phase jitter is measured in a 300 Hz bandwidth.
  - Frequency shift 'FS'.

LIC Line Analysis Procedures (LLAP)

The LLAP is a set of tests initiated manually from the PKD and which are automatically chained. They are intended to test a communication facility: the line itself and the two DCEs.



The following areas are successively tested :

- Local self-test
- Local self-test with telephone wrap plup
- Remote self-test
- Local/remote configuration compatibility
- Received and transmitted data activity on both DCEs
- Received line signal quality.

Note: Devices beyond the remote DCE (such as tailed DCEs and lines) are not tested.

Detailed LLAP procedures are described in the *Problem Determination Guide*.

Chapter 5. The Token-Ring Subsystem

The TRSS in 3745 Data Flow

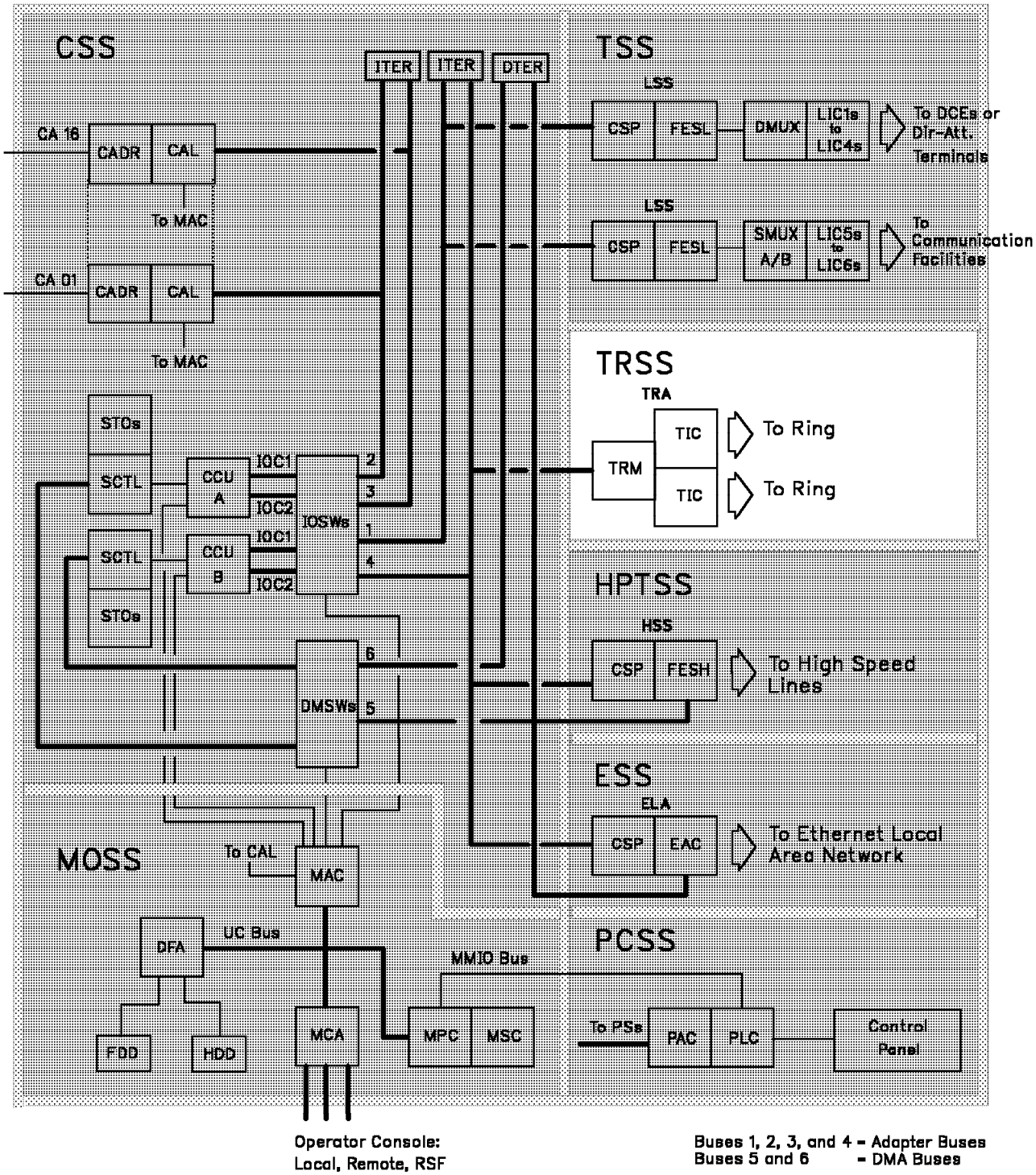


Figure 5-1. TRSS in 3745 Data Flow. For models 21A-61A, DMA and IOC buses are connected to the CBC in the 3746-900. The MCA card is replaced by the MLA card which interfaces to the MPC card through the MMIO bus. This MLA card links the MOSS to the Service Processor through a LAN.

Token-Ring Network

The token-ring networks are designed specifically to provide an integrated approach to communications in a particular location.

In case of large companies with multiple, widely separated sites, individual token-ring networks will almost always be interconnected.

In a token-ring network the data rate is much higher than is possible using common carrier communications.

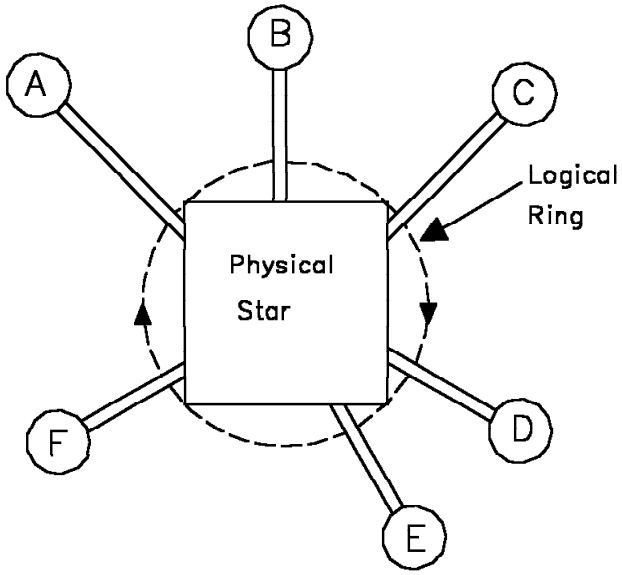
A token-ring network can replace switched and non-switched telephone lines and also allow voice communications over the same cabling system that carries data communications.

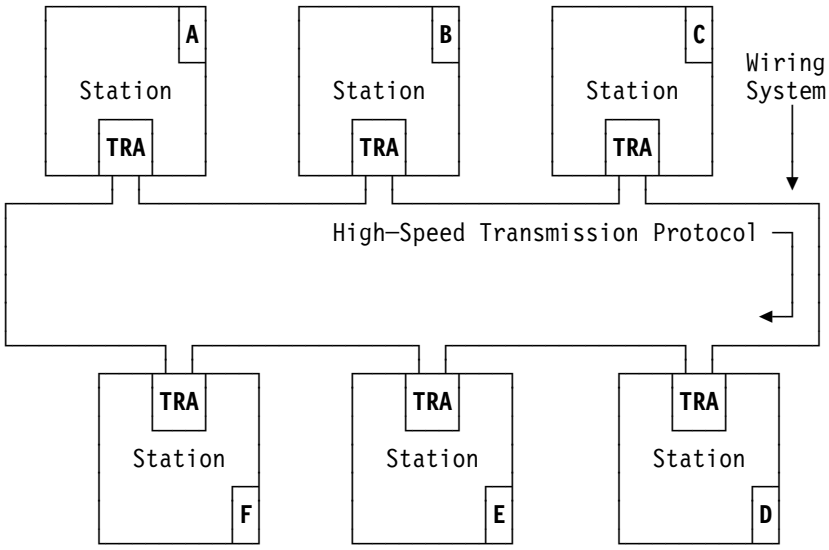
The token-ring network complies with the recommendation 802.5 of IEEE and the ISO 8802/5.

IBM Token-Ring Network

It is an information transport system that provides high-speed
(4 Mbps or 16 Mbps) connection between users within a single building complex through the implementation of a common:

- Cabling system
- Communication adapter
- Access protocol.





Legend: TRA : Token—Ring Adapter
Station : Can be controller, display/keyboard terminal, node...

Figure 5-2. Token-Ring Network Configuration Example

Cabling System (Ring)

Several transmission media may be used together:

- IBM Cabling System (twisted-pair of copper wire)
- Telephone communication facilities
- Optical fiber.

Token-Ring Adapter

The adapter in the 3745 has the following functions:

- Frame and address recognition
- Token generation
- Error checking and logging
- Buffering (transmit and receive)
- Time out controls
- Connect the product to the token-ring network.

For Example

The 3745 is connected to the IBM Token-Ring network through the token-ring interface coupler card (TIC). A cable composed of two pairs of copper wires (transmit and receive pairs), connects the controller to the Multistation Access Unit (MSAU) through a wall connector.

The cable running from the controller or a station to the MSAU, is called a lobe.

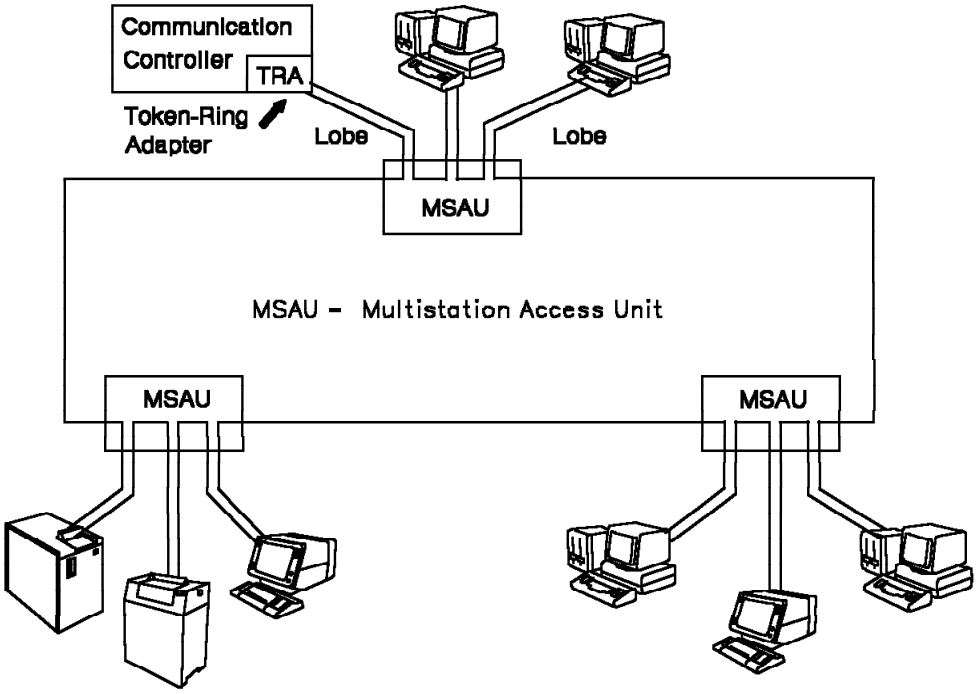


Figure 5-3. Example of Lobes

Multistation Access Unit

The multistation access unit (MSAU) provides insertion service to the main ring for its attached lobes. Nodes or stations are attached to the lobes.

The multistation access units that include electronic or electro-mechanical switching elements, are shown below:

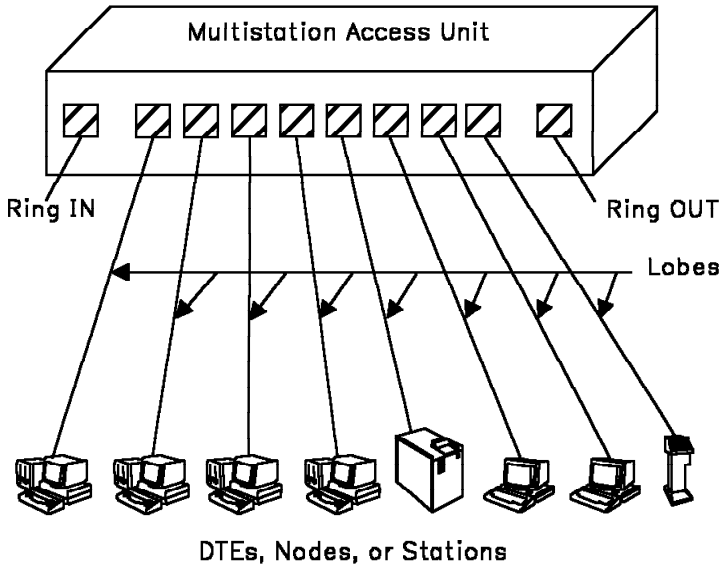


Figure 5-4. Multistation Access Unit

Access Protocol

A token is a short message. It travels around a communication ring that allows attaching different systems to the communications facilities provided by that ring. When a token is used for transmission by an attachment, it is known as a frame.

Actually, a token is a very short frame (3 bytes) that has no addressing, message, or error-checking capabilities. Those are added when the token becomes a true frame.

General Frame Format

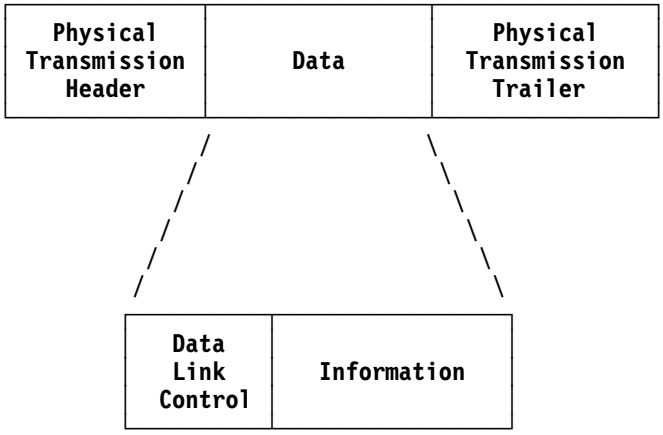


Figure 5-5. Frame Format

Once a station is physically attached to a ring, it first synchronizes itself to the data patterns passing through it over the ring.

Token-Ring Access Control Protocol

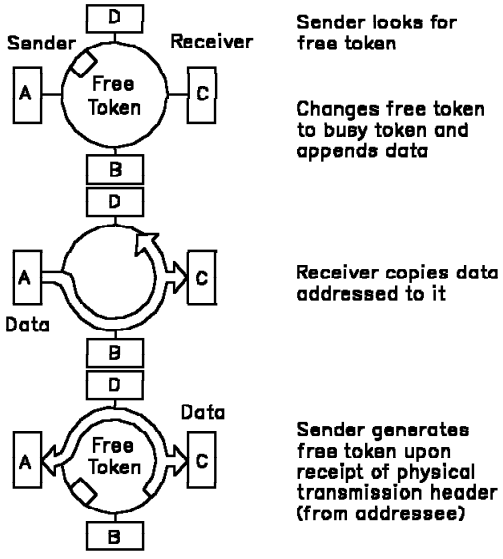


Figure 5-6. Token-Ring Access Protocol Example

Token-Ring Encoding

The differential Manchester protocol is used as means to transmit information around the ring, to all devices connected to that ring and power-on.

Major System Components

Nodes

A node may be one of the following machines:

- Communication controller
- Intelligent workstation
- Keyboard/display terminal
- Printer
- Terminal control unit
- Processor
- Facsimile device
- Personal computer
- Protocol converter.

Interface Couplers

Each node has its own Token-Ring interface coupler card to gain access to the Token-Ring network or ring.

The 3745 has up to eight Token-Ring interface coupler (TIC) cards.

Bridges

A bridge is a high-speed switching device that allows linking multiple rings and maintaining a physical ring separation.

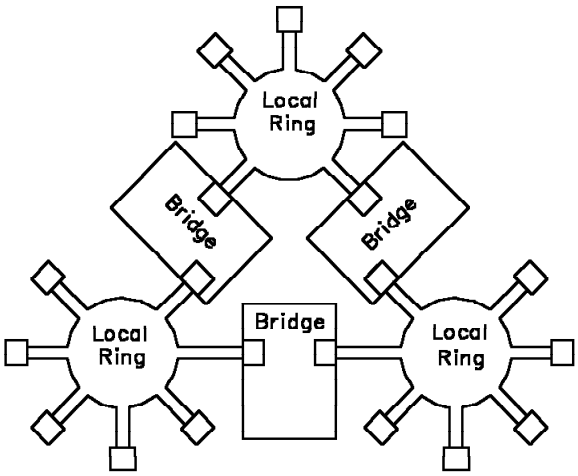


Figure 5-7. Ring-to-Ring via Bridge Example 1

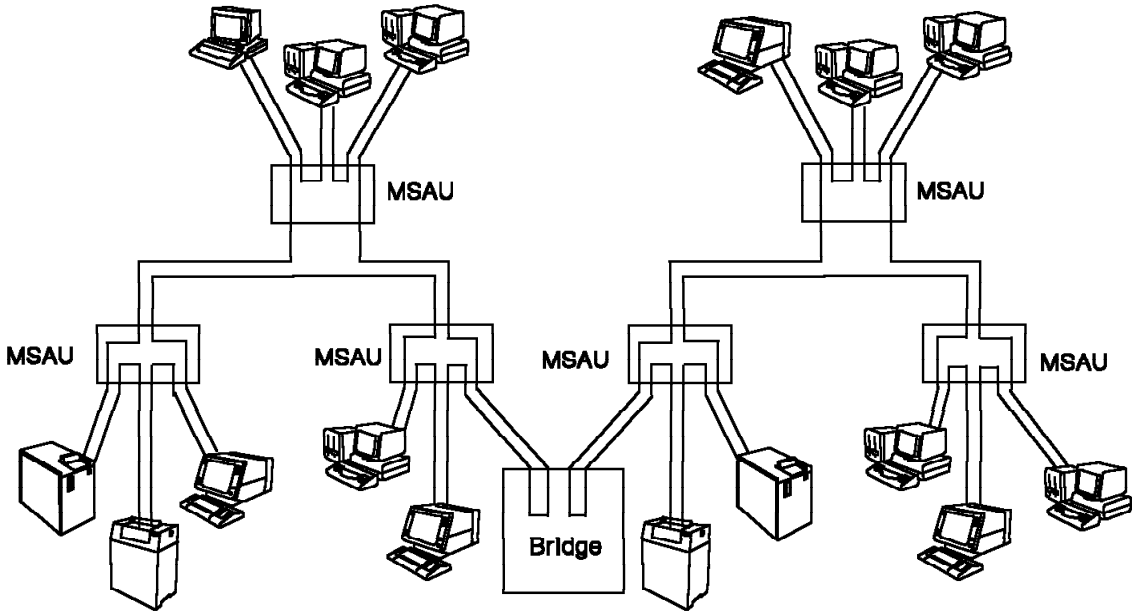


Figure 5-8. Ring-to-Ring via Bridge Example 2

Typical Multi-Floor Wiring

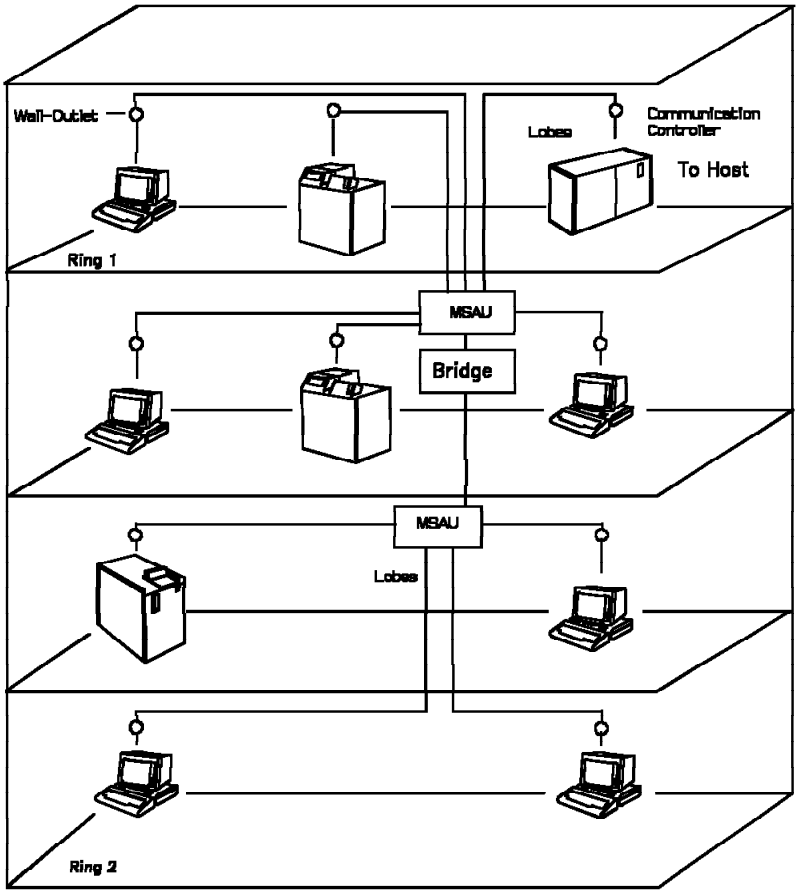


Figure 5-9. Multi-Floor Wiring Example

The Token-Ring Adapter in the 3745

Introduction

The token-ring subsystem (TRSS) allows connection to an IBM Token-Ring network which uses the token-ring protocol. The TRSS in a communication controller is controlled by the NCP token-ring interconnection function.

The hardware is based on a processor-driven card named token-ring interface coupler card (TIC) and the token-ring multiplexer card (TRM). There are two types of TIC: TIC1 and TIC2. TIC1 runs at ring-speed of 4 Mbps only. TIC2 runs at ring-speed of 4 Mbps or 16 Mbps (the speed is set through software).

The combination of a TRM and the associated TICs (up to two) is called a token-ring adapter (TRA). The TICs installed with a TRM must both be either TIC1s or TIC2s. **A mixture of TIC types with the same TRM is not allowed.**

The combination of all the TRAs in a controller is called the TRSS.

One token-ring network can be accessed by each TIC card.

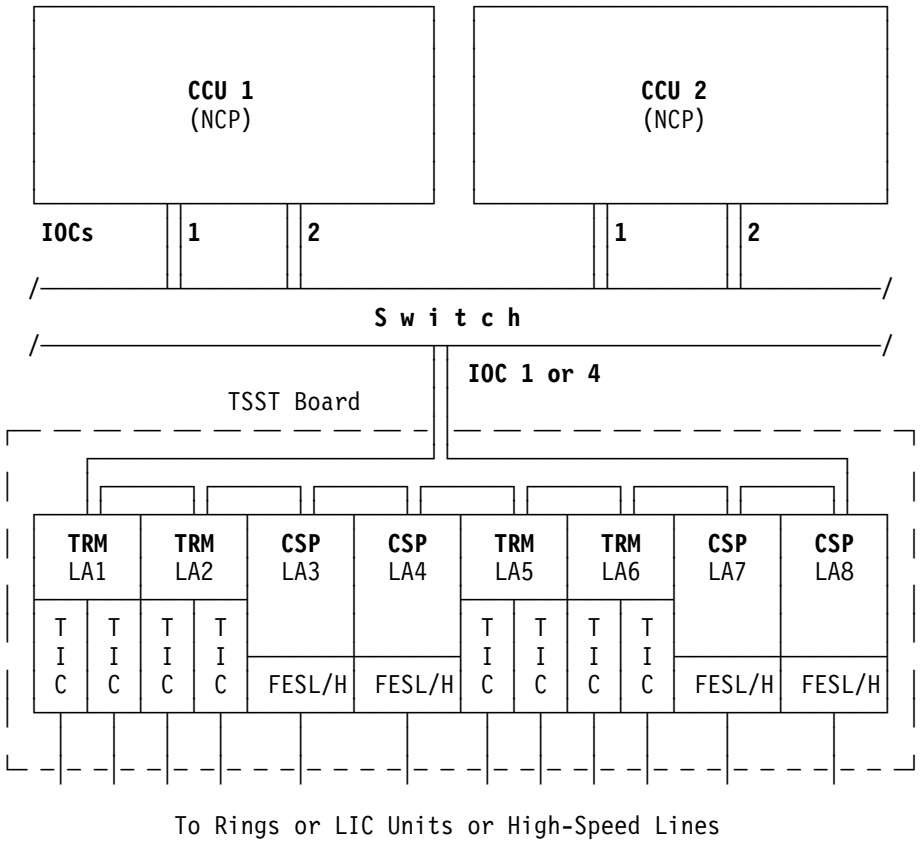


Figure 5-10. TSST Board Data Flow

Packaging

Up to four TRAs and up to four low-/high-speed scanners may be installed on the TSST board on the base frame only. The TRM interconnects with the input/output control bus (IOC bus) and it is accessed from the CCU with a unique address as for the scanner. The TIC cards are connected to the TRM by a bidirectional bus called the TIC bus.

For board and card locations, see Chapter 5 of the *Maintenance Information Procedures* manual, SY33-2054.

Token-Ring Interface Coupler (TIC) Card

The TIC card has a low profile connector for connection to the ring.

The card consists of four high-level functional areas.

- The front end that interfaces to the ring
- The protocol handler
- The message processor
- The TIC bus interconnection control.

TIC Data Flow

The TIC can perform the following operations on the data stream that passes through it on the ring:

1. Repeat the received data without copying it.
2. Repeat and copy the received data.
3. Change the state of single bits in the received data before retransmitting it.
4. Originate the transmission of data.
5. Remove from the ring messages that it has previously transmitted.

The next figure shows the relationship between the message processor and the other functional areas of the TIC card.

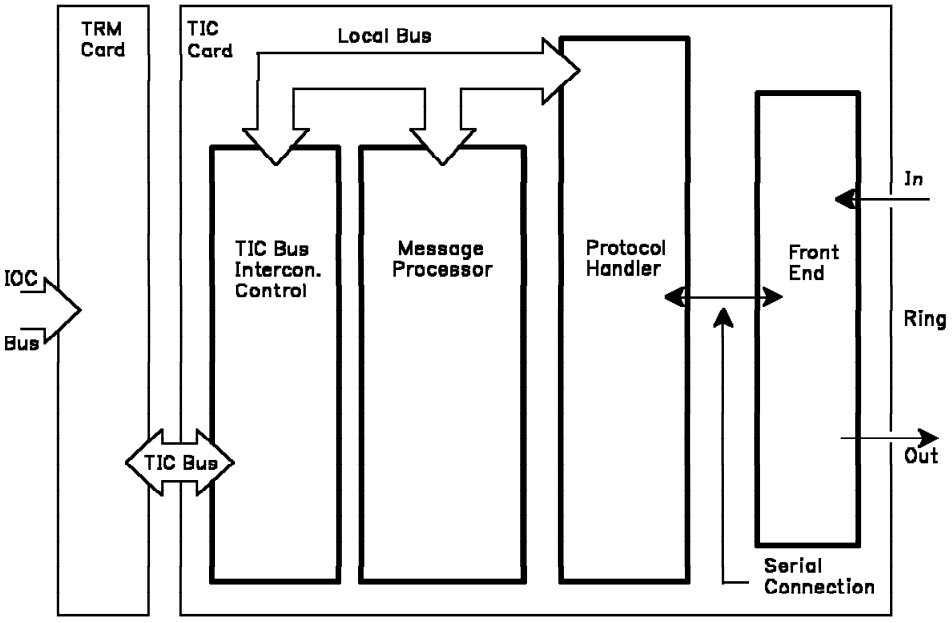


Figure 5-11. TIC Card Data Flow

The Front End

The front end is the direct interface with the transmission line of the ring.

The front end transmits and recovers Manchester-encoded data (including certain 'violation' sequences) as it passes around the ring.

The front end synchronizes itself with the received data stream and develops a clock which is boundary-aligned to the bit stream. The bit stream, along with the derived clock, is passed to the protocol handler.

The front end requires monitoring and control by the protocol handler.

The Protocol Handler

The protocol handler acts as the logical interconnection between the front end and the local bus.

It prepares received data for processing by the microcode operating in the microprocessor of the message processor. It also prepares data that has been assembled by the microprocessor for transmission through the front end onto the ring.

It decodes addresses for recognizing received messages and strips messages from the ring that have been previously transmitted.

It checks that the ring is active and operational. Part of this checking is to identify and present protocol errors to the microprocessor for logging.

These logs are used to isolate the faulty element in the IBM Token-Ring network.

The protocol handler controls and maintains the low-level bit and byte protocols on the ring.

The Message Processor

The message processor acts as the master control element for the protocol handler and the TIC bus interconnection control in the TIC card. Interaction with these functional areas is across an 18-bit local bus. The message processor is the general name for the microprocessor (microcode and the hardware). It consists of the following items:

- A microprocessor
- Static random access modules (RAM) for message data
- Static random access modules (RAM) for parity
- Read-only storage module (ROS) for microcode.

The microprocessor uses the random-access memory (RAM) as workspace when processing instructions.

The message processor can set up control conditions or interrogate status across the local bus using MMIO-type operations.
Data is accessed and stored in the RAM by the protocol handler and TIC interconnection control using direct memory access protocol.

The RAM is also used as buffer space for messages to be passed from the ring to the TIC bus interconnection, and messages to be passed from the TIC bus interconnection to the ring.

Access to the buffer space by the protocol handler and the TIC bus control is also controlled by the microprocessor.

Transfers into and out of the RAM are performed using direct memory access (DMA) protocols.

TIC Bus Interconnection Control

The TIC interconnection control provides a mechanism for transferring data between TIC storage (RAM) and CCU storage, via cycle steal. It operates in halfword bus mode.

The function performed by the TIC bus interconnection control can be visualized as a double interface DMA controller with a 128-byte hardware store-and-forward buffer. The 128-byte buffer can logically connect either to the TIC bus interconnection control or to the local bus, but not to both at the same time.

When DMA data transfer is occurring at the TIC bus interconnection control, the TIC is the bus master, and the data can flow in only one direction (read or write) at a time.

In addition to its DMA function, the TIC bus interconnection control can also transfer data to or from TIC storage. This function is intended for adapter initialization and to obtain TIC status.

Receive Operation

On receive, data is taken from the ring into the front end, where it is reshaped into distortion-free digital signaling elements.

The front-end synchronizes itself with the received data stream and develops a clock which is boundary-aligned to the bit stream.

This bit stream, along with the derived clock, is passed to the protocol handler.

The protocol handler converts the encoded data stream into coding usable by the adapter.

By counting received clock pulses, the protocol handler assembles the bit stream into halfwords units.

Parity is generated on the received data de-serialized from the ring to check data validity through the adapter.

During the receive sequence, cyclic redundancy check (CRC) calculation is begun on the received data.

The destination address is compared against the stored values in the protocol handler to determine if the message is to be copied by the adapter. If so, the protocol handler conditions itself to begin the copy, and transfer is started to the message processor.

The destination and source addresses, the physical control field, the data portions, and the CRC characters of the in-progress received message are now passed to the message processor in sequence.

When the end of the CRC-protected field is received, the previously received CRC characters are compared to the calculated CRC.

- If there is a match, message reception is considered complete by the protocol handler.
- If there is a mismatch on the CRC check, the message processor is signalled that the message should not be considered valid.

The message processor assembles into multi-byte blocks the information received from the protocol handler.

When that assembly is complete, the message processor begins a transfer into CCU storage. These segment transfers continue until the complete message has been transferred.

When the transfer is completed, the message processor completes the receive operation by reporting the status of the transfer to the CCU.

Transmit Operation

Data flow during transmit operations is essentially the reverse of that during receive operations.

The message is accumulated by the CCU in CCU storage, and the message processor is set up with the storage location and length information. The message processor then does a storage-to-storage transfer of the message, including the destination and source addresses, from CCU storage to the message processor.

The message processor signals the protocol handler to begin transferring the message from the message processor resident storage into the hardware buffers of the protocol handler.

When the protocol handler senses that a transmission is pending, it begins the transfer into its buffers. After enough characters have been buffered, the protocol handler searches for a free token on the ring. When one is found, the token is changed to a busy token.

The control characters are generated, and transmitted.

Sequential transmission out of the buffers continues with the destination and source addresses.

When the entire information field has been transferred, the protocol handler inserts the CRC characters that have been accumulated in the message.

The protocol handler begins to remove (strip) any data from the ring that is being received.

The incoming data stream is searched for a match of the source address with the address of the TIC .

After a match is found and transmission is complete, the TIC encodes and transmits a free token on the ring.

The transmission of the free token is followed by a continuous transmission of idle characters.

The TIC also begins repeating the received data stream, and the transmit operation is considered complete.

Token-Ring Multiplexor (TRM) Card

The TRM card handles the operations between the CCU and the Token-Ring interface couplers (TICs).

On one side, the TRM interconnects the CCU and the MOSS through the IOC bus, and on the other side, the TRM interconnects the TICs through the TIC bus.

The TRM functions are:

- Receive and re-drive the lines toward the IOC bus
- Provide the clocking generation
- Perform the daisy chain continuity for the IOC bus serial lines
- Convert PIO operations into MMIO operations
- Convert DMA operations into cycle steal operations
- Can generate three different types of interrupt
- Check the validity of the transactions between the CCU or the MOSS and the TICs.

To perform these functions, several registers are located in the TRM:

- Buffer and the extended buffer
- TIC control register
- Interrupt request and bus request register
- Diagnostic register
- Level 1 error status register
- Level 2 error status register
- MOSS error status register.

IOC Bus Interconnection

The IOC bus interconnection allows communication between the TRAs and the CCU (NCP), or between the TRAs and the MOSS.

The IOC bus signal lines go to/from the TRM card bottom connector I/O pins.

See Chapter 4, "Buses and Switching" for more information.

Signal Line Names	Mnemonic	Initiated by	PIO/ TRM	AIO	Inter- rupt
Card present IN	+ PREIN	Adp.before	X	X	
Card present OUT	+ PREOUT	TRM	X	X	
Cycle steal request high	+ CSRH	TRM		X	
Cycle steal grant high	+ CSGH	CCU		X	
Cycle steal grant high previous	+ CSGHP	CCU		X	
Cycle steal priority line	+ CSPRY	TRM/adapt.		X	
CSG through tag	+ CSGT	TRM		X	
IOC data bus	+D0 – +D15	TRM/CCU	X	X	X
End of chain	+ EOC	TRM		X	
Halt	+ HALT	CCU	X	X	
Input/output	+ I/O	CCU	X	X	
Interrupt request removed	+ IRR	TRM	X	X	
Interrupt to MOSS	+ITMOSS	TRM	X	X	X
Level 2 priority line	+L2PRY	TRM/adapt.			X
Level 2 serial select line in	+L2SSLIN	Adp.before			X
Level 2 serial select line in previous	+L2SSINP	Adp.prev.			X
Level 2 serial select line out	+L2SSLOU	Adp.prev.			X
Modifier	+ M	TRM		X	
Parity valid	+ PV	TRM	X	X	
Parities	+P0,+P1	TRM/CCU	X	X	X
Power on reset	– POR	Power blck			
Reset	+ RESET	Switch			
TA	+ TA	CCU	X		
TD	+ TD	CCU	X	X	
Valid halfword	+ VH	TRM	X	X	X
Valid byte	+ VB	TRM		X	

Figure 5-12. Summary of the IOC Bus Interconnection Signal Lines

TIC Bus Interconnection

The TIC bus is a bidirectional bus which connects the TRM card to the TIC cards via the card bottom connector I/O pins and the board.

Three types of operation are used on this interface: DMA, MMIO, or IACK operation.

DMA Operation

The DMA operation allows transferring a burst of data between the TRM and the TIC.

During DMA operations, the TIC controls the bus and the TRM is the tributary unit.

MMIO Operation

The MMIO allows access to the registers of the IOC interconnection control of the TIC.

Interrupt Acknowledge (IACK) Operation

Interrupt acknowledge (IACK) cycles are used to access a vector in the TIC when the TIC requests an interrupt to the TRM. The vector indicates the cause of the interrupt.

Summary of the TIC Bus Signal Lines

Signal Line Names	Mnemonic	Initiated by	PIO/ MMIO	DMA	Inter- rupt
Address bus	+A1, +A2, +A3 - +A23, +APL, +APH, +APX, +A0	TRM, TIC TIC	X	X	
Data bus	+D0 - +D15, +DPL, +DPH	TRM, TIC	X	X	X
Address strobe	− AS	TRM, TIC	X	X	X
Card select(2)	− CS	TRM	X		
Read/write	+ RNW	TRM, TIC	X	X	X
Upper data strobe	− UDS	TRM, TIC	X	X	X
Lower data strobe	− LDS	TRM, TIC	X	X	X
Data transfer acknowledge	− DTACK	TRM, TIC	X	X	X
Bus error	− BERR	TRM		X	
Bus request(2)	− BR	TIC		X	
Bus grant(2)	− BGR	TRM		X	
Bus busy	− BBSY	TIC		X	
Bus release	− BRLS			X	
Interrupt request (2)	− IR	TIC			X
Interrupt acknowledge(2)	− IACK	TRM			X
Reset (2)	− RESET	TRM			
System clock	+ BCLK	TRM	X	X	X
System last Transfer	− SLT	TIC		X	

Figure 5-13. Summary of the TIC Bus Signal Lines

TRM Arbitration Mechanism

Since two TIC cards can be attached to the TRM, the TRM can simultaneously receive up to two bus requests for DMA, and up to two interrupt requests from the TIC cards.

The arbitration logic comprises two scan wheels, one for bus requests (BR), the other for interrupt requests (IR). Each wheel in turn can point to either of the two attached TICs.

Machine Internal Communications

The NCP running in the CCU can communicate with the TRM or TICs via three main operations:

- Programmed input/output
- Cycle steal
- Interrupt operations.

The TRM can communicate with the TICs via two operations:

- Memory mapped input output (MMIO) from TRM to TICs
- Direct memory access (DMA) from TICs to TRM.

See figure below.

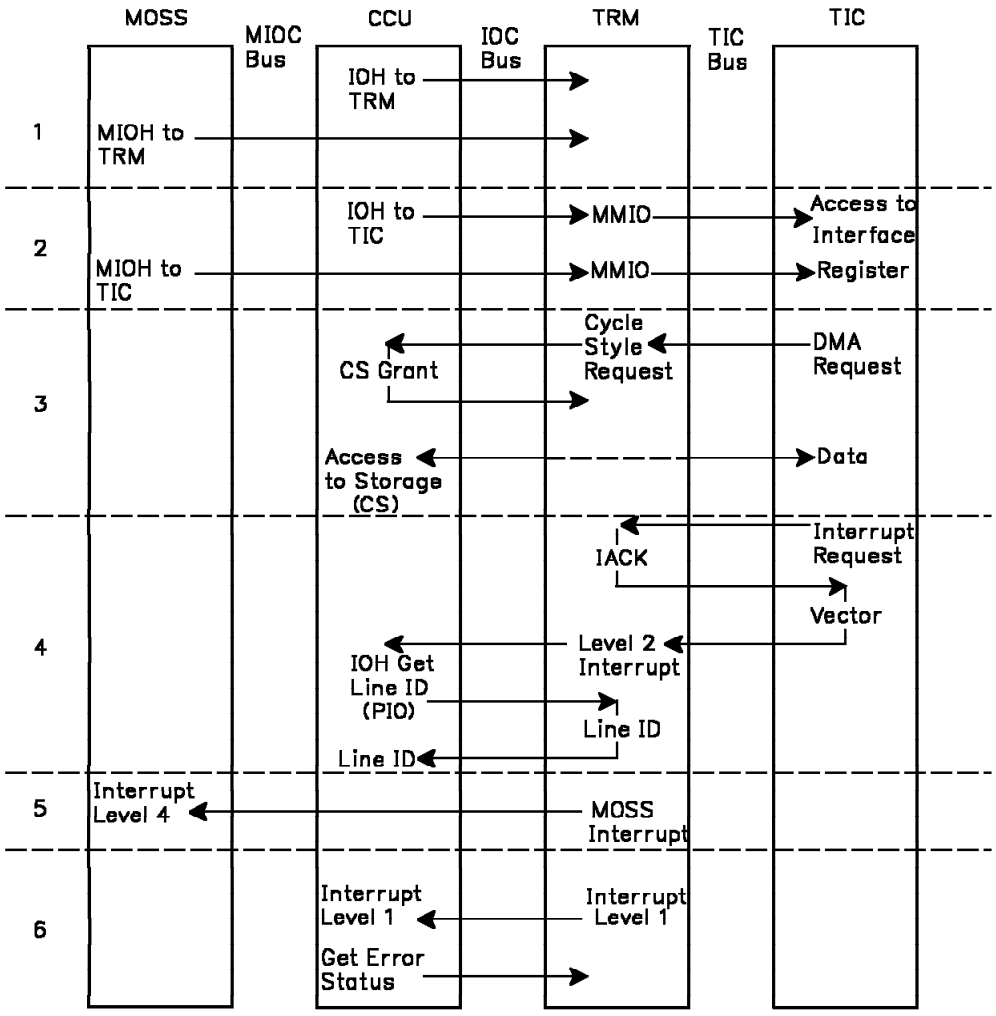


Figure 5-14. Internal Machine Communications

PIO-MMIO Operations

Direct communications are made at program level via input output halfword (IOH) instructions (1). These instructions are always passed on to the IOC bus through the program input or output (PIO) operation.

The PIO is decoded by the TRM and is either responded to directly if it addresses the TRM, or is transformed into a memory mapped input output (MMIO) (2) if it addresses an associated TIC card. (See “TRM Mapping of PIO to MMIO” on page 5-26 for details)

CS-DMA Operations

There are pointers in the TIC which enable the TIC to indirectly communicate (via the TRM) to the CCU, using CCU storage blocks.

Each TIC issues direct memory access (DMA) requests (3) to the TRM to fill or empty these storage blocks. These requests are passed to the IOC as cycle steal requests (3).

A cycle steal operation (AIO) which transfers the data between main storage and the TIC (via the TRM), is then performed through one of the IOC buses.

The program product uses IOHs to inform the TIC of the availability of new storage blocks (3). (See “TRM Cycle Steal Operations” on page 5-37 for details)

Interrupt Operations

The TIC can alert the CP via interrupt requests presented to the TRM (4).

The TRM determines what kind of interrupt has been raised by fetching an interrupt vector in the TIC (4).

The TRM then presents a level 2 interrupt request to the CCU (2).
The CCU then issues an IOH 'get line ID', which is responded to by the TRM with a line identifier determined by the value of the interrupt vector (4).

The TRM can alert the MOSS via the 'Interrupt to MOSS' (5). The MOSS is able to generate PIOs on the IOC bus by use of MIOH. (See “TRM Interrupt Operations” on page 5-39 for details)

The level 1 interrupt occurs in two cases (6):

1. When a TRA disconnect command is requested by the MOSS, a level 1 request is sent on the IOC bus.
2. When an error is detected on the IOC bus during an AIO or PIO operation.

Programmed Input/Output Operations

General PIO Operations

PIO operations are halfword operations driven either by the CCU or the MOSS.

- The CCU program execution generates IOH instructions which are transformed into PIO operations in order to control the attached TIC through the IOC.
- The MOSS can generate MIOH operations which are treated the same way as IOHs.

Support operations with the TRM and support operations with a TIC through the TRM by converting PIO operations into MMIO operations.

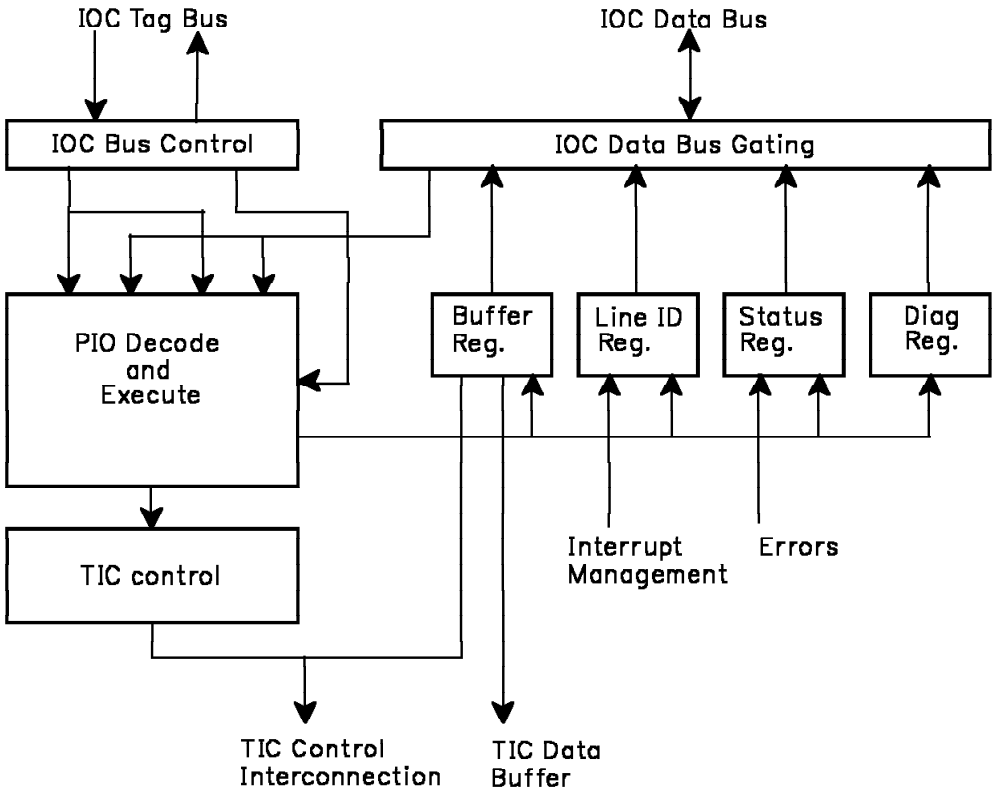


Figure 5-15. TRM PIO Example

The IOC bus control manages the IOC tags to synchronize the CCU and TRM exchanges.

The PIO decode and execute is the logic interconnection between the CCU and the different areas accessed in PIO mode.

The line ID register is a halfword register which stores the type A line identification for the first TIC. The other seven line IDs are calculated using the contents of this register. (refer to “Line Identification (Line ID) Generation” on page 5-40 for line ID type A and B definitions).

The 'status block' is a set of registers used to log hardware-detected errors. This set of registers include a level 1 error status register, two level 2 error status regis-

ters and a MOSS error status register. (For more details refer to “TIC Adapter Check Register” on page 5-53 and “MOSS Error Status Register” on page 5-52.)

The TIC control is used to control the operations of each TIC.

PIO Functional Description

TRM PIO Initialization

The TRM detects a request from the CCU when it detects that the I/O tag is active. At this time, the TRM can be in one of the following states:

Idle: Ready to enter a PIO sequence.

Interrupt Request Pending: Since interrupt requests are presented to the CCU on the data bus, the TRM and all other adapters on the IOC bus must remove their interrupt requests.

Cycle Steal Request Pending: Since cycle steal request (CSR) is presented to the CCU on a dedicated line, the TRM does not deactivate the request while performing the PIO operation.

TRM Direct Selection

The CCU knows the TRM address and sends it at TA time.
The TRM decodes its address by comparing the group address and IOC bus number of the address/command halfword to the board wired address. It also compares the type address to B'1001' and bit 14 (1=TRM 1, 0=TRM 2).

If all compares are equal, the TRM becomes selected and sends VH to the CCU.

TRM Indirect Selection

The CCU issues a PIO 'get line ID' when it honors a level 2 interrupt because it does not know which adapter requested service. In this case, the TRM becomes selected when it recognizes the get line ID command, and it is preselected.

Restrictions

- If the TRM is in CCU PIO disable mode, it can be selected only by the MOSS.
- When a CCU operation is initiated, the IOC bus is busy until the end of the operation. This operation cannot be overlapped by another operation such as an AIO.

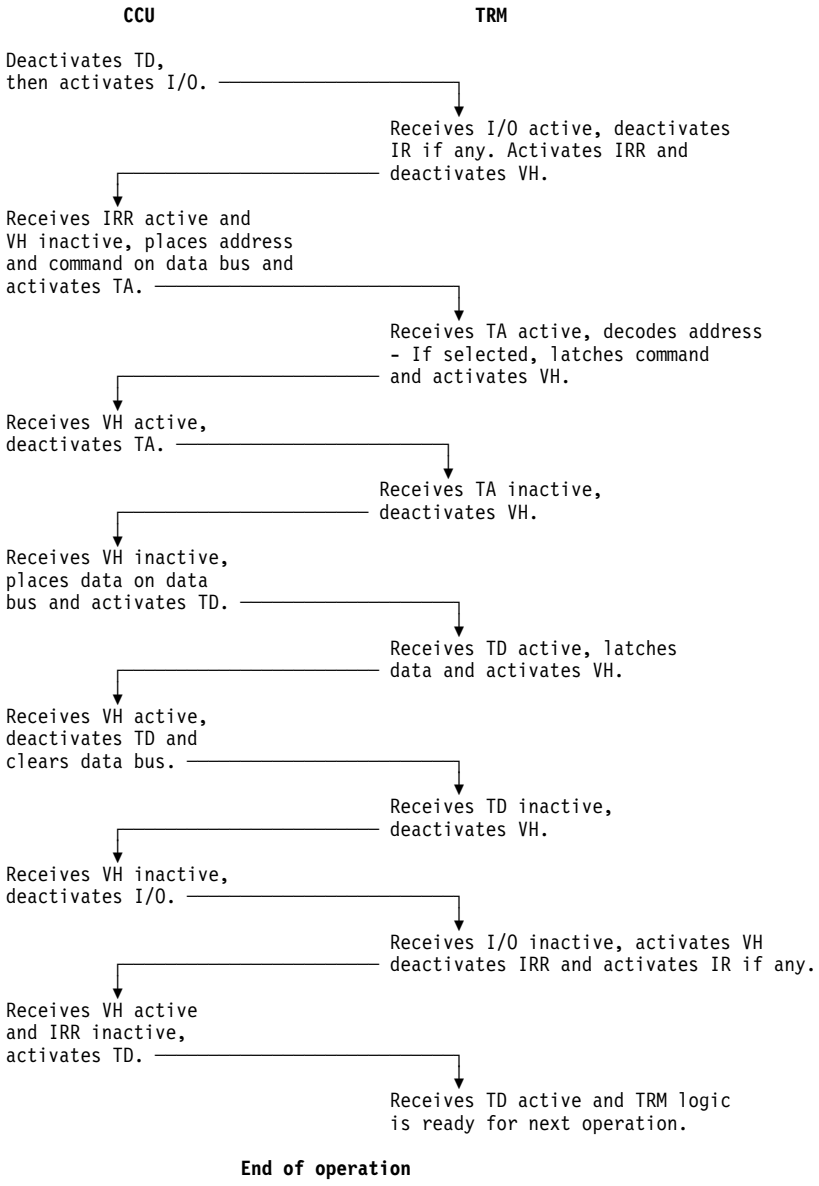
TRM MOSS Selection

When a PIO is executed by MOSS through the IOC, the MOSS bit is active in the command field.

TRM PIO Management

The TRM decodes and executes the PIO operations issued by the CCU.

PIO Write Sequence



PIO Read Sequence

Same as the write sequence except that, during TD time, the data is sent from the TRM to the CCU.

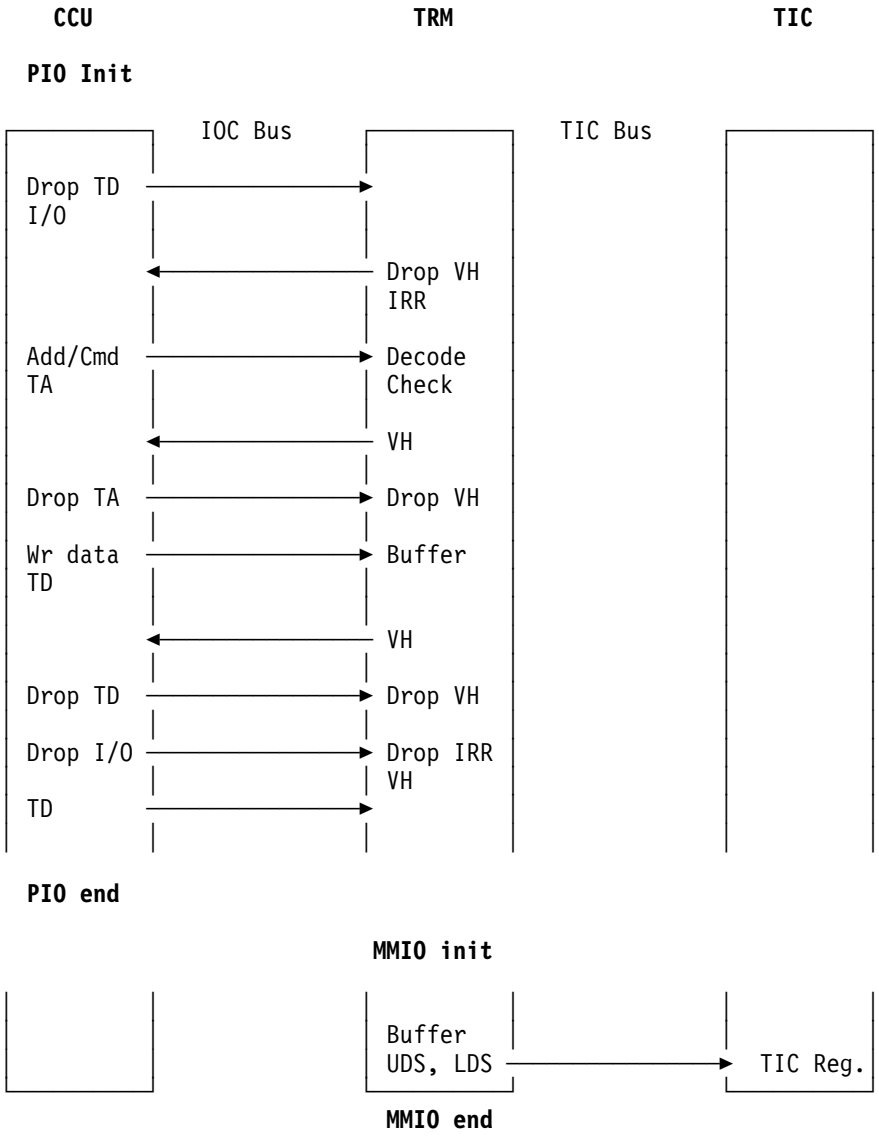
TRM Mapping of PIO to MMIO

Some PIOs are used to access the TIC cards. During these operations, (the protocol is the same on the IOC bus) MMIO operations are performed by the TRM on the TIC bus.

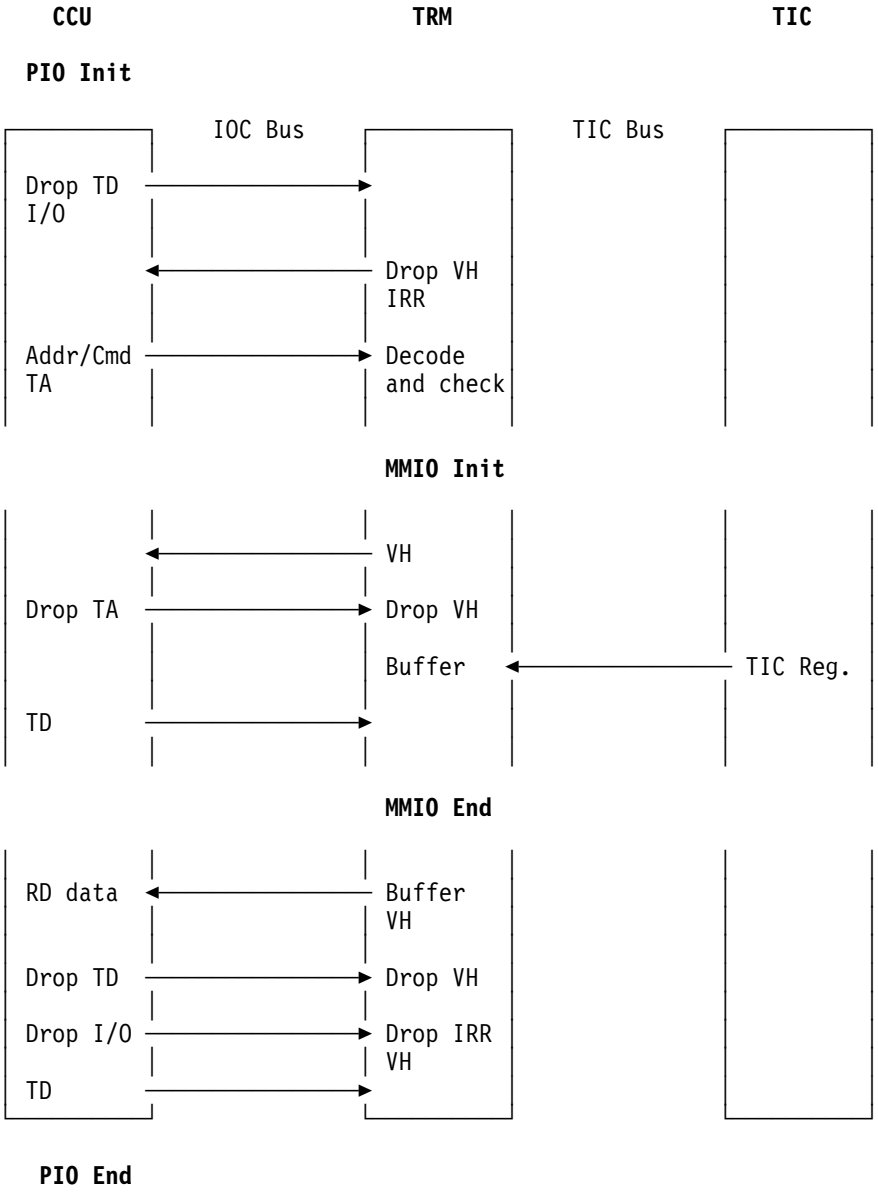
At TA time some bits are used to generate the address on the TIC bus, and at TD time the halfword data is transferred to the TIC data bus.

PIO/MMIO Hand-Shaking Mechanism

PIO/MMIO Write



PIO/MMIO Read



PIO Format and Types

PIO Format at TA Time

The PIO function is used to address registers in the TRM and in the TIC.

The format follows the general rules of the machine to allow compatibility with the other adapters.

The type address in the first byte selects the TRA.

The group selects two TRMs on one IOC bus. Thus, the first byte is used to address only one board in the machine with a TRA installed.

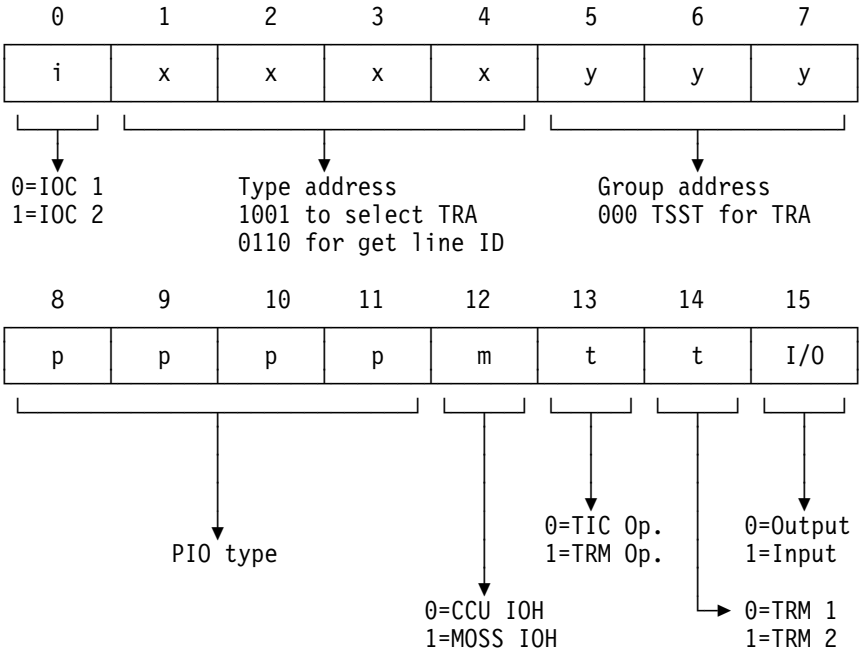
The diagram below shows the PIO format at TA time.
Most figures in this section are shown in IOC bus format.
Bit 0 is the most significant bit and bit 15 is the least significant one.

The get line ID PIO is also used and has a special format.

It uses the B'0110' group address and byte 1 must be X'01'.

There are two types of PIO operation, one type for the TRM and another for the TIC.

TA Field



List of the PIO Types for TRM

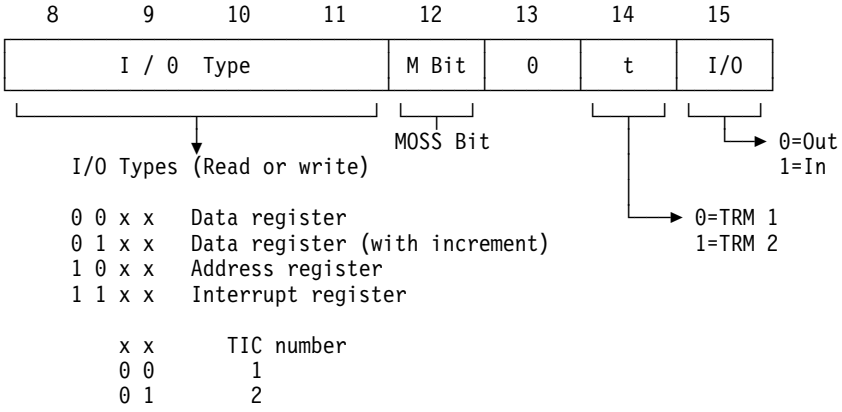
PIO Types Decoding	Function During Read	Function During Write
Bit 8 9 10 11		
0 0 0 0	Get line ID (CCU)	
0 0 0 0	Get command completion (MOSS)	Start/Stop/Mask/Unmask from MOSS
0 0 0 1	Get TRM control register	Set TRM control register
0 0 1 0	Get TIC control register	Set TIC control register
0 0 1 1	Read line ID base	Load line ID base
0 1 0 0	Read IR/BR register	Write IR/BR register
0 1 0 1	Read diagnostic register	Write diagnostic register
0 1 1 0	Read buffer register	Write buffer register
0 1 1 1	Read extend buffer register	Write extended buffer register
1 0 0 0	Read computed line by MOSS	Programmed reset TRM
1 0 0 1	Get level 2 error status TICx-1	┐
1 0 1 0	Get level 2 error status TICx-2	│
1 0 1 1	Not used	│
1 1 0 0	Not used	├ Invalid codes
1 1 0 1	Get level 1 error status	│
1 1 1 0	Get MOSS error status register	│
1 1 1 1	Read CSCW	┘

Note: Usage of unused codes will be detected as an invalid IOH.

PIO Types for TIC

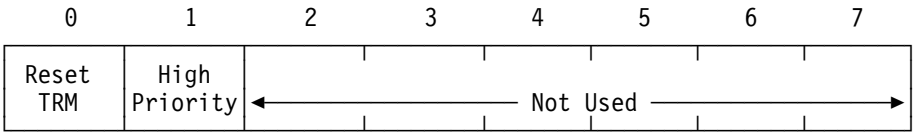
Below is the encoding of the TA field for TIC PIO/MMIO operations. The format of byte 0 is the same as the PIO format at TA time.

TA Field



Set/Get TRM Control Register

TD Field Byte 0 (Byte 1 not used)



Reset TRM

The reset TRM is set by the program, using the IOH programmed reset TRM (PIO type 1000), or either the power-on reset or the tag reset.

Reset by the program via the set TRM control register with TD bit 0 OFF.

The reset TRM bit is only an indicator of a previous reset. Setting this bit via a set TRM control register IOH does not perform any reset function.

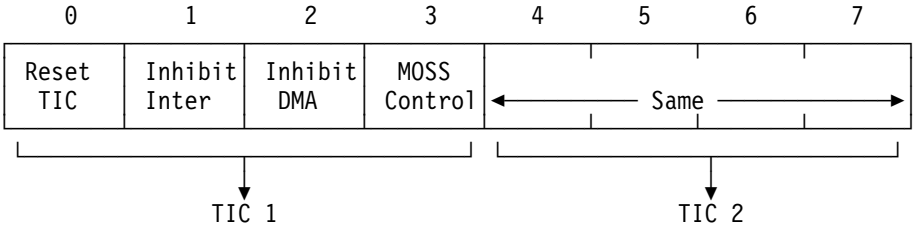
Refer to “TRA Resets” on page 5-48 for more details.

High Priority

- Set by the program to give this TRM high priority in the level 2 interrupt and cycle steal request mechanisms.

Set/Get TIC Control Register

TD Field Byte 0 (Byte 1 not used)



Reset TIC

Controls the reset line of each TIC.

The reset TIC bit is set by either the power-on reset and the reset tag or a set TIC control register PIO. A programmed reset TRM does not affect this bit.

The power-on reset is activated during machine power-on or during selective power-on sequence.

The reset tag line is activated by the MOSS (for fall-back or switch-back procedures).

Inhibit Interrupt
TIC interrupt request is ignored by the TRM.

Inhibit DMA
TIC DMA request is ignored by the TRM.

MOSS Control
A TIC interrupt is switched from a level 2 interrupt to a MOSS interrupt.

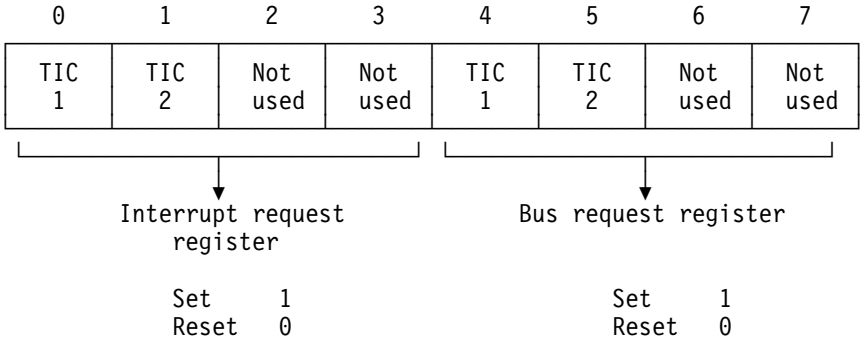
The MOSS error status register is used instead of the level 2 error status register to log errors.

Write/Read Interrupt Request and Bus Request Register
This register is used by diagnostics to simulate interrupt requests and bus requests in order to check the interrupt and DMA mechanisms.

The read command is used for isolation in case of errors reported in level 3.

During wrap mode, the value set by a write IR/BR PIO will remain until another write IR/BR PIO is performed. However, during normal operation, that value will follow the tags coming from the TIC bus.

TD Field Byte 0 (Byte 1 not Used)



TRM Buffer and Extended Buffer
The buffer register is a two-byte register.
The extended buffer is a single-byte register which is accessed on byte 1 of the IOC bus.

These buffers are placed between the IOC bus and the TIC bus. All data and addresses are passed from one bus to the other via these buffers.

TRM PIO Command Description

Fast Get Line Identification

This is the command by which the program running in the CCU is able to find the origin of the level 2 interrupt.

This command is a broadcast command which is answered by the first adapter in the daisy chain with a level 2 interrupt pending.

The line identification (line ID) is computed by the TRM using the following algorithm:

```
Base + (8 x (TIC number – 1)) + (4 x line ID type)

     Base         = Data loaded by the PIO 'load line ID base'
     TIC number   = 1–2
     Line ID type = 0 for type A
                    1 for type B
```

See “Line Identification (Line ID) Generation” on page 5-40

The level 2 interrupt is reset in the TRM upon successful completion of the 'get line ID' PIO.

Read Computed Line ID by MOSS

The function of this PIO is the get line ID except that it is not a broadcast command and is always answered by the addressed adapters.

This command is issued by the MOSS.

Read/Load Line ID Base

This function is used to load the first line ID in the halfword register during TRM initialization. This register can be read by the program.

The use of line ID base is described in the get line ID command above.

Get Command Completion

TD Field

0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0

8	9	10	11	12	13	14	15
MOSS Int.	0	0	0	Level 2 Int.	MOSS Status Int.	MOSS Dire. Int.	MOSS Int. Mask

Get command completion is used by MOSS to answer an interrupt.

Bit 8 of the MOSS interrupt allows MOSS to verify that the addressed adapter is the originator of the interrupt.

Bit 8 is automatically reset by the TRM at the get command completion unless the operation is abnormally terminated by a halt.

Bit 8 will stay active if the get command completion is terminated by a halt.

Bit 12 indicates that a status is pending in one of the level 2 error status registers.

Bit 13 indicates that a status is pending in the MOSS error status register.

Bit 14 indicates that the interrupt request from a TIC under MOSS control is active.

Bit 15 detects the current state of the MOSS interrupt mask.

Set Command

Four commands are defined, based on the data sent at TD time.

Stop Command TD=X'0B00' is used by MOSS to start the disconnect process.

Start Command TD=X'0C00' is used by MOSS to reconnect a TRA.

Mask Command TD=X'8000' will mask all the interrupts to MOSS except the 'disconnect end of operation' MOSS interrupt request. The state of the 'mask' can be checked by the get command completion.

Unmask Command TD=X'4000' will unmask the interrupts to MOSS.

All other TD values cause no action to take place. The PIO will complete without error, however, if the other TD values are used.

Programmed Reset TRM

The programmed reset TRM resets the TRM but does not force a reset to the attaching TICs.

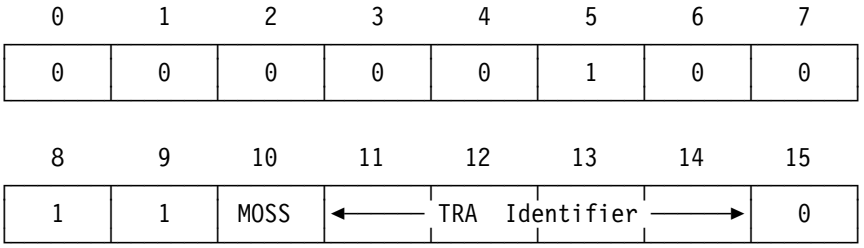
This command will set the reset bit in the TRM control register.

The disconnect and CCU PIO disabled state of the TRM is not changed by a programmed reset.
The TD field is not used by this PIO.

The next PIO issued to the TRM after a programmed reset must be a get TRM control register PIO.

Read CSCW

TD Field



The read CSCW is a diagnostic function to read the CSCW. (For more details see “TRM Cycle Steal Operations” on page 5-37.)

The MOSS bit is set to 1 if the TRM is under MOSS control (CCU PIO disabled).

For a description of the TRA identifier see “TRM Cycle Steal Operations” on page 5-37.

TRM Cycle Steal Operations

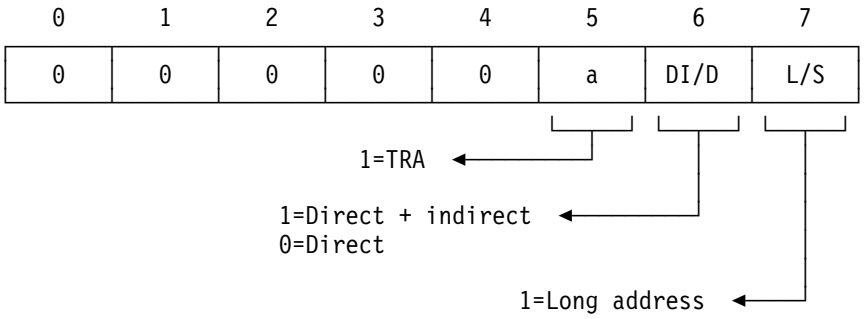
In the 3745 controller, the IOC bus is managed by the CCU. For data transfer, an adapter accesses the main storage without program intervention trough CS operations.

Cycle steal is also called an adapter-initiated operation (AIO) because it is initiated by an adapter when the adapter wants to transfer data to or from main storage without using the control program.

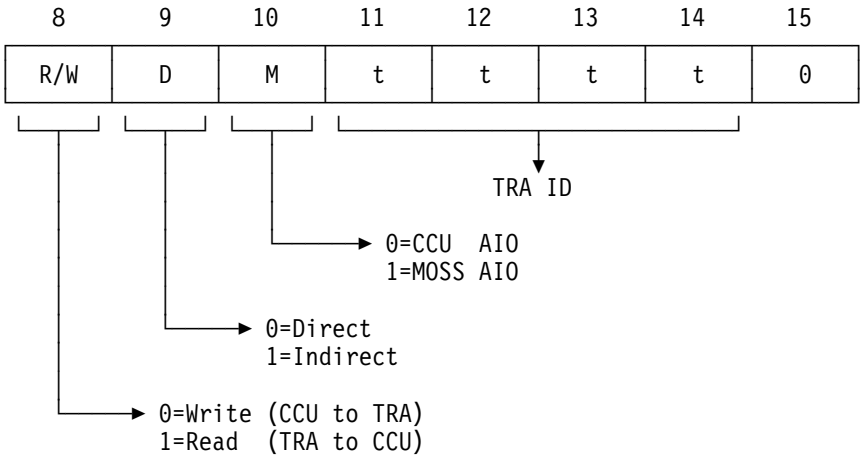
Different types of cycle steal operations are identified by a control halfword called the cycle steal control word (CSCW).

The CSCW is sent by the adapter as the first data halfword during a cycle steal operation. The format of the CSCW is:

TA Field Byte 0



TA Field Byte 1



Direct Long and Indirect Operation for Normal Cycle Steal

The CSP and TRA use a shared pointer register X'F' (IOC 1 pointer register X'3F' and IOC 2 pointer register X'6F') for cycle steal operations. For this reason the direct/indirect transfer mode is used as follows (bit 6=1):

- The first two halfwords of data after the CSCW (address high, address low) are used to load the pointer register X'F'. Since it is a 22-bit register, 2 halfwords are needed. Therefore, 'long' is specified in CSCW bit 7.

- The next halfword of data will be stored into CCU storage or will be read from CCU storage (depending on the R/W bit in the CSCW) according to the address contained in the pointer register.

  For each halfword transmitted, the pointer register will be advanced by 2.

Since the pointer register is fixed (X'F') and known, there is no need to include it in the CSCW. Therefore, bits 11 to 14 are used as an identification for the TRA.

If a level 1 interrupt occurs for an AIO, the CCU can read the following information by executing an input '75':

CSCW bit 5=1 for TRA or CSP
CSCW bits 11-14 for TRA ID

The TRA identification number is composed of the 3-bit group address (board address) in bits 11-13 and bit 14 which is 1 for TRM 1 or 0 for TRM 2. This TRM ID enables the program to determine which adapter was performing an AIO when an error occurs.

Direct Short Operation for Error Cycle Steal Operation

This operation is used in case an error is detected at the beginning of a TIC DMA operation. In this case, the TRM modifies the CSCW to direct and short mode which allows the TRM to stop the operation after sending only one address halfword to the IOC pointer register.

The address halfword is sent as all zeros.
The pattern for the error CSCW is B'0000 0100 r1mt ttt0'.

TRM Mapping of DMA to Cycle Steal

Exchanges of control blocks or data buffers between the CCU storage and the TIC RAM are initiated by the TIC.
The DMA operations are mapped by the TRM to cycle steal operations on the IOC bus.
The TRM manages the bus-to-bus timings and acts as the vehicle by which addresses and the data are transferred between the CCU and the TIC.
The CCU addresses are provided directly by the TIC. They have been previously loaded into TIC storage by the NCP token-ring function.
A single byte can be presented on the IOC bus only if it is the last byte transferred.
The TRM transfers over the IOC bus in 64-byte bursts.

TRM Interrupt Operations

The TRM can generate three different types of interrupt:

Level 1 Interrupt

For a disconnect function initialized by the MOSS.
This interrupt is put in the IOC bus byte 1 bit 5 between PIO and AIO operations.

The IOC will also generate a level 1 interrupt for errors it detects during a PIO or AIO with the TRM.

The control program is able to analyse the interrupt from the external register X'76'.

Note: For level 1, the first adapter on the IOC bus will be serviced first. Since the MOSS works with only one adapter at a time, no contention is possible.

Scenario for IOC Level 1 Error Recovery

Origin			Operation	TA	TD
MOSS	TRM	NCP			
X			Send halt tag		
X			Raise level 1 interrupt		
	X		Load level 1 error status register		
		X	Read external registers 7E, 76, 75		
		X	Reset IOC level 1		
		X	Get level 1 error status	X'cctt'	X'rrrr'

```
cc   TRM address B'x1001sss'

     x is the IOC number
     sss  is the group address (always 000 for TRA)
     (cc=X'48' for IOC1 or X'C8' for IOC2 )

tt   X'D5' for TRM 1, X'D7' for TRM 2
rrrr is the level 1 error register contents
     (see note below and get level 1 error status register)
```

Note: For compatibility with the TSS and existing NCP error recovery code, the response to a get level 1 error status for an error on a get line ID is B'1xx11xxx1xxxxxxx'.

Disconnect Operation Scenario

Origin			Operation	TA	TD
MOSS	TRM	NCP			
X			Disconnect (TRA stop)	X'cctt'	X'0B00'
	X		Level 1 to NCP		
	X		Load level 1 error status register		
		X	Get level 1 error status TRM	X'ccrr'	X'8100'

tt X'04' for TRM 1, X'06' for TRM 2
cc TRM address B'x1001sss'

x is the IOC number
sss is the group address (always 000 for TRA)
(cc=X'48' for IOC1, X'C8' for IOC2)

rr is X'D5' for TRM 1, X'D7' for TRM 2

Level 2 Interrupt

The level 2 interrupt is issued to the CCU when the TRM passes an interrupt initiated by a TIC or when an interrupt is generated as the result of an error detected by the TRM.

This interrupt is put in the IOC bus byte 0 bit 1 between I/O operations.

For level 2, a priority mechanism at TRM level, is used to resolve contention between the different adapters.
Each adapter can be set to either high or low priority.
For adapters set to the same priority, the first adapter on the IOC bus will be serviced first.

Line Identification (Line ID) Generation

When the CP receives a level 2 interrupt, it places a PIO get line ID command on the IOC bus.

This command is decoded by all adapters. However only one, according to the level 2 interrupt priority mechanism, will answer with a line ID.

For adapters set to the same priority, the first adapter on the IOC bus will be serviced first.

The line ID allows the program to identify the requesting adapter and to process the interrupt.

There are 2 different line IDs per TIC:

- Type A. For the TIC interrupts for which the system status is cycle-stolen to the CCU.
- Type B. For the TIC interrupts for which the system status is not cycle-stolen to the CCU (SCB clear or adapter check) and interrupts generated for TRM-detected errors.

The get line ID command resets the level 2 interrupt and the TRM is now free for another operation including an interrupt (IR) from another TIC.

The CCU interrupt code sequence ends with a reset interrupt PIO/MMIO to the concerned TIC.

The TIC will lower its interrupt line and this will allow the TRM to treat another interrupt coming from the same TIC.

In its turn the TIC is free for other operations.

Interrupt to MOSS

This interrupt is sent to the MOSS over a dedicated line.

The TRM sends an interrupt to MOSS instead of a level 2 interrupt to the CCU when a TIC is under MOSS control, when the TRM is disconnected from the NCP or when an error is detected during an MIOH.

Scenario for Interrupt to MOSS

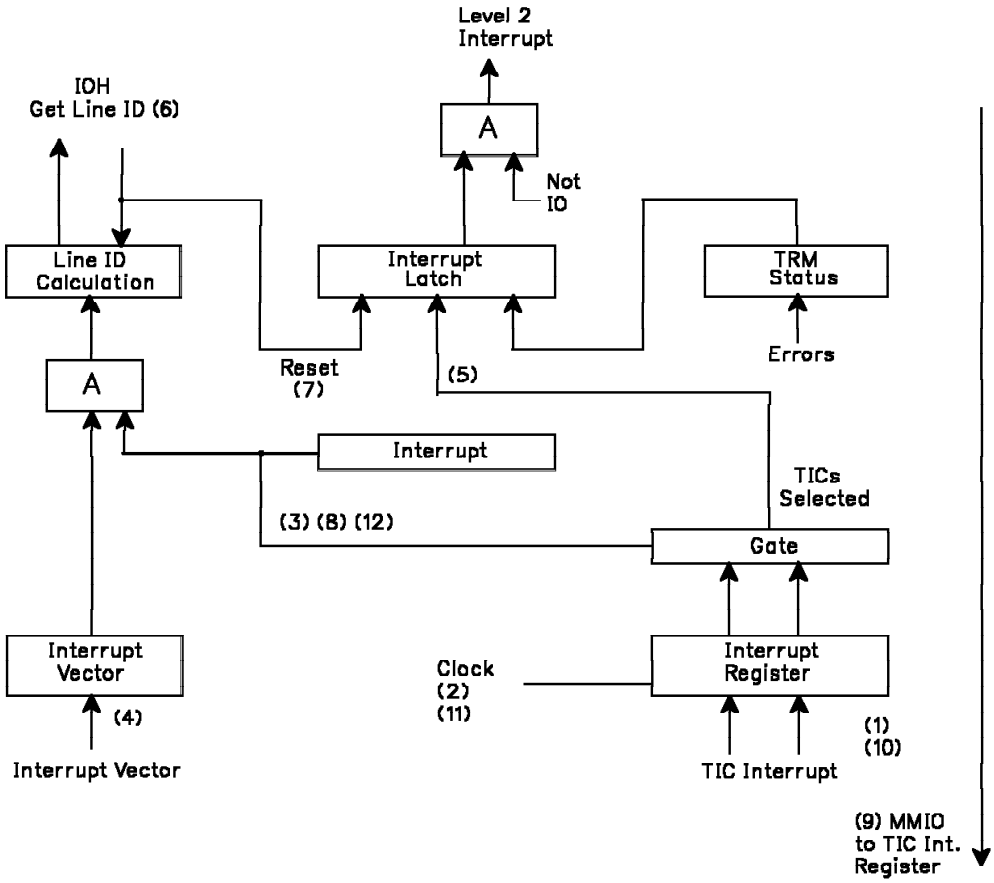
Origin		Operation	TA	TD
TRM	MOSS			
X		Raise interrupt to MOSS		
	X	Get command completion	X'cctt'	X'yyyy'
X		Clear interrupt to MOSS		

```
cc   TRM address  B'x1001sss'

     x is the IOC number selected (0 for IOC1 or 1 for IOC2)
     sss  is the group address (always 000 for the TRA)

tt   is X'0D' for TRM 1 or X'0F' for TRM 2
yyyy is the command completion value in the TRM
```

TIC Interrupts



(1) TIC n raises an interrupt.
(2) Interrupt is stored in TRM IR/BR register.
(3) TIC n selected.
(4) TRM inputs interrupt vector.
(5) TRM raises a level 2 interrupt.
(6) CCU issues get line ID.
(7) Get line ID resets TRM level 2 interrupts.
(8) Another TIC is selected if another request
is stored in the TRM interrupt register
(9) CCU resets the TIC interrupt.
(10) TIC n interrupt falls.
(11) TIC n interrupt is reset in the TRM IR/BR register.
(12) Interrupt from TIC n will now be honoured.

Figure 5-16. TIC Interrupt Management by the TRM

TIC Interrupt Scenario

1. The TIC interrupts the CCU when the TIC or ring status has changed.
2. The TIC will cycle steal (DMA) the system status, if any, to the CCU and then send an interrupt request to the TRM.
3. The TRM raises interrupt acknowledgment.

4. Upon receiving acknowledgment, the TIC gates the interrupt vector onto the lower data bus.
   Two bits of the interrupt vector are then read into the TRM level 2 error status register.

   - The interrupt vector identifies the cause of the interrupt.

     Six interrupt vectors are loaded into the TIC during initialization. Each vector consists of one byte. Each byte contains a value which identifies the cause of the interrupt:

     – Command status
     – Transmit command status
     – Receive command status
     – Ring status
     – SCB clear
     – Adapter check.

5. Upon receiving a vector, the TRM sends a level 2 interrupt to the CCU.

   When it receives a get line ID from the CCU, it places the proper line ID on the IOC bus at TD time.

   The line ID is based on the line ID base, TIC number and received vector (See “TRM PIO Command Description” on page 5-34 for details).

6. The TIC then waits for a reset interrupt MMIO operation or a retry.

7. If the TRM detects an error during a TIC interrupt, it will log an error in the level 2 error status register and request a level 2 interrupt.

   When the error is reset by the error recovery procedures, the TIC interrupt acknowledge will be retried.

Origin			Operation	TA	TD
TIC	TRM	NCP			
X			Cycle steal SSB (8 bytes) into CCU storage (not done for 'Adapter Check' and SCB clear interrupt types)		
X			Interrupt request		
	X		Read interrupt vector 8 bits		
	X		Level 2 to NCP		
		X	Get line ID	X'x001'	
	X		Send line ID type A or B answer the get line ID		X'llll'
	X		Reset level 2 interrupt if get line ID is terminated normally		
		X	Reset TIC interrupt	X'nnnn'	X'A000'

x depends on the IOC bus number selected
(x = 3 for IOC 1 or B for IOC 2)

llll is the line ID type A or B

nnnn is B'x100 1sss 11rr 00t0' where:

sss is the group address (always 000 for TRA)
rr is TIC number
t is the TRM number (0=TRM 1, 1=TRM 2)

TRM Interrupt Scenario

The TRM interrupts the CCU only in case of an error. When the TRM detects an error during an operation with a TIC, it logs the error into the TRM level 2 error status register associated with the TIC, and activates a level 2 interrupt request to the CCU. Then, it presents a type B line ID and the program reads the TRM error status register.

Origin			Operation	TA	TD
TIC	TRM	NCP			
	X		Load level 2 error status register		
	X		Level 2 interrupt request sent to NCP		
		X	Get line ID	X'x001'	
	X		Send line ID B to answer the get line ID		X'bbbb'
	X		Reset level 2 interrupt if the get line ID is terminated normally		
		X	Get level 2 error status	X'pppp'	X'vvvv'

x depends on the IOC bus number selected
(x = 3 for IOC 1 or B for IOC 2)

bbbb is the line ID type B

vvvv is level 2 error status value

pppp is B'0100 1sss kkkk 0000' where:

sss is the group address (always 000 for TRA)
kkkk is the PIO code according to the TIC number

Line ID Loading

Line ID loading is part of the TRM initialization process.

With a PIO operation the program sets the line ID base which corresponds to the type A line ID for the first TIC.

The line ID base is initialized to X'0000' after a TRM reset.

TRA Disconnect/Connect Function

These functions are initiated by the MOSS.

A level 1 interrupt to the CCU is raised by the TRM after it receives the stop PIO command.

Disconnect Function

The disconnect function disables the TRM for all PIO operations from the NCP. PIOs from the MOSS are still accepted and concurrent diagnostics can be run when the TRM is this state.

This function also prevents the TRM from sending any level 2 interrupt to the NCP. Errors and TIC interrupts will be reported to MOSS when the TRM is in the disconnect state.

As soon as the CCU PIO disable latch is set, an IOC time out will occur in case of an IOH sent to the TRM from the NCP.

Connect Function

The connect function allows the reconnection of the TRA to the NCP. The MOSS also informs the control program.

The origin of a PIO is determined to be from MOSS if IOC data bus bit 12 is ON during TA time.

Origin			Operation	TA	TD
MOSS	TRM	NCP			
X			Disconnect (TRA stop)	X'cctt'	X'0B00'
	X		Set latch disconnect		
	X		Level 1 to NCP		
		X	Get level 1 error status register	X'ccrr'	
	X		Set latch CCU PIO disable		
	X		Send interrupt MOSS		
X			Get command completion	X'ccuu '	X'zzzz'
X			Connect (TRA start)	X'cctt'	X'0C00'
	X		Reset latch disconnect		
X			Inform the NCP		

cc TRM address B'x1001sss'
x is the IOC number selected (0 for IOC1 or 1 for IOC2)
sss is the group address (always 000 for the TRA)

tt is X'0C' for TRM 1 or X'0E' for TRM 2
rr is X'D5' for TRM 1 or X'D7' for TRM 2
uu is X'0D' for TRM 1 or X'0F' for TRM 2
zzzz is the command completion value in the TRM

TRA Resets

Three functions are implemented to reset the TRA (TRM and TICs) or a part of the TRA:

1. The power-on/tag reset function
2. The programmed reset function
3. The TIC reset function.

Power-ON Reset/Tag Reset

These resets are activated in two ways:

1. By the power-on reset line coming from the power blocks.
2. By the reset tag coming from the switch card.

It completely resets the TRA:

- All requests on the IOC bus are deactivated.
- The TRM reset bit is forced ON in the TRM control register (which indicates a reset has been done).
- The TIC reset bits are forced ON (and the reset leads on the TIC bus) in the TIC control register.
- All the interrupts and their associated statuses are reset.
- The disconnect bit and the CCU PIO disable bit are reset.
- The entire control logic is forced to idle state.
- The BR and IR scan wheel is pointed to the TIC 1.
- More generally, all other functions and all other registers are forced in their inactive state.

Programmed Reset

The programmed reset is initiated by a PIO (IOH or MIOH). It allows the program to reset the TRM without resetting the attached TIC(s) and the connect/disconnect state of the TRM.

The result is the same as the hardware reset except the TIC reset bits, the disconnect mode latch, and the CCU PIO disabled latch are left in their current state.

TIC Reset

The program can perform a selective reset of the TIC by setting or resetting the TIC control register TIC reset bit. The reset bits are connected to the TIC reset leads on the TIC bus. The reset lead is active as long as the reset bit is ON in the TIC control register. The TIC reset lead causes the TIC to disconnect itself from the ring and perform a reset.

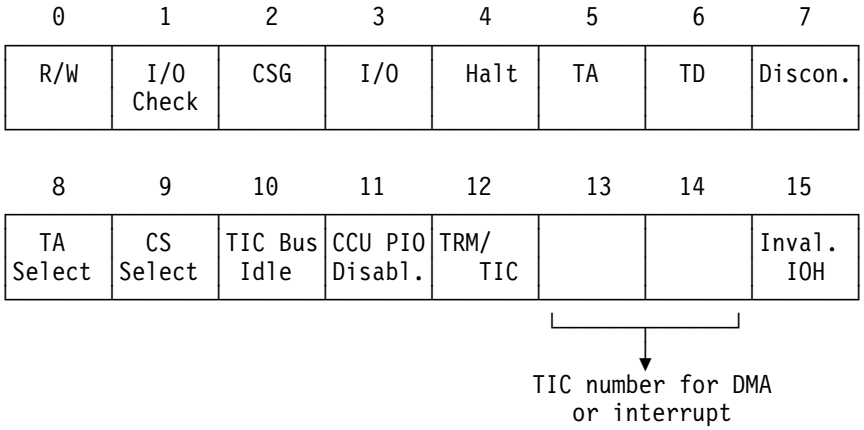
Diagnostic Section TA0A

The TRM must be 'disconnected' before running the diagnostic section TA0A. The 'disconnect' command must be performed after each power-OFF to power-ON.

Error Detection and Reporting

TRM Level 1 Error Status Register

TD Field



Level 1 interrupts can be generated by the:

- TRM on disconnect
- IOC on time out, bus-in parity, CSCW, storage protect or address exception errors.

Error reporting using IOC level 1 interrupts is limited to errors occurring on the IOC bus and errors detected by the IOC.

TRM internal errors and the TIC interconnection errors found during PIO/MMIO, DMA/CS, or read interrupt vector operations, are reported by a level 2 interrupt for the appropriate TIC.

The pattern in the level 1 status register for a disconnect level 1 interrupt has the following value B'1000000100000000'.

When the CCU IOC logic detects an error, it raises the halt tag.

When the TRM detects the halt tag, it sets the level 1 status register with the exception of bits 7 and 11.

Bits 7 and 11 reflect the status of the indicated latches when the get level 1 error status register PIO is executed.

During an IOC level 1 interrupt, bits 0-3, 5-6, 8-10 and 12-15 are valid only if bit 4 is ON.

Bit 0 This bit (R/W bit) is ON if a read PIO/AIO is being executed. It is OFF if a write PIO/AIO is being executed. The R/W bit is always ON for a disconnect level 1 interrupt. It is valid only if bit 8 or 9 is ON for an IOC level 1 interrupt.

Bit 1 This bit (I/O check) is ON if the TRM detects a parity error on the IOC bus when the halt tag is activated.

Bit 2 This bit (CSG) is ON if the CSG tag in the TRM is active when the halt tag is activated.

Bit 3 This bit (I/O) is ON if the I/O tag in the TRM is active when the halt tag is activated.

Bit 4 This bit (halt) is ON if the TRM has detected the activation of the halt tag on the IOC.

Bit 5 This bit (TA) is ON if the TA tag into the TRM is active when the halt tag is activated.

Bit 6 This bit (TD) is ON if the TD tag into the TRM is active when the halt tag is activated.

Bit 7 This bit (disconnect) is ON if the TRM is in disconnect mode when the read level 1 error status register PIO is executed.

Bit 8 This bit (TA select) is ON if the TRM has recognized its address (with good parity) and the PIO has not completed when the halt tag is activated.

Bit 9 This bit (CS select) is ON if the TRM has trapped CSG for an AIO and the AIO has not completed when the halt tag is activated.

Bit 10 This bit (TIC bus idle) is ON if the TRM detects that the TIC bus is idle when the halt tag is activated.

Bit 11 This bit (CCU PIO disable) is ON if the TRM is disabled for CCU PIOs when the read level 1 error status register is executed.

If the TRM is CCU PIO disabled, the level 1 error status register can be successfully read only by an MIOH.

Bit 12 This bit (TRM/TIC) is ON if an AIO or a get line ID PIO is being executed by the TRM when the halt tag is activated.

If this bit is ON, it means that bits 13 and 14 are valid.
If this bit is OFF, it means that the error cannot be associated with any particular TIC.

Bits 13 and 14 Bits 13 and 14 are used to encode the TIC number for some errors.

During a cycle steal operation, bits 13 and 14 are used to identify the TIC that was doing the DMA operation when the halt tag was received. They also indicate the originator of the level 2 interrupt for an error during a get line ID PIO. These bits are valid only if bit 12 is ON.

00=TIC 1
01=TIC 2

Bit 15 This bit (invalid IOH) is ON if the TRM decodes an invalid PIO type when the halt tag is activated. This bit is valid only if bit 5 is ON.

TRM Level 2 Error Status Registers

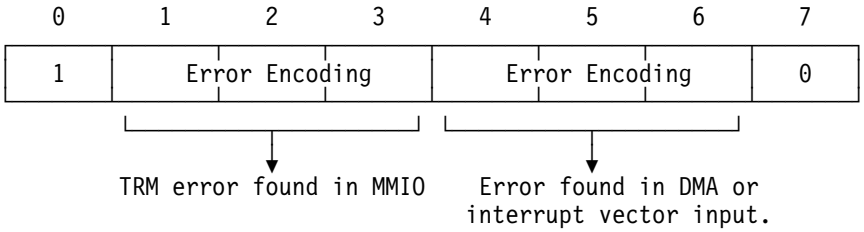
The TRM provides two level 2 status registers (one per TIC).

The level 2 status information is set by the TRM when an error is found in the TRM (not on the IOC bus), an error is detected on the TIC interconnection, or the TIC requests an interrupt.

This information can be read by the program through a get TRM level 2 error status command. The error or status is reset if the PIO read operation completes with no errors. After the status is successfully read, the TRM is able to log another error or status.

FORMAT 1 (Error Detected by TRM)

TD Field Byte 0 (Byte 1 not Used)



Error Encoding:

0 0 0 No error
0 0 1 TRM internal
0 1 0 TIC interconnection type 1
0 1 1 TIC interconnection type 2

Internal The TRM is suspected.

Type 1 The working TIC is suspected.

Type 2 All TICs can be suspected (idle state error).

This error encoding is performed by the TRM using the checkers in the TRM (See “Error Detection and Reporting” on page 5-49).

The status provides two independent error fields:

1. PIO/MMIO operations which require program retry
2. Operations which do not require program retries:
   - DMA (TIC retries automatically)
   - Input interrupt vector (TRM automatically retries)

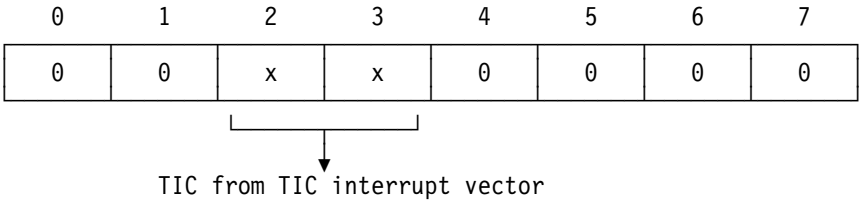
Both fields can be significant at a given time.

When a field is set, another error will not be set in the same field until it is reset by a successful 'get TRM level 2 error status'.

A DMA or input interrupt vector operation is retried automatically when the error in the level 2 error status register is reset by a successful 'get TRM level 2 error status' PIO.

FORMAT 2 (Interrupt Request by the TIC)

TD Field Byte 0 (Byte 1 not Used)



Format 2 is used when a TIC requests an interrupt.

The contents of this register will be:

B'00100000' for the SCB clear vector.

B'00010000' for the adapter check vector.

B'00000000' or B'00110000' for the other TIC vectors.

NCP initializes the TIC interrupt vectors to

B'xx10xxxx' for SCB clear.

B'xx01xxxx' for adapter check.

B'xx00xxxx' or B'xx11xxxx' for the remainder.

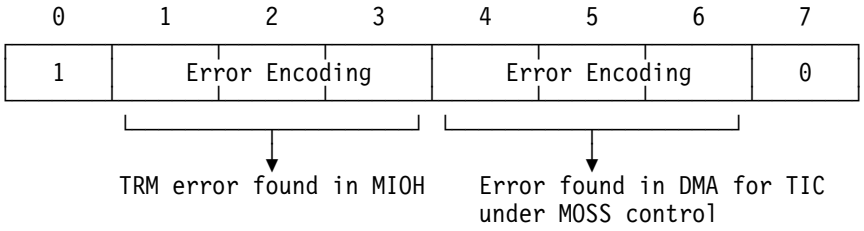
A format 1 entry will cause the type B line ID to be used.
A format 2 entry with bits 2 and 3 = B'10' or B'01' will also use the type B line ID.
All other cases use the type A line ID. (See “Line Identification (Line ID) Generation” on page 5-40 for type line ID definitions).

If the level 2 error status register contains a format 2 entry and the TRM detects an error that requires logging a format 1 entry, the TRM will overlay the format 2 entry. After the format 1 entry is read and reset, the interrupt vector will again be fetched from the TIC and the format 2 entry set in the register again.

MOSS Error Status Register

Format 1 is used for errors detected by TRM in MOSS PIO/MMIO operations or in direct memory access (DMA) operations (TIC to CCU storage).

TD Field Byte 0 (Byte 1 not Used)



Error encoding:

0 0 0 No error
0 0 1 TRM internal
0 1 0 TIC interconnection type 1
0 1 1 TIC interconnection type 2

Internal The TRM is suspected.

Type 1 The working TIC is suspected.

Type 2 All TICs are suspected.

The MOSS error status register is used to log errors associated with MOSS operations. If a MOSS control bit in the TIC control register is ON, all MMIO and DMA errors for that TIC will be logged in the MOSS error status register.

If the TRM is connected, all MIOH/MMIO errors will be logged in the MOSS error status register.

If the TRM is disconnected and the associated MOSS control bit is OFF, all MMIO and DMA errors for a TIC are logged in the normal level 2 error status register.

Format 2 is not used for the MOSS error status register.

TIC Adapter Check Register

The adapter check interrupt is generated when the TIC has encountered an unrecoverable hardware or microcode error. In this case the TIC is waiting for a reset. The reason for the TIC check is located in 8 bytes beginning at address X'05E0'. The TIC check status is defined as follows:

X'5E0' (TIC adapter storage)

Byte 0 and 1	Byte 2 and 3	Byte 4 and 5	Byte 6 and 7
Adapter check	Parameter 0	Parameter 1	Parameter 2

Each bit of the TIC adapter check gives the error type and the contents of parameters 0 to 2 give additional information. More details are given in the following table.

TIC Adapter Check Register Decoding Byte 0

Bit	Error Type	Error Description	Parameters 0-2 Contents
x...	MMIO parity error	Data parity error between CCU and TIC	Contents is ignored
.x..	DMA abort read	DMA read operation abort for time out or parity error or bus error	Parm 0=0000 time out error 0001 parity error 0002 bus error Parms 1–2 contain the failing CCU address plus or minus 6 bytes
..x.	DMA abort write	DMA write operation abort	Same as for DMA abort-read
...x	Illegal operation code	Illegal operation code detected	Parm 0 = TIC register 13 Parm 1 = TIC register 14 Parm 2 = TIC register 15
.... x...	Parity error	Local bus parity error detected by TIC processor	Same as for illegal OP code
.... .x..	Parity error external	Local bus parity error detected by TIC during operation with CCU	Same as for illegal OP code
.... ..x.	Parity error – IOC bus interf.	Local bus parity error detected by TIC during operation with CCU	Same as for illegal OP code
....x	Parity error (PH) (protocol handler)	Local bus parity error detected by TIC during operation with the protocol handler	Same as for illegal OP code

TIC Adapter Check Register Decoding Byte 1

Bit	Error Type	Error Description	Parameters 0-2 Contents
x...	Parity error receive	Local bus parity error detected by TIC during receive operation	Parm 0 = buffer address
.x..	Parity error transmit	Local bus parity error detected by TIC during transmit operation	Parm 0 = buffer address
..x.	Ring underrun	DMA underrun detected during ring transmit	Parms 0–2 are ignored
...x	Ring overrun	DMA overrun detected during receive operation	Parms 0–2 are ignored
.... x...	Invalid interrupt	Unrecognized error interrupt was generated	Parm 0 = TIC register 13 Parm 1 = TIC register 14 Parm 2 = TIC register 15
.... .x..	Invalid error interrupt	Unrecognized error interrupt was generated	Parm 0 = TIC register 13 Parm 1 = TIC register 14 Parm 2 = TIC register 15
.... ..x.	Invalid transmit operation	Unrecognized transmit operation request was generated	Parm 0 = TIC register 13 Parm 1 = TIC register 14 Parm 2 = TIC register 15
....x	Program check	TIC processor program check detected	Parm 0 = Abend code Parm 1 = Address location that detected the error

TRA Interaction with Control Program

TIC Initialization

The NCP token-ring interconnection function initializes a TIC as follows:

1. The NCP resets the TIC.
2. The NCP issues read interrupt until theTIC initialization is complete without any error.
3. The NCP loads the initialization parameters in the TIC (22 bytes).
4. The NCP writes X'9080' to the TIC interrupt register.
5. The NCP issues read interrupt register until the TIC initialization is complete without any error.

In order to begin normal operation, the NCP initiates communications by placing an open command in the system control block (SCB), and specifying the required parameters. When the open command status is set into the system status block (SSB) and the command status interrupt is received, the NCP issues a receive command so that the TIC can receive frames.

TIC Read Interrupt Register (Initialize)

Byte 0

Bit	Bit Name	Description
*	Adapter interrupt	Ignored
. * * * * * * *	Interrupt requests	Ignored

Byte 1

Bit	Bit Name	Description
0	Interrupt system	Always 0
. x	Initialize	Bit=1: Bring-up successful and TIC adapter ready for initialisation Bit=0: Initialization completed with or without error
. . x	Test bit	Bit=1: Bring-up diagnostics following hardware reset Bit=0: When initialize bit is set to 1
. . . x	Error bit	Bit=1 Error during bring-up diagnostic or initialization sequence Bits 4-7 specify the error condition
. . . . x x x x	Error code	During bring-up or initialization If test=1: Contain bring-up error code If test=0: Contain bring-up initialisation error code (See bits 4-7 decoding hereafter)

Bits 4-7 : Error Code During Bring-up With Test=1

Bit 4-7	Error Code Description
0 0 0 0	Initial test error
0 0 0 1	ROS CRC error
0 0 1 0	RAM error
0 0 1 1	Instruction test error
0 1 0 0	Transmit operation test error, interrupt test error
0 1 0 1	Protocol handler hardware error
0 1 1 0	IOC interconnection control register error

Bits 4-7 : Initialization Error Code With Test=0

Bit 4-7	Error Code Type	Description
0 0 0 1	Invalid parameter length	This code will be set if 22 bytes are not passed
0 0 1 0	Invalid options	
0 0 1 1	Invalid receive burst size	The receive burst size is odd
0 1 0 0	Invalid transmit burst size	The transmit burst size is odd
0 1 0 1	Invalid DMA abort thresholds	The bus error or parity error count is zero
0 1 1 0	Invalid SCB address	The SCB address is odd
0 1 1 1	Invalid SSB address	The SSB address is odd
1 0 0 0	MMIO parity error	TIC adapter detects a parity error during a system MMIO write operation
1 0 0 1	DMA time out	TIC adapter time out (10 seconds) waiting test DMA transfer complete
1 0 1 1	DMA parity error	TIC adapter detects bad parity from the CCU during DMA transfer tests
1 0 1 1	DMA bus error	The CCU asserts bus error during one of the test DMA transfers
1 1 0 0	DMA data error	The initialize DMA test fails due to a data compare error
1 1 0 1	Adapter check	The TIC adapter has encountered an unrecoverable hardware error (for details see page 5-53)

Problem Determination Aids

Token-Ring Wrap Tests

Using NCP

Under NCP a wrap test is performed at each TIC open command processing as a first step before inserting itself into the ring.

The TIC internal lobe media test, tests the ring up to and including le logic (relay contact normally closed) pertaining to the position of the IBM 8228 MSAU or equivalent where the lobe connector is plugged-in (the 8228 is a wiring concentrator).

It also tests the ring up to the point were it is unplugged before the 8228 (that is, at the tailgate, at the wall connector, and so on).

The lobe media test is only invoked on the open command and is not performed as a result of the reset or initialization commands.

Note that a disconnected cable during the lobe media test will cause a lobe wire fault check to appear in both the display token-ring status function and the ring status field (field E) of the token-ring interconnect function. (Refer to the *Problem Determination Guide*, GA33-0096.)

When a lobe wire fault is detected the TIC will be frozen and the status will remain unchanged until the next open is issued.

Using TRA Diagnostics

Using the TRA diagnostic routine TG01, a wrap test is also performed up to and including the 8228 or up to the point at which the ring is unplugged before the 8228. (See *3745 Diagnostic Descriptions*, SY33-2059 for more details). However, no open commands are issued by the diagnostic routine so a lobe wire fault will not be detected.

Diagnostic Section TA0A

The TRM must be 'disconnected' before running the diagnostic section TA0A. The 'disconnect' command must be performed after each power-OFF to power-ON.

Chapter 6. High Performance Transmission Subsystem (HPTSS)

HPTSS in 3745 Data Flow

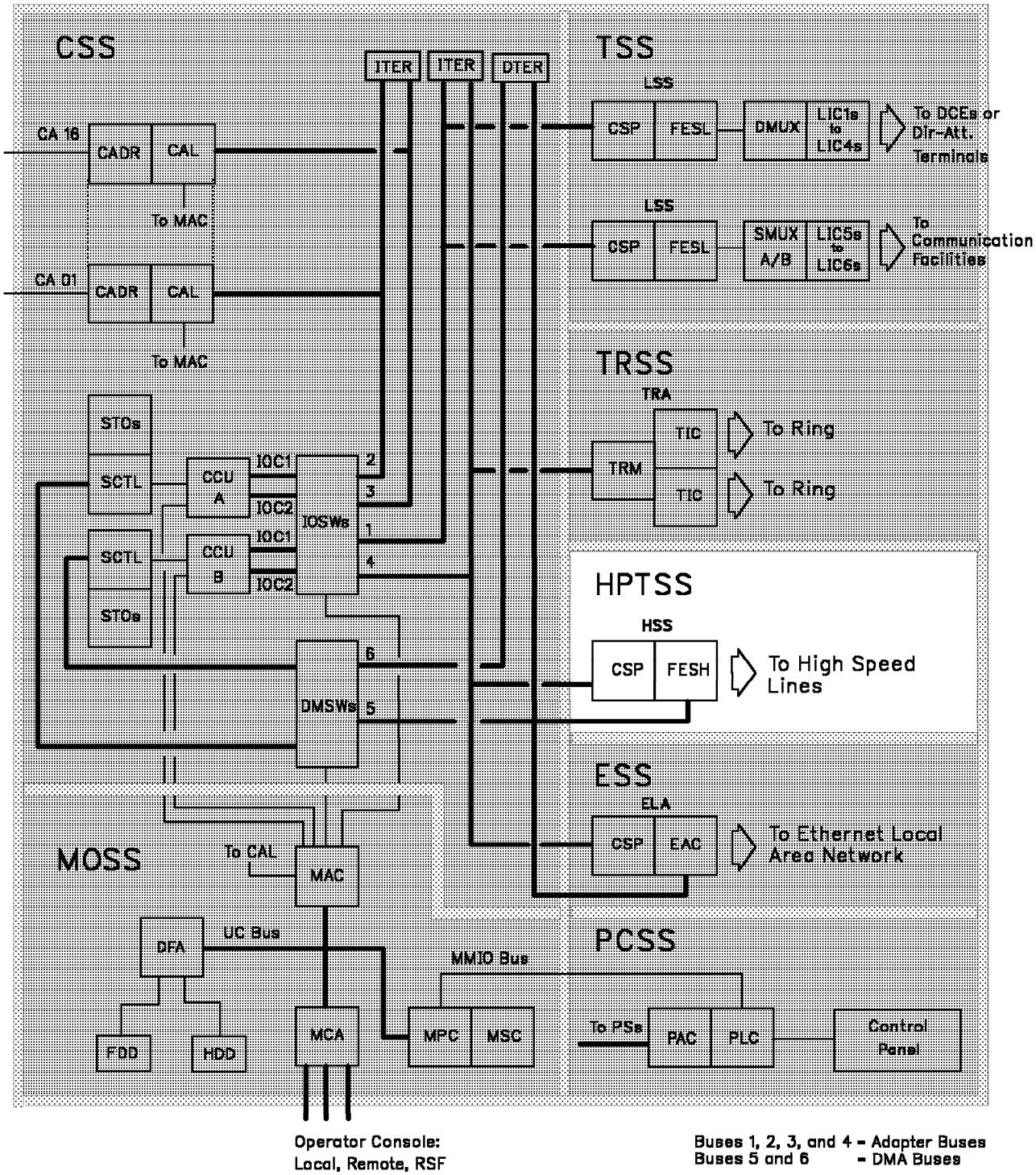


Figure 6-1. HPTSS in 3745 Data Flow. For models 21A-61A, DMA and IOC buses are connected to the CBC in the 3746-900. The MCA card is replaced by the MLA card which interfaces to the MPC card through the MMIO bus. This MLA card links the MOSS to the Service Processor through a LAN.

Introduction

The High Performance Transmission Subsystem (HPTSS) is a combination of one or several high-speed link scanners (HSSs) and NCP for the 3745.

The HSS is capable of clear channel, duplex, leased-line, HDLC/SDLC transmission using satellite, Transfix, and any other transmission link (fiber, direct attachment of 3745, 3725, and so on) requiring high-speed data transmission up to 2.048 Mbps. The HSS is also capable of operating with Frame Relay traffic. Included are modifications on the NCP/ESS interface to improve the transmit and receive command performance. This is referred to as the Frame Relay Performance Enhancement (FRPE).

This point-to-point non-switched connection can be attached to any network with the proper network adapter like data communication equipment (DCE) or network communication terminal equipment (NCTE).

The HSS operates with the Network Control Program (NCP) and is transparent to the SDLC data traffic.

System Environment

Since the HSS is transparent to the data, the NCTE or DCE must conform to the network standards. The HPTSS adapters (HSSs) can operate as secondary to the network clock connected to a network. When operating as a secondary, the HSS operates with any clock speed up to 2.048 Mbps.

The HSSs can also be directly connected back-to-back without a network.

When directly attached to each other, the adapters can operate at any one of the three speeds set by the NCP: 245.76 Kbps, 1.47456 Mbps or 1.8432 Mbps. The connection to a 3725 is limited to 245.76 kbps.

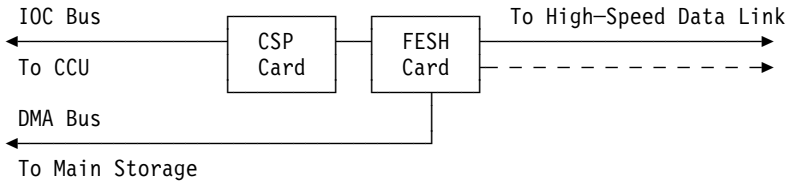
The HSS provides two separate V.35 or X.21 interfaces to a network.
However, only one V.35 or X.21 interface to the NCTE or DCE can be active and enabled at a time.

HSS Packaging

The handling and management of such a high-speed data link is achieved by two cards:

- One communication scanner processor packaged on one card, the CSP card identical to those of the low-speed scanner (LSS) but with a different CSP microcode load module (see “CSP Microcode Summary” on page 6-7).
- One high-speed front-end scanner packaged on one card, the FESH card.

For board and card locations, see the Chapter 5 of the "Maintenance Information Procedures", SY33-2054.



Up to eight HSSs (coupled CSP/FESH cards) may be installed on the line adapter board of the base frame, to control up to eight high-speed data links at one time.

On each FESH, a fan-out (standard feature) allows two high-speed data links to be connected at the tail gate to that FESH. But only one of them must be active at a time.

No line interface coupler card (LIC) needs to be installed as for the lines connected to the low-speed scanner (LSS).

Line Addressing

Each HSS supports a maximum of two line addresses. However, only one line at a time may be active in the control program and only one line can be defined using the LKP function.

With eight possible HSSs, the maximum number of lines is 16. Line numbers 1024 through 1039 are dedicated for HSS use.

The two lines associated with a particular HSS are addressed by the TD1 field of the IOH. TD1 bit 6 selects one of the two lines. TD1 bit 7 selects either the transmit or receive interface of a line. TD1 bit 7=0 selects the transmit interface and TD1 bit 7=1 selects the receive interface.

Refer to “HPTSS Line Addressing” on page 3-72 for the mapping of the lines between the boards and the tail gate.

HSS Commands

Commands are set in TD0 of the start line or start line initial instructions. The following NCP commands are supported by the HSS:

Commands	Codes (Hex)
Set mode	01
Enable	02
Disable	03
Change	06
Flush data	09
ResetD	0B
ResetN	0C
SDLC transmit control	10
SDLC transmit data	11
SDLC receive	13
SDLC receive continue	14
Trace	2C
Stop trace	2D
Halt	F0
Halt immediate	F1
Dump Control blocks (no status)	F4
Dump Control blocks (status)	F5

The following MOSS command is supported by the HSS:

Commands	Codes (Hex)
Wrap	2E

Interface or Port Types

Two types of line interface or port are available on the FESH card:
(Refer to “Communication Interfaces” on page 6-63 for more details)

1. V.35
2. X.21 leased (including French Transfix).

They allow the 3745 to be connected to:

- U.S. T1 type line
- European high-speed lines (CEPT lines)
- Satellites
- In-plant transmission link for direct-attached adapters.

HPTSS Data Flow

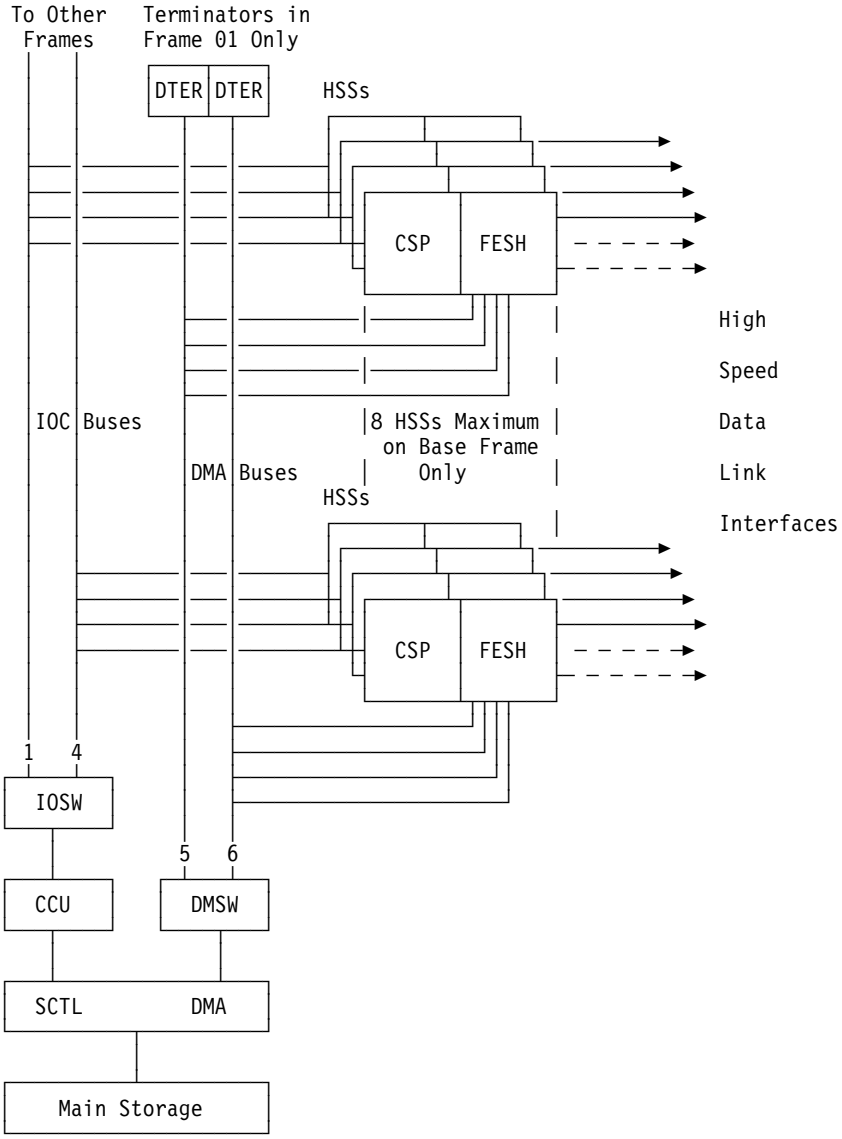


Figure 6-2. HPTSS Data Flow

CSP Microcode Summary

The HSS requires a different CSP microcode load module than the LSS to take advantage of the hardware buffer management for supporting speeds up to 2.048 Mbps.

Listed below are the main microcode functions supported by the HSS.

- Supported line speed: up to 2.048 Mbps
- Supported line interfaces or ports: V.35 and X.21 (called X.21 Transfix in France) leased line
- SDLC/HDLC duplex protocol on point-to-point leased line

  A network adapter may be required, such as DCE or network communication terminal equipment (NCTE).

- Echo suppression
- Frame up to 64 kbytes long (SNA maximum size)
- CSP ROS common with other microcode load modules
- SDLC address compare performed by FESH
- NCP buffer prefixes automatically handled by FESH via DMA bus (except for SIT buffers)
- The HSS transfer of data between adapter and NCP differs from the LSS:
  - When the LSS transfers data to the NCP buffers, via the IOC bus, it uses the cycle steal mechanism.
  - When the HSS transfers data to the NCP buffers, via the DMA bus, it uses the FESH hardware.
- One PIO per SDLC frame for transmit
- One or several PIOs per SDLC frame are possible for receive
- IOC cycle steal is used for command parameters and status, IML, dump, and SIT trace data.
- Frame Relay duplex protocol attached as a DTE to a Frame Relay network, or as part of the Frame Relay network as a DCE.
- Multiple Frame Relay frames with one transmit PIO.
- One PIO per received Frame Relay frame.
- Use of a SNAP header format table to place Frame Relay headers and data in the proper alignment for NCP in their receive buffers.

Main Differences with LSS

- Buffering of the receive and transmit frames is done in a FESH buffer instead of CSP storage.
- SDLC transmit continue command not supported.
- SDLC receive monitor command not supported.
- No multiplexing (only one line).
- HSS microcode deals with buffer prefixes only with scanner interface trace (SIT). The remaining buffer prefix handling is done by the FESH.
- CCU storage access for NCP buffer data is done through DMA instead of IOC cycle steals as in LSS.

However, IOC is still used for the following:

1. Dump, IML, diagnostics.
2. Sending status (followed by CCU level 2 interrupt) when FESH, DMA or SCTL error has to be reported.
3. Facilities (see “Problem Determination Aids” on page 6-60) invoked from the operator console (MOSS) to:
   a. Perform diagnostics.
   b. Access FESH registers and random access memory.
4. IOH transfer between NCP and CSP.
5. MOSS exchange with HSS.

Programming Notes

SDLC Address Compare

The primary SDLC address is indicated by the NCP in the receive SDLC command. The secondary station address is loaded with the set mode command.

The CSP microcode initializes the FESH by storing in registers X'0E' and X'0F' the address pattern to be compared. The broadcast address (X'FF') is always accepted by the FESH.

The CSP microcode initializes the FESH in order to activate the compare.

If there is an address mismatch, the incoming SDLC frames are flushed.

The SDLC extended address mode (2-byte address from SDLC transmit command) is indicated on each receive command.

The compare does not apply to frames already stored in the FESH receive buffer.

The NCP manages any starting, stopping or changing address related to SDLC address compare in the HSS.

Init Command

Before the NCP sends the set mode command, the MOSS sends to the CSP microcode all the configuration data.

The customer may change the configuration data online via the MOSS.

The values are changed in the HSS when the NCP issues the next init command.

Echo Suppression

Echo suppression is used in communication via satellite. It may also be used by other communication types (see "HSS Receive Operation" page 6-22).

The echo suppression is indicated by the NCP at set mode time.

For transmit operations and echo specified from the NCP:

- If primary, the CSP microcode forces transmitted address byte 0, bit 0 to 0.
- If secondary, the CSP microcode forces transmitted address byte 0, bit 0 to 1.

For receive operations and echo specified from the NCP:

- If primary, and received address transmitted byte 0 bit 0 is 1, the CSP resumes processing; otherwise, the FESH flushes the frame.
- If secondary, and received address byte 0 bit 0 is 0, the CSP resumes processing; otherwise, the FESH flushes the frame.

Miscellaneous

Additional parameters are received by the HSS microcode from the customer system generation parameters and also from the configuration data set from the MOSS.

These SYSGEN parameters are stored in the CSP and the FESH at IPL time.

The CDF parameters are stored in the FESH via the set mode command from the NCP system generation parameters and CDF parameters from MOSS.

The controller load dump program (CLDP) is also able to receive a 'write IPL' command for a remote load or dump.

Internal Interconnections

As shown in “HPTSS Data Flow” on page 6-7, each HSS interconnects with the communication subsystem (CSS) and the MOSS via the IOC bus and the DMA bus.

CSP-to-IOC Bus

This connection is used for:

- Communication with the NCP (through the same IOH high level commands as the other LSS scanners)
- MOSS command exchange
- HSS IML
- Diagnostics.

The physical interconnection between the HSS CSP and the CCU is identical to that between the LSS CSP to the CCU (refer to Chapter 4, "Transmission Subsystem").

For board and card locations, see the Chapter 5 of the *Maintenance Information Procedures Manual*, SY33-2054.

NCP-HSS Microcode

The CCU uses IOH and IOHI to exchange data, commands and statuses with the HSS CSP in the same way as with the LSS, but cycle steal is not used when the FESH is running.

CLDP-HSS Microcode

The controller load/dump program (CLDP) is used in a remote 3745 to interconnect the CCU and the HSS CSP microcode. The main functions performed are:

- IPL of the remote 3745
- Dump of the remote 3745

The CLDP never:

- Issues SDLC transmit continue or receive monitor commands
- Uses data areas, but NCP buffer pointers for both transmit and receive operations.

FESH to CSP

The physical interconnection between the FESH and the CSP is identical to that between the FESL and the CSP of the LSS.

For board and card locations, see the Chapter 5 of the *Maintenance Information Procedures Manual*, SY33-2054.

Microcode to FESH

The picocode is loaded from the CSP in each layer of the FESH RAM at IML time.

The FESH-to-CSP interconnection is activated and controlled via external registers and control words (CW).

A CW is built by the CSP microcode and specifies the actions to be performed by the FESH.

The CW is cycle stolen by FESH, then executed.
The FESH informs the CSP microcode when the action is completed.

Data Transmission

The CSP microcode can issue the following commands to the FESH:

- Start transmit initial
- Start transmit
- Soft stop transmit (For example; it causes the FESH to transmit the error sequence, which is a MOSS init parameter from the NCP)
- Hard stop transmit (For example; it forces the transmit data line to a mark level all ones).

Data Reception

The CSP microcode can issue the following commands to the FESH:

- Start receive
- Start receive continue
- Stop receive
- Flush the current frame.

Data and Modem Management

The CSP microcode can issue the following commands to the FESH:

- Start modem monitor
- Start modem-out
- Start data management

FESH to DMA Bus

This connection is used for direct CCU storage access and specifically:

- NCP buffer prefix exchange
- Data transfer between the high-speed line and main storage
- Parameters and status exchange between the NCP and the HSS microcode.

Communication Scanner Processor (CSP)

The HSS CSP hardware is identical to that of the LSS CSP (refer to Chapter 4, "Transmission Subsystem" for details).

Front End Scanner High-Speed (FESH)

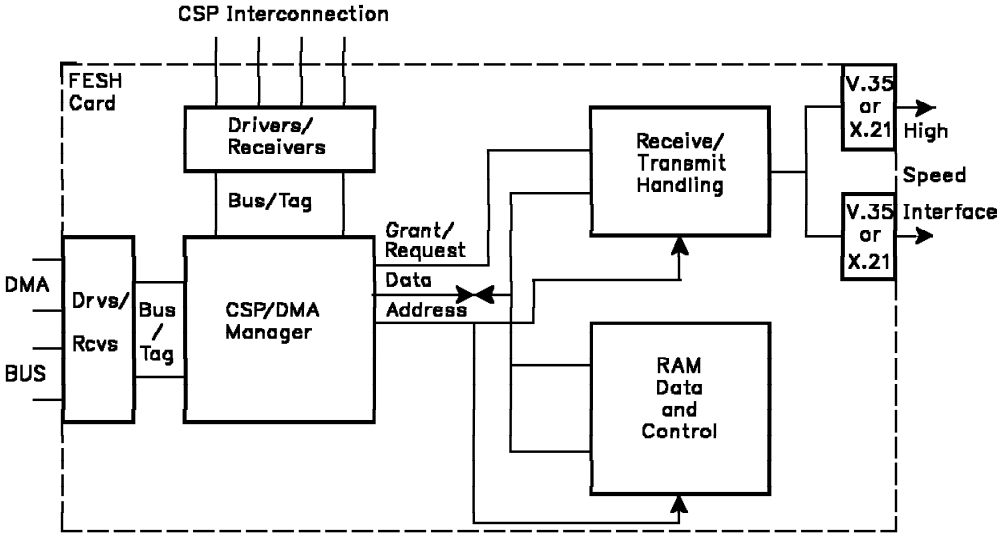


Figure 6-3. FESH Data Flow

The transmit/receive handling of the FESH is functionally organized in layers as follows:

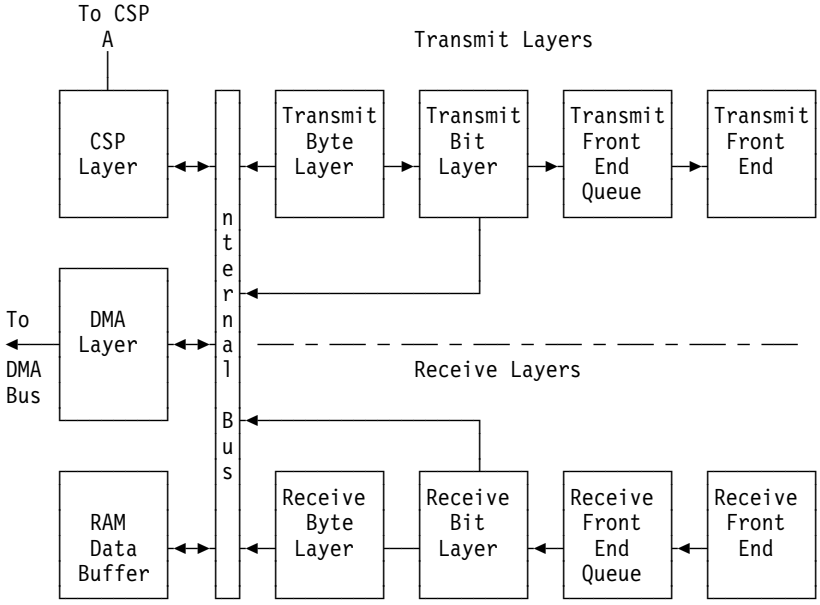


Figure 6-4. Transmit and Receive Layers

Transmit Layers

The transmit layers are composed of:

- The front-end circuits which perform the following functions:
  - Serialization of data
  - Flag generation
  - Zero insertion
  - CRC generation.
- The transmit bit layer which:
  - Handles byte transfer between transmit front-end buffers and the FESH RAM.
- The transmit byte layer which:
  - Handles NCP buffer prefixes for transmission.
  - Interconnects with the CSP layer (external registers and control words).
  - Handles chaining thru NCP buffers for SDLC transmits.
  - Handles chaining thru NCP buffers for each frame relay frame and chaining between frames to transmit.

Receive Layers

The receive layers are composed of:

- The front-end circuits which perform the following functions:
  - Deserialization of data
  - Zero deletion
  - Flag detection
  - Early flag detection
  - Abort detection
  - Idle detection
  - Overrun detection
  - CRC calculation error detection
  - Address compare/satellite echo suppression
  - Interconnection with receive queue buffer.
- Receive bit layer:
  - Handles byte transfer between receive front-end buffer and FESH RAM.
- Receive byte layer:
  - Handles NCP buffer prefixes for receive
  - Interconnects with CSP layer (external registers and control words).
  - Handles chaining thru NCP buffers for SDLC receives.
  - Handles chaining thru NCP buffers for frame relay frame receives. Also, use the SNAP header format table to determine the offset and maximum counts to use for the first two buffers in the receive chain for frame relay. Provide the actual count used in the receive buffer prefix.

Modem-Out Layer

The modem-out layer:

- Interconnects with the CSP layer control word (CW).
- Activates output modem control leads according to the modem-out CW prepared by the CSP microcode.

Modem-In Layer

The modem-in layer:

- Interconnects with the CSP layer (control word and external registers).
- Performs input modem control lead status confirmation.
- Reports input modem control lead changes and X.21 steady states according to the modem-in CW prepared by the microcode and stored in the FESH RAM.

DMA Manager Layer

The DMA manager layer:

- Interconnects on one side with:
  - FESH RAM
  - Data management buffer
- Interconnects on the other side with the DMA bus.
- Handles the DMA bus protocol.
- Performs data transfer from/to CCU main storage, to/from transmit/receive/data management buffers.
- Handles priorities of DMA bus requests from transmit/receive data management layers.

CSP Layer

The CSP layer:

- Interconnects on one side with the CSP storage and microcode.
- Interconnects on the other side with the various FESH layers via CSP external registers and cycle steal operations.
- Handles the protocols of CSP external registers and cycle steal operations.
- Handles cycle steal requests from transmit/receive/data management/modem-in/out layers on a priority basis.

Scanner Status After the IML

At the end of scanner IML it is possible to get from the CCU storage, the status of the scanners associated with their mailbox.

The 16-byte mailboxes are located from CCU storage address 3F8000 (for 4MB storage) or 7F8000 (for 8MB storage).

The status of the scanners just IMLed are in the last two bytes of the mailbox. These values must be displayed before any mailbox exchange between the CCU storage and the corresponding scanner (for example: CCU functions). Below are the possible statuses of the scanner after an IML:

Values	Description
X'nnFF'	No answer from scanner following the MOSS command 'nn'
X'C900'	Normal status IML OK
X'C901'	FESH picocode failed
X'C902'	FESH card and picocode level not compatible
X'C904'	FESH card not installed

Figure 6-5. Values of the Last Two Bytes of the Mailboxes after IML

Reset FESH

All latches are reset, the DMA and modem interfaces are disabled, the card is kept in 'freeze mode' (FESH not operational) until the CSP loads the microcode in those storage locations which are not reset.

NCP-to-CSP Command Flow

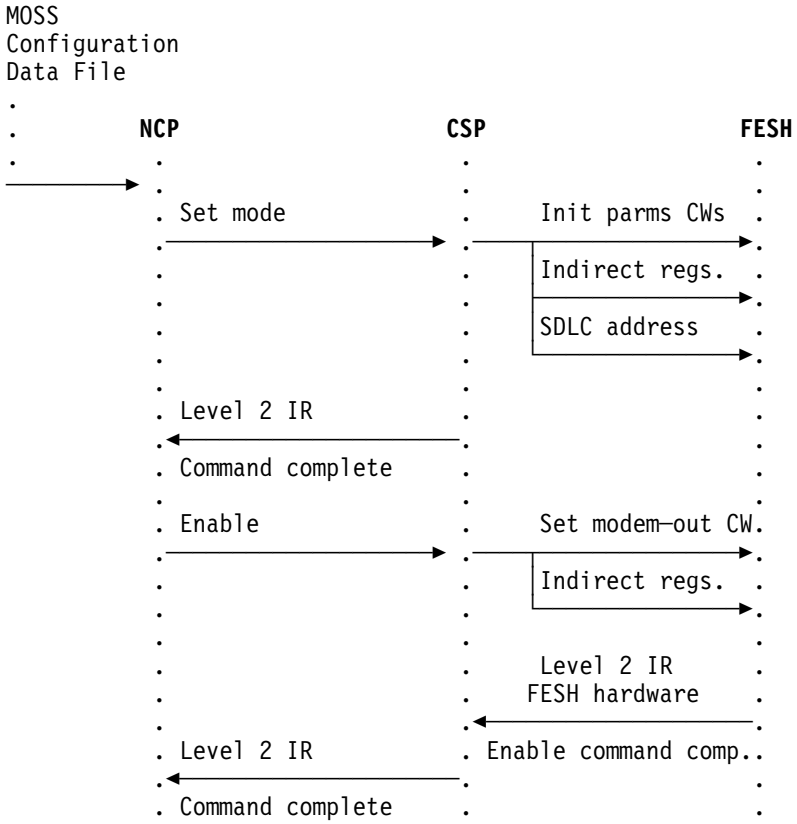
The following shows the general command flow between the NCP and the HSS (CSP + FESH). These diagrams are the main line paths of command execution in the HSS. Exception and error conditions are not covered.

The supported NCP commands are listed in “HSS Commands” on page 6-6.

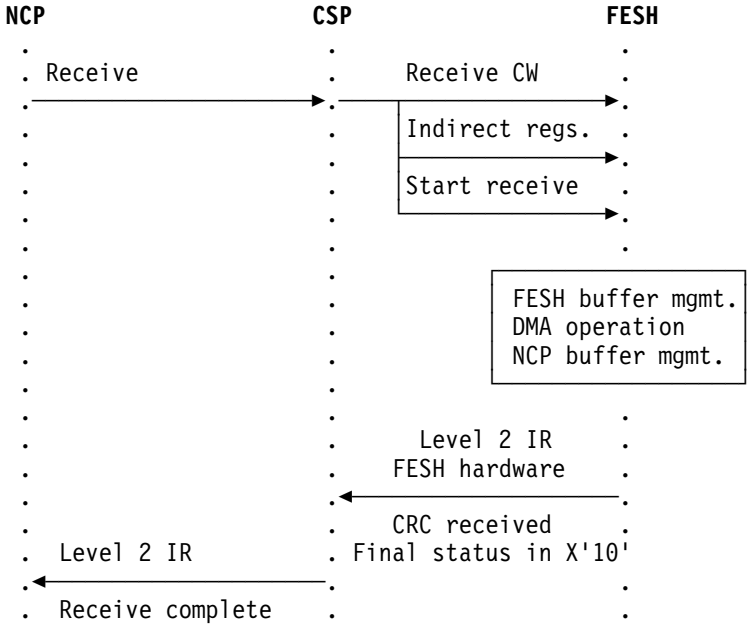
The following NCP commands are not supported by the HSS:

- SDLC receive monitor
- Transmit continue.

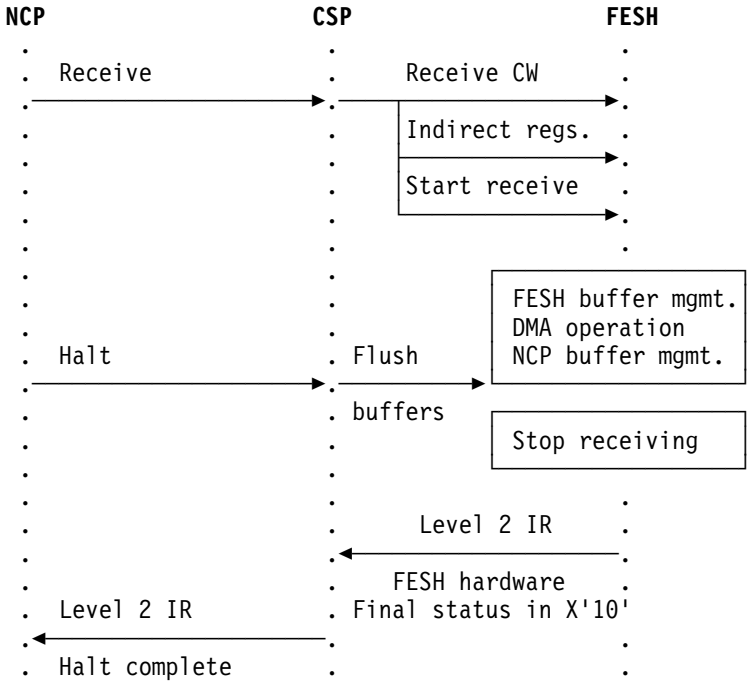
Set Mode/Enable Commands



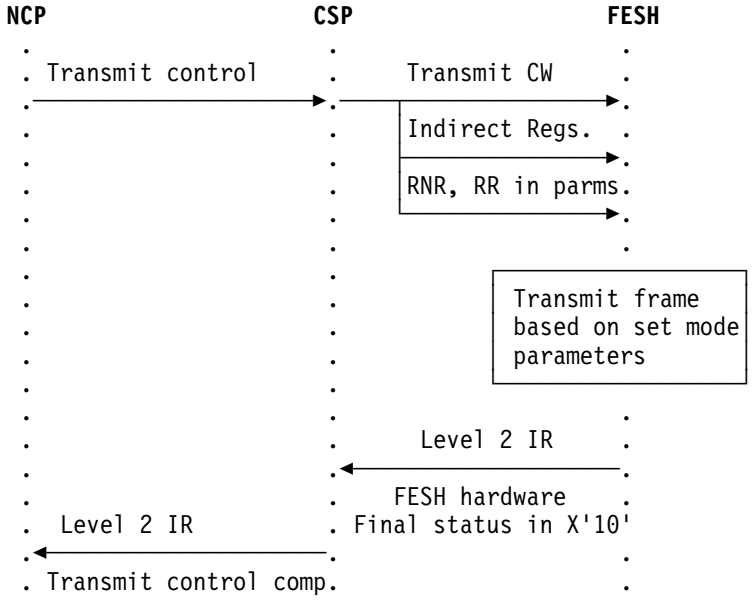
Receive Command



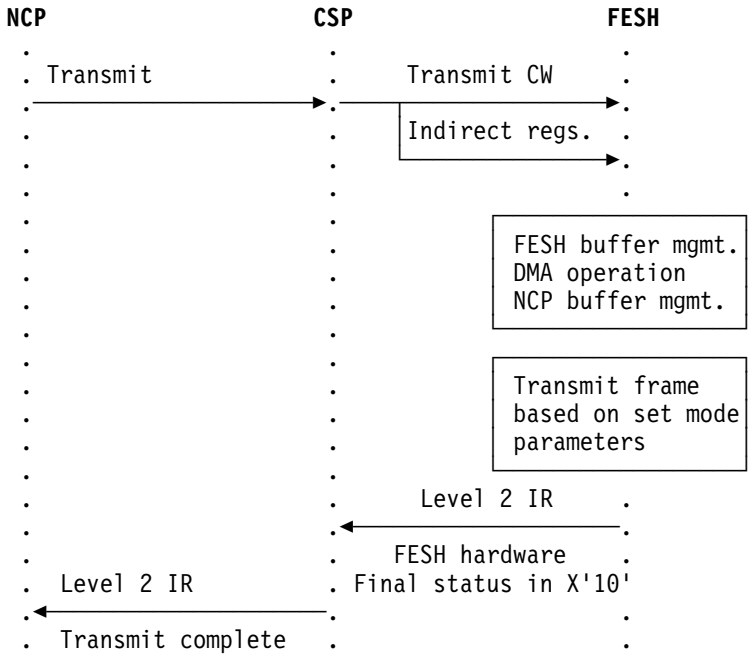
Halt Command



Transmit Control Command



Transmit Command



Transmit Operation

Microcode Functions

The microcode:

- Handles NCP transmit commands through PIO operations on the IOC bus.
- Gets transmit parameters and sends transmit status from/to the NCP via the DMA bus.
- Builds the transmit control word (CW) to be sent to the FESH.
- Indicates to the FESH transmit layer (external register setting) the:
  - Transmission coding mode (NRZI or non-NRZI) at set mode
  - Start of transmit initial
  - Start of transmit
  - Stop of transmit operation (hard and soft).

FESH Hardware Functions

Transmit Initial Command

The transmit initial command is used between the CSP and FESH hardware to perform a wrap test on the X.21 interface. The NCP issues a wrap command to the FESH with modifier bits indicating the type of wrap to be performed.

Then, the CSP issues the transmit initial command with the loop bit ON to the FESH, to support X.21 network testing, or to send a data pattern other than flags between SDLC frames.

On reception of a start transmit initial command from the microcode, according to a control bit (loop bit), the FESH sends in 'non-zero insert mode' to the transmit line:

- Loop bit OFF:
  - An initial character sequence (7 characters maximum) prepared by the microcode at initialization time.
  - Then, the SDLC frame with the receipt of the transmit command (see hereafter the "Transmit Command" paragraph).
- Loop bit ON:
  - The initial character sequence (7 characters maximum)
  - Then sends *the last two characters of the sequence continuously* until the microcode sets the start transmit command or the stop transmit command (used by the X.21 wrap command from the CSP to the FESH).

Transmit Command

On reception of a start transmit command, the FESH transmit layer cycle steals the transmit control word prepared by the microcode in CSP storage.

When the control word is loaded, the transmit byte layer:

- For SDLC, cycle steals the address or command (A/C) fields prepared by the microcode in CSP storage.

- If the SDLC frame contains A/C fields only, the transmit byte layer starts the transmission.
- If the SDLC frame contains an I-field, the FESH begins a DMA operation to load the I-field from the CCU storage to the FESH RAM via the DMA bus.
- For frame relay, begin a DMA operation to load the transmit data from the CCU storage to the FESH RAM via the DMA bus.

Note: The maximum size of an A/C field is four bytes.

The bit layer machine and the byte layer machine operations are overlapped so that the transmission of data can continue while data is being obtained from the CCU via the DMA interconnection.

This overlap of operations continues until a zero buffer pointer is detected.

- When a zero buffer pointer is detected the bit layer instructs the front-end to send the CRC and ending flag, followed by the ending sequence specified at set mode (line at mark or continuous flags).
- If frame relay, look for another frame to transmit. If there is one, continue as if starting a new frame. Continue as in the previous bullet until all frames are transmitted.
- The byte layer also sets the end of transmit bit in the transmit status register and generates a level 2 interrupt to the CSP.

During the transmission over the line, the hardware may detect that no data has been loaded in the external RAM whereas the FESH bit layer requests a new buffer (DMA transfer up to the buffer count not completed), in that case the hardware:

- Sets the underrun and the end transmit bits in the transmit status register.
- Raises a level 2 interrupt to the CSP.
- Sends the transmission error sequence initialized at set mode.

Soft Stop Transmit Command

On reception of this command, the hardware:

- Stops transmitting the data.
- Stops any transmit DMA transfer in process.
- Sends the transmission error sequence initialized at set mode.

Hard Stop Transmit Command

On reception of this command, the hardware:

- Stops transmitting data.
- Stops any transmit DMA transfer in process.
- Puts the line at mark.

Receive Operation

Microcode Functions

The microcode:

- Handles NCP receive commands through PIO operations on the IOC bus.
- Gets receive parameters from the NCP.
- Sends receive status from/to the NCP through data management exchanges on the DMA bus.
- Prepares the receive control word (CW) for the FESH:
  - The CSP cycle steals the storage address of the received SDLC frame address/control fields.
  - If a non-I frame is to be transmitted, the number of bytes of the address or command (A/C) field is indicated (4 bytes maximum).
- Indicates to the FESH (external register setting) the:
  - Transmission coding mode (NRZI or non-NRZI) at set mode
  - Start of receive command
  - Receive continue command
  - Stop of receive operation command
  - Flush command.

FESH Hardware Functions

Receive Command

When the FESH is enabled it always:

- Monitors for flag (flush other characters).
- Performs address compare.
- On flag recognition, starts accumulating received characters in the receive queue buffer.
- Performs zero deletion.
- Performs CRC accumulation (The two CRC characters are not stored in the receive queue buffer).
- On flag recognition, checks the CRC.
- Stores the receive ending conditions in the receive queue buffer and then in external register X'10' for the microcode:
  - End of receive CRC OK
  - End of receive CRC bad
  - Flag OFF boundary
  - Abort (not followed by idle)
  - Idle
  - Overrun.
- Accumulates multiple frames in the receive buffer queue.
- If receive queue full:
  - Indicates overrun as ending condition in receive queue.
  - Flushes further incoming characters of the frame on which the overrun occurred.
  - Ignores subsequent data and flags until the CSP issues a receive command.

Receive Flow

On reception of a receive command from the microcode, the FESH receive layer:

- Cycle steals the receive control word (CW) prepared by the microcode in CSP storage.

When the CW fetch is completed, the receive byte layer:

- Cycle steals the A/C field into CSP storage starting at the address specified in the receive CW.

If the ending condition is reached (no I-frame) the byte layer:

- Generates a level 2 interrupt to the CSP.

If no ending condition is detected in the receive queue (I field), the following operations are performed.

Receive Operation For I-Frame:

The receive operations are overlapped so DMA operations are done in parallel with the extraction of the data characters from the transmission line.

The process is continued until the ending condition is detected.

End of Receive:

When an ending condition is detected in the receive queue, the byte layer sends the address of the last NCP buffer used, the residual byte count of the last buffer, in the CSP storage, and generates a level 2 interrupt to the CSP.

Receive Continue Command (SDLC only)

During the receive flow, the byte layer detects the end of message:

- Stops reading characters from the receive queue, but the FESH continues receiving characters from the line.
- Raises an interrupt to the CSP and indicates to the microcode that a new buffer pool is needed.
- Waits for start receive continue from the microcode.
- On reception of start receive continue from the microcode, the hardware resumes the normal process.

Flush End of Frame Command

When receiving I-frames to be flushed, a 'frame reject' frame (FRMR) can be received and must not be flushed. For this purpose, the NCP issues a receive command to get the A/C field of the received frame.

In that case the FESH performs an action similar to the receive continue process and:

- Stops reading characters from the receive queue after having sent the A/C fields into CSP storage.
- Raises a level 2 interrupt to the CSP and indicates to the microcode that a new buffer pool is requested.

- Waits for start receive continue from the microcode in case of FRMR frame, or for a flush end of frame command.

Flush Command

On reception of this command, the hardware reads and flushes the remaining data characters of the frame out of the receive queue, until an ending condition is reached. This ending condition is reported to the microcode.

Stop Receive Command

On reception of the stop receive command from the microcode, the hardware clears out the contents of the receive queue buffer.

Modem Interface Management

Modem-In Management

To manage the DCE input leads, the microcode:

- Prepares a CW in CSP storage.
- Starts the process by sending the start modem monitoring command to the FESH.

The modem-in layer monitors the modem input leads.

On a modem control lead change, according to the CW, and after possible lead state confirmation, the modem-in layer interrupts the microcode (level 2 interrupt) which can then get the modem input lead status at the time of the change.

After a modem change has been reported to the microcode, the hardware does not report a new change until the microcode sends a new modem-in monitoring command.

Confirmation parameters are defined in the configuration data file and are loaded in the FESH at initialization time.

V.35 Modem-In Lead State Confirmation

On V.35 lines, the FESH is capable of monitoring:

- Data set ready (DSR)
- Clear to send (CTS)

However, in normal operation, the CSP microcode only monitors the DSR and CTS leads.

The FESH modem-in layer starts a count before delivering the new modem-in value to the CSP, in order to avoid unwanted interrupts caused by modem-in leads bouncing, or specific DCE behavior.

The confirmation delay is adjustable by the customer, through the CDF function, to adapt to the DCE characteristics.

DSR Confirmation:

Confirmation is performed on DSR going ON and OFF.

The confirmation delay is specified for each signal in a 3-bit parameter field loaded by the microcode. A specific timer starts each time the associated signal switches. The change is confirmed when the timer elapses.

Parameter Value	Confirmation Delay
0 0 0	No delay
0 0 1	1 ms
0 1 0	4 ms
0 1 1	16 ms
1 0 0	32 ms
1 0 1	64 ms
1 1 0	128 ms
1 1 1	256 ms

Note that the actual confirmation delays can be greater than the above values due to the fact that the timers restart at each signal change.

CTS State Confirmation:

The CTS state confirmation is set in indirect register X'09'.

The transmit clock and the transmit data requests made to the bit layer are gated by CTS in the FESH, in order to perform data transmission only when CTS is ON (refer to “Modem-Out Management” on page 6-27 and “Modem Retrain” on page 6-27 for explanation). However, this gating can be disabled by the microcode.

CTS drop reporting can be controlled by the microcode.

One timer step value is available:

- 400 ms step

If the timer value is zero (default value), CTS drop is reported without delay.

If this value is not zero, the hardware handles CTS drop according to the timer value. If the timer expires (25.2 s maximum) before CTS drops, a modem-in change is reported.

X.21 Modem-In Lead State Confirmation

In X.21, the modem-in microcode layer immediately reports to the microcode any change of the X.21 steady states and performs, in parallel, the confirmation of the following steady states which are detected by the FESH hardware:

	I	R
Clear	OFF	0
Controlled Not Ready (CNR)	OFF	0/1 (16-bit time)
Controlled Ready (CR)	OFF	1
Ready for Data (RD)	ON	X (don't care)
Local Wrap (LW)	OFF	X'0F' data received (16-bit time)
Remote Wrap (RW)	OFF	X'33' data received (16-bit time)

To confirm any state, the hardware verifies that the state remains unchanged during a count of 16-bit times.

When a state is confirmed, a modem-in change is reported to the microcode with the indication steady state ON.

DCE Clock Failure

The hardware monitors the receive and transmit DCE clocks of each line to detect clock failures.

If one or both DCE clocks disappear during a period of time exceeding 2.5 s, the FESH reports a clock failure to the microcode in indirect register X'11' (no level 2 interrupt is sent to the CSP).

Modem-Out Management

To manage the DCE output leads, the microcode prepares a CW in CSP storage and starts the process by setting the send modem-out command to the FESH.

On reception of this command, the hardware activates the output leads according to the contents of the CW.

The microcode can, at any time, read the modem-out lead register which contains the output leads activated by the hardware.

Modem Retrain

The term 'modem retrain' is used here to mean the temporary inability of a modem to respond to requests from the attached business machine (DTE). On V.35 lines, this typically occurs when two modems lose carrier synchronization. While 'retraining' the carrier, they are unable to provide service.

On X.21 lines, a 'retrain' means that the network or DTE places the line under test and during this time, the line is unable to provide service.

V.35 Modem Retrain

'Modem retrain' is detected on V.35 lines as a drop of clear to send (CTS). When this occurs:

1. The FESH starts a timer derived from the set mode enable time out value.
2. The FESH continues any transmission until the end of message is reached.
3. If a transmission is in progress when CTS drops, and the retrain timer has not expired, the following ending status is sent to the CCU when the transmission completes:
   - SCF = X'22' (underrun/data transmitted)
   - SCF = X'20' (underrun)
   - SES = X'80' (modem retrain)
   - LCS = X'00'
4. If CTS does not recover, and the retrain timer expires while a transmission is in progress, the ending status sent to the CCU is:
   - SCF bit 3 = 1 (modem check)
   - LCS = X'E2' (CTS dropped)

   If CTS does not recover, but there is no transmision in progress, the error will be detected and reported on the next transmit command as:
   - SCF bit 3 = 1 (modem check)
   - LCS = X'F2' (CTS failed to come up)
5. Data reception is not affected.

X.21 Modem Retrain

On X.21 lines, modem retrain is entered when a DCE uncontrolled not ready or DCE controlled not ready steady state is detected. When this occurs:

1. The CSP microcode starts a 20 second timer.
2. The FESH continues any transmission until the end of message is reached.
3. If a transmission is in progress when the retrain starts, the following ending status is sent to the CCU when the transmission completes:
   - SCF = X'22' (underrun/data transmitted)
   - SCF = X'20' (underrun)
   - SES = X'80' (modem retrain)
   - LCS = X'00'
4. If data reception is in progress when the retrain starts, the incoming frame is flushed (to avoid filling the NCP buffers) and the receive command is ended with the following status:
   - SCF = X'04' (end of message)
   - SES = X'10' (data check)
   - LCS = X'00'
5. If the DCE does not return to a 'ready' or 'ready for data transfer' state before the time out expires, the following ending status is sent to the CCU:
   - SCF bit 3 = 1 (modem check)
   - LCS = X'EE'

Time-Out Values

The following is a list of the various timer values used by the HSS along with their sources:

Enable time out Taken from the set mode data, it is used during enable command execution and also during transmit command execution (to monitor CTS, if it is down).

Disable time out Taken from the set mode data, it is used during disable command execution to allow the modem, time to respond to the changes on the modem-out leads.

Reply time out Taken from the set mode data, it is used during receive command execution to monitor for a reply to a transmission.

DSR confirmation A MOSS init value, it confirms a steady state on DSR for the stated period.

X.21 modem retrain A fixed 20-second value.

V.35 modem retrain The enable time out value is used if it is less than or equal to 25.2 seconds. A retrain timer of 25.2 seconds is forced if the enable time out exceeds this value. If the enable time out is not a multiple of 400 ms, the modem retrain timer is rounded to the next 400 ms increment.
See examples next:

Enable Time out	Resulting Retrain Value
0 ms	0 ms
100 ms	400 ms
400 ms	400 ms
25.2 s	25.2 s
40 s	25.2 s

Customization Parameters

Using the CDF Display/Update option 1 at the MOSS console, the CE or the customer can have access to the HSS parameters. The CE or the customer can choose two parameters: the DMA burst size (see the note 3 hereunder) and the DSR integration timer.

The DMA burst size is function of the number of HSS line adapters installed (see note 3 hereunder). A DMA burst size of 64 is correct. Other acceptable values should be between 64 and 240.

DMA burst (see note 3 hereunder) size values should be always multiple of 16.

Any value below 64 may increase the risk of overrun.

The DSR integration timer is a function of the manufacturer's equipment attached to the network. Normally 16 ms is adequate.
However, the CE or the customer must read the manufacturer's installation guide to determine if 16 ms can be used.

The following parameters are default values for the HSS port:

- DMA burst size (see note hereunder) (multiple of 16 values only): 64
- Error sequence: 7FFF
- DSR integration timer (0, 1, 4, 16, 32, 64, 128, 256): 16

Notes:

1. The DMA burst size and error sequence are valid for attachment to the X.21 or V.35 interface for the SDLC protocol.
2. The integration timers are valid only for the V.35 interface.
3. DMA size (length of burst). Depending on the 3745 microcode level, this field may no longer be displayed and modifiable. Its default values are set as follows:

   64 for receive operations
   253 for transmit operations.
4. For frame relay, the DMA burst size parameter is not used. The DMA burst size used by the FESH is dependent on the NCP buffer size.

Microcode Interaction with Control Program

This section describes the software interconnection between the network control program (NCP), which resides in the 3745 central control unit (CCU) and the HSS microcode residing in the communication scanner processor (CSP).

NCP-to-CSP Interconnection Description

The program interconnection provides a control path between the NCP and the CSP. The interconnection uses only programmed output instructions and programmed input (PIO) instructions during normal operation.

The interconnection is composed of the following functional components:

1. The NCP parameter/status area (PSA) to store the CSP control and status information.
2. Two programmed output instructions: set line vector table high and set line vector table low to tell the scanner the location of the line vector table (LNVT) in CCU storage.
3. Two programmed output instructions: set special line vector table high and set special line vector table low to tell the scanner the location of the trace line vector table (TLNVT) in CCU storage.
4. A programmed output instruction: start line initial to set or modify the parameter/status area address, and to initiate a command sequence.
5. A programmed output instruction: start line to initiate command sequences without modifying the parameter-status area address.
6. A programmed input instruction: fast get line ID to initiate auto-selection of a CSP and to get line identification data when servicing CSP interrupts.
7. A programmed input instruction: get error status to get information about a CSP program or hardware check.
8. A programmed input instruction: get command reject status to get additional information about a command reject status.
9. A programmed input instruction: get microcode check to get additional information about microcode-detected errors.

Parameter/Status Area

The control program residing in the CCU (NCP) provides a fixed-length field of CCU storage for each line interface serviced by high-level commands.

The parameter/status area is a field reserved in CCU storage by the NCP.

It is used to transfer the control and status information between the control program in the CCU and the CSP.

Information is transferred using direct memory access (DMA) or cycle steal under control of the CSP.

The parameter/status area is made up of:

1. A parameter area (16 bytes long)
2. A status area (12 bytes long).

The parameter area is used to pass to the CSP, parameters required in the execution of a command.

The status area is used to pass ending status to the control program in the CCU.

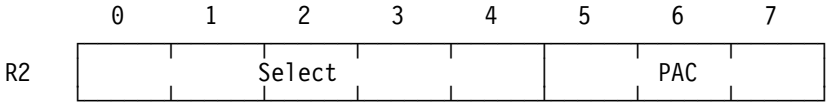
Upon receipt of a start line or start line initial instruction, the CSP gets information from the parameter area, executes the command, puts ending status into the status area, and requests a CCU level 2 interrupt.

Refer to “Parameter/Status Area Layout” on page 6-34 and “Miscellaneous Status Fields” on page 4-191, for field description.

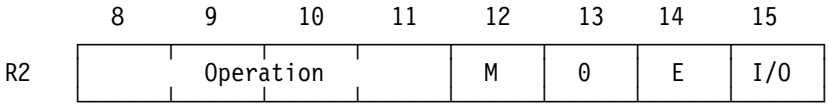
Input/Output Instruction Formats

The CCU communicates with the CSP via input/output halfword (IOH) or input/output halfword immediate (IOHI) instructions sent on the IOC bus at TA time.

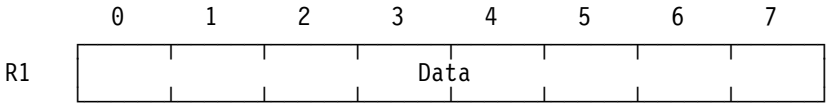
TA Field Byte 0



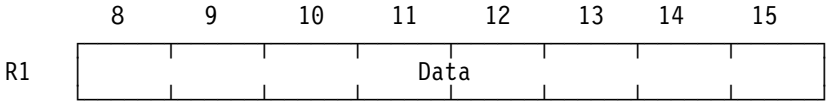
TA Field Byte 1



TD Field Byte 0



TD Field Byte 1



I is the 16-bit immediate data field of the IOHI instruction.

TD fields:

The contents of these two bytes depend on the instruction (as indicated in the operation field of TA1). For example, if the operation is start line or start line initial, TD byte 0 is the command to be performed (set mode, SDLC transmit, and so on) by the scanner, and TD1 contains the line interface address. Refer to the description of each operation for a definition of the TD fields.

IOH/IOHI Instruction (from NCP/EP) Summary

IOH/IOHI Byte 1[1]	Instruction
00	Start line
01	Fast Get line ID
10	Start line initial
11	Get error status
20	Set line vector table high
21	Get command reject status
30	Set line vector table low
31	Get microcode check
50	Set special line vector table high
60	Set special line vector table low
F2	Automatic dump

Start Line

The start line (TA byte 1=X'00') is issued to the CSP when a new command is to be started and the location of the parameter/status area has already been established.

Fast Get Line ID

The fast get line ID (TA byte 1=X'01') is issued to all CSPs (select bits 2 and 3 are ON to indicate a 'broadcast address') when servicing a CCU level 2 interrupt.

Start Line Initial

The start line initial (TA byte 1=X'10') is issued to the CSP when a line operation is to be started and it is necessary to establish the location of the parameter/status area.

Get Error Status

The get error status (TA byte 1=X'11') is issued to the CSP in response to a CCU level 1 interrupt request. This interrupt indicates a CSP program or hardware error.

Set Line Vector Table High

Set line vector table high (TA byte 1=X'20') indicates to the CSP its entry into the line vector table (LNVT) in CCU storage. More specifically, the NCP passes the high byte LNVT address for the first interface supported by a given CSP.

Get Command Reject Status

Get command reject status (TA byte 1=X'21') is issued to the CSP after the CCU has received a command reject error status to gather more information about the command reject.

The CSP responds with a two-byte status which identifies the command in process followed by the command that overlapped it. There is no default value for TD.

[1] IOH: byte 1
IOHI: byte 1 of second halfword

Set Line Vector Table Low

Set line vector table low (TA byte 1=X'30') indicates to the CSP its entry into the line vector table (LNVT) in CCU storage. More specifically, the NCP passes the low halfword LNVT address for the first interface supported by a given CSP.

Get Microcode Check

Get Microcode Check (TA byte 1=X'31') is issued to the CSP after the CCU has received a type 3 error status with bit 4 set (microcode check) to get information about the microcode check.

The CSP responds with a two-byte field containing the identification of the checker in the second byte. The following is a list of the HSS microcode checks that can be returned:

Status	Meaning
0001	Double queuing of an ICB pointer
0003	Fast get line ID not active
0008	Branch to X'8000'
000A	Branch to X'A000'
000B	Branch to X'B000'
000C	Branch to X'C000'

Set Special Line Vector Table High

Set special line vector table high byte (TA byte 1=X'50') is used to modify the location of the special line vector table (SLNVT).

Set Special Line Vector Table Low

Set special line vector table low halfword (TA byte 1=X'60') is used to modify the location of the special line vector table (SLNVT).

Automatic Dump

Automatic dump (TA byte 1=X'F2') is used to cause a scanner dump.
As a result of this instruction, the HSS sets a CCU level 1 interrupt and returns a status that causes NCP to request a scanner dump from MOSS.

IOH/IOHI Instruction (from MOSS) Summary

IOH/IOHI Byte 1[2]	Instruction
08	Start MOSS
09	Get command completion
18	Run JIB checkout
19	Get error status
28	Set MOSS area high
29	Get JIB checkout results
38	Set MOSS area low
39	Get scanner status
48	Reset

[2] IOH: byte 1
IOHI: byte 1 of second halfword

CSP Addressing

The CSPs associated with the possible eight HSSs installed in a 3745 are assigned the addresses of the first eight line adapters (LA) on the LA board 1 (TSSB board).

These addresses are used in the input and output instructions to select individual HSS adapters. In addition, all CSPs respond to a general broadcast address which is used in the fast get line ID instruction during auto-selection.

Parameter/Status Area Layout

The configuration of the parameter/status area differs from command to command. However, the fields which appear in multiple commands are always found in the same PSA location.

In addition, certain field and bit definitions are described, but are not used by the HSS. These items are used by the 3745 low-speed transmission subsystem adapter (LSS) and are included for completeness, since the two adapters use the same NCP interconnection.

A layout of an HSS PSA follows.

Trace Correlation Counter	Modifiers	0
Offset 1	Offset 2	1
Buffer 1 Count		2
First Buffer Pointer 1		3
Xmit/Rcve A–field 1	Xmit/Rcve A–field 2 or C–field	4
Xmit C–field 1	Xmit C–field 2	5
Buffer 2 Count		6
First Buffer Pointer 2		7
SCF	CCMD	8
SES	LCS	9
Residual Count / ELCS	FRPE Mode (Set Mode) Last Buffer Pointer	A
Last Buffer Pointer		B
Rcve A–field 1	Rcve A–field 2 or C–field	C
Rcve C–field 1	Rcve C–field 2	D
		E
		F

Figure 6-6. General HSS PSA Layout

Status Control Field (SCF)
This byte contains information which describes the progress of the operation being executed.

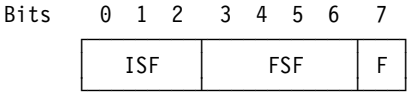
Refer to “Status Control Field (SCF) Bit Definition” on page 4-191 for bit description.

Current Command (CCMD)
This byte identifies the CSP command to which this status applies.

Secondary Status (SES)
This byte identifies errors encountered during execution of the command. When any bit in this byte is ON the service request bit (bit 1) in the SCF must be OFF.

Refer to “Secondary Status Field (SES) Bit Definition” on page 4-191 for bit description.

Line Communication Status (LCS)
This byte contains status applicable to the line being serviced. The byte is divided into three fields as shown below:



ISF = Initial status field
FSF = Final status field
F = Leading graphics / time out during X.21 clear

Refer to “Initial Status Field (ISF) Bit Definition” on page 4-192 and “Final Status Field (FSF)” on page 4-193 for initial and final status bit definitions.

Residual Count
This byte indicates the number of unused bytes remaining in the last buffer used.

Last Buffer Pointer
This three-byte address points to the last buffer used during receive operations.

SDLC Receive Address 1
This byte contains the first byte of the SDLC station address received in the current frame.

SDLC Receive Address 2
This is the second byte of a two-byte SDLC station address. If the address and control fields are one-byte long each, the control field is located here.

SDLC Receive Control 1
In case of two-byte address or two-byte control, this byte contains the first byte of the SDLC control field received in the current frame.

SDLC Receive Control 2

This is the second byte of a two-byte control field. If the control field is two bytes long, it is always located in bytes 10 and 11.

Microcode Interaction with MOSS

The interconnection between the MOSS and the HSS is based on:

- IOH instructions issued by MOSS.
- A dedicated communication area located in CCU storage called the 'MOSS area'. This area can be read and written by MOSS and by the HSS. It is divided into two parts:
  - A parameter/status area in which each of the scanners has its own specific 'mail box'.
  - A data area used by functions like 'Alter/Display', 'Dump', 'IML' and 'Init'.
- A special interrupt line through which a scanner can interrupt MOSS on level 4 to signal completion of a command.

In all cases, the HSS acts as a slave to the MOSS and therefore cannot initiate any unexpected action. The MOSS communicates with only one scanner at a time.

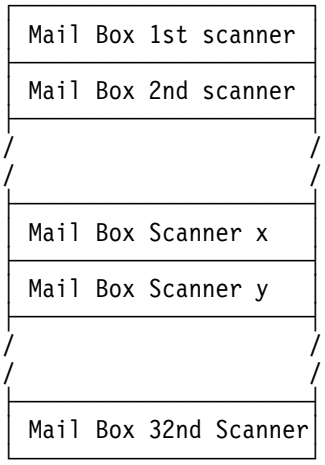
Communication Schemes

Communications between MOSS and the HSS for any function requested from MOSS follow one of the schemes hereafter:

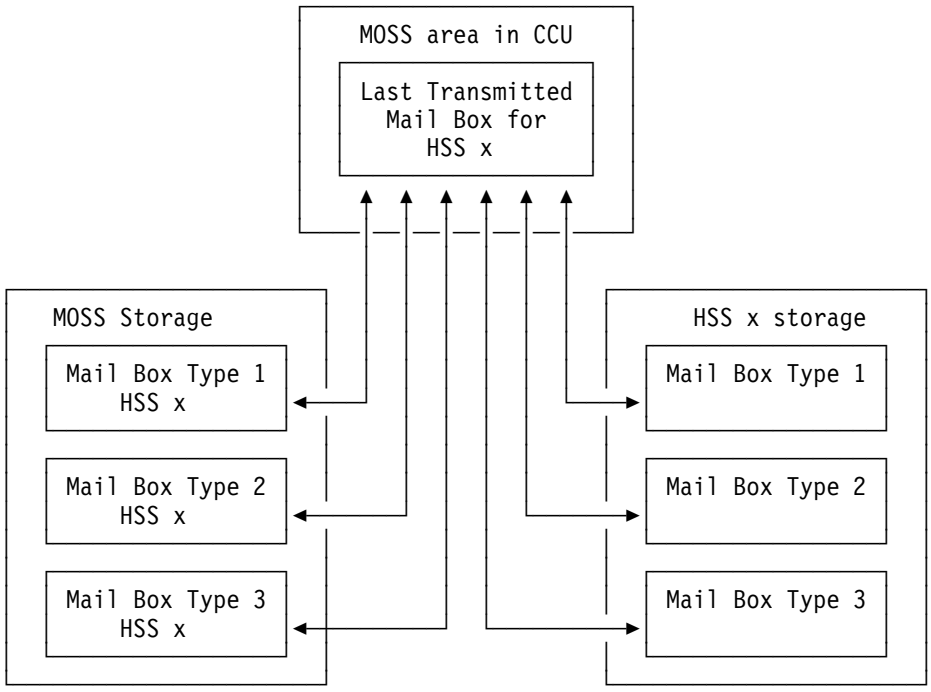
1. Input IOH where two bytes of data are synchronously returned to MOSS at the TD area of the IOH. The MOSS area is not used. There is no MOSS interrupt. The following applications use this scheme:
   - Get scanner status
   - Get processor checkout results
   - Get command completion
   - Get error status.
2. Output IOH where there is no mail box and no interrupt. MOSS sets a timer at the completion of which it can interrogate the HSS with an input IOH. The following applications use this scheme:
   - Scanner reset
   - Run processor checkout
   - Set MOSS area high
   - Set MOSS area low.
3. Output IOH where the mail box is used for status and/or parameters and no interrupt. The HSS transfers its own mail box from the MOSS area into CSP storage to get the parameters. After completion of the command, the HSS puts its command status into the status part of the MOSS area mail box.
4. Output IOH where there are no mail box for parameters, status in mail box for errors, MOSS interrupt. MOSS waits for its timer to expire or for the HSS interrupt.
5. Output IOH where the mail box is used for parameters, status for errors, interrupt. MOSS waits for its timer to expire or for the HSS interrupt.

MOSS Area Layout

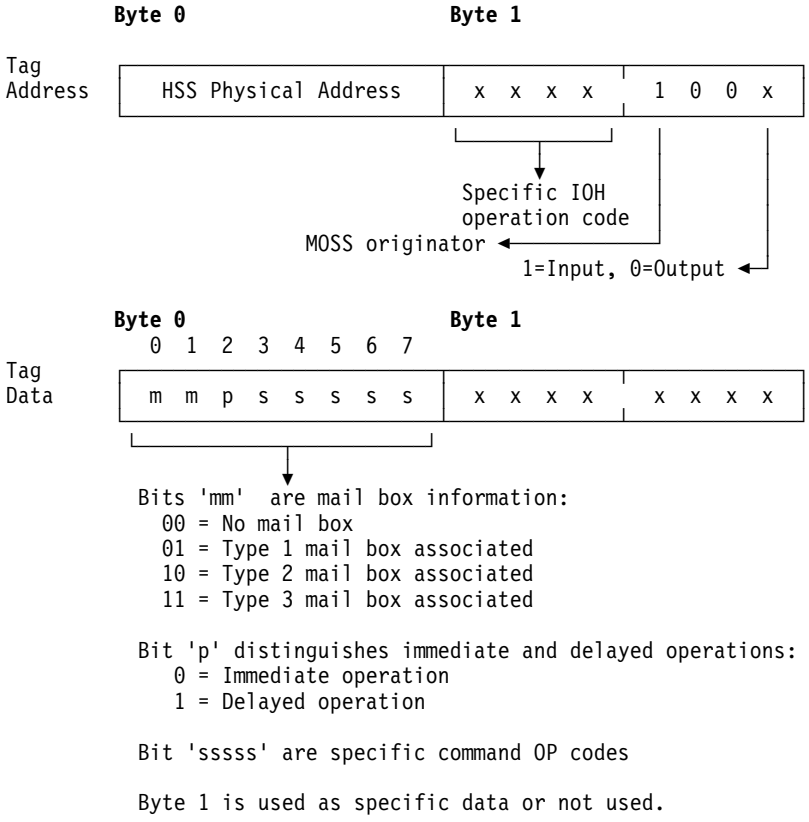
The MOSS area is located in CCU storage. The beginning address of this area is provided to the HSS via the set MOSS area high and set MOSS area low IOHs. The following figure shows the scanners/MOSS mail box area layout used by the HSS:



Mail Box Layout



MOSS I/O Instruction (MMIO)



HSS Registers

HSS CSP External Registers

The HSS CSP microcode uses the same external register format and numbering as the LSS CSP microcode. Refer to the Chapter 4, "Transmission Subsystem" for more information on the CSP external register bit descriptions.

FESH External Registers

X'10': Level 2 Status Register

In Transmit

Bit	Meaning
0	Always 0
. 0	Always 0
. . 0	Always 0
. . . x	End of transmit
. . . . x . . .	Underrun
. . . . . x . .	Driver check
. . . . . . * *	Not used

Modem Change

Bit	Meaning
0	Always 0
. 0	Always 0
. . 1	Always 1
. . . x	DSR – I
. . . . x . . .	CTS – R
. . . . . x . .	Controlled not ready
. . . . . . x .	Local Wrap
. . . . x	Remote Wrap

DMA Error

Bit	Meaning
1	Always 1
. 0	Always 0
. . 0	Always 0
. . . x	DMA interconnection error
. . . . x . . .	DMA time out
. . . . . x . .	DMA burst count error
. . . . . . x .	DMA error during read (1) or write (0)
. . . . *	Not used

Receive

Bit	Meaning
0	Always 0
. 1	Always 1
. . 0	Always 0
. . . x	End of receive
. . . . x . . .	Receive ending condition bit 1 ┐ See
. . . . . x . .	Receive ending condition bit 2 ┤ note
. . . . . . x .	Receive ending condition bit 3 ┘
. . . . *	Not used

Note: Receive Ending Condition Bits 4 5 6

0 0 0	CRC OK
0 0 1	CRC bad
0 1 0	Flag off boundary
0 1 1	M—code program error
1 0 0	Abort (not followed by idle)
1 0 1	Idle
1 1 0	Overrun
1 1 1	Not used

Buffer Request

Bit	Meaning
0	Always 0
. 1	Always 1
. . 1	Always 1
. . . * * * * *	Not used

FESH Error

Bit	Meaning
1	Always 1
. 1	Always 1
. . 0	Always 0
. . . x	CSP interconnection error
. . . . x . . .	FESH internal error
. . . . . * * *	Not used

X'11': SCTL Error

When X'10' contains a DMA error type '100':

Bit	Meaning
1 0 1	always 101
. . . x	SCTL/DMSW error line 0
. . . . x . . .	SCTL/DMSW error line 1
. . . . . x . .	SCTL/DMSW error line 2
. . . . . x .	SCTL/DMSW error line 3
. x	Parity error on switch-to-FESH transfer

X'12': Indirect Addressing Selection and High

Bit	Meaning
x	Address bit 8
. x	Address bit 9
. . x	Address bit 10
. . . x	Address bit 11
. . . . x . . .	Address bit 12
. . . . . x . .	Read (1) or write (0)
. . . . . x .	Function bit 0 ┐
. x	Function bit 1 ┘ See note below

Note: Function Bits 6-7 = 0 0 Command
0 1 Indirect external registers
1 0 External RAM (receive queue, data buffers, control words, etc).
1 1 M-code RAM

Commands: The following are the microcode hexadecimal values

10	Receive	80	Soft stop transmit
20	Receive continue	90	Hard stop transmit
30	Flush to end of frame	A0	Start modem monitoring
40	Stop receive	B0	Start modem-out
60	Start transmit initial	C0	Start data management
70	Start transmit	D0	Status taken by microcode

X'13': Indirect Addressing Low Address

Bit	Meaning
x	Address bit 0
. x	Address bit 1
. . x	Address bit 2
. . . x	Address bit 3
. . . . x . . .	Address bit 4
. . . . . x . .	Address bit 5
. . . . . x .	Address bit 6
. x	Address bit 7

X'14': Data Register 1

Bit	Meaning
x	Data bit 0
. x	Data bit 1
. . x . . .	Data bit 2
. . . x . .	Data bit 3
. . . . x .	Data bit 4
. x	Data bit 5
. . . . . x .	Data bit 6
. x	Data bit 7

X'15': Data Register 2

Bit	Meaning
x	Data bit 0
. x	Data bit 1
. . x . . .	Data bit 2
. . . x . .	Data bit 3
. . . . x .	Data bit 4
. x	Data bit 5
. . . . . x .	Data bit 6
. x	Data bit 7

X'17': Miscellaneous FESH

The indirect registers are selected by external registers X'12' and X'13'.

Bit	Meaning
x	Data management operation complete
. x	Freeze FESH
. . x . . .	FESH EC level bit 0
. . . x . .	FESH EC level bit 1
. . . . x .	FESH EC level bit 2
. x	CDS bit 0
. . . . . x .	CDS bit 1
. x	CDS bit 2

FESH Indirect Registers

These indirect registers are selected by the FESH external registers 12 and 13.

X'00': Data Management Layer DMA Burst Length

Bit	Meaning
x	DMA burst length for the FESH data management layer (in bytes)
. x	
. . x	
. . . x	
. . . . x . . .	
. . . . . x . .	
. . . . . . x .	
. . . . x	

X'01': Receive Layer DMA Burst Length

Bit	Meaning
x	DMA burst length for the FESH receive layer (in bytes)
. x	
. . x	
. . . x	
. . . . x . . .	
. . . . . x . .	
. . . . . . x .	
. . . . x	

X'02': Transmit Layer DMA Burst Length

Bit	Meaning
x	DMA burst length for the FESH transmit layer (in bytes)
. x	
. . x	
. . . x	
. . . . x . . .	
. . . . . x . .	
. . . . . . x .	
. . . . x	

X'03': Receive Layer NCP Buffer Prefix Length

Bit	Meaning
x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x .	NCP buffer prefix length for the FESH receive layer (in bytes)

X'04': Transmit Layer NCP Buffer Prefix Length

Bit	Meaning
x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x .	NCP buffer prefix length for the FESH transmit layer (in bytes)

X'05': Receive Data Area Maximum Length

Bit	Meaning
x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x .	Maximum length of the receive data area available for data storage (in bytes)

X'06': Line Interface Selection Register (Transmit)

Bit	Meaning
x	Port 1 (0) or port 2 (1)
. x	V.35 (0) or X.21 connected (1)
. . x	Interface enabled
. . . * * * * .	Not used
. . . . x	Enable CTS gating

X'07': Miscellaneous Information (Receive)

Bit	Meaning
* * * *	Not used
. . . . x . . .	Enable SDLC address compare
. . . . . x . .	Enable extended SDLC address compare
. . . . . . x .	Enable satellite echo suppression
. . . . *	Not used

X'08': DSR Change Confirmation Timer (Transmit)

Bit	Meaning
x	DSR timer bit 0
. x	DSR timer bit 1
. . x	DSR timer bit 2
. . . * * * * *	Not used

X'09': CTS Change Confirmation Timer (Transmit)

Bit	Meaning
*	Not used
. x	CTS timer bit 0
. . x	CTS timer bit 1
. . . x	CTS timer bit 2
. . . . x . . .	CTS timer bit 3
. . . . . x . .	CTS timer bit 4
. . . . . . x .	CTS timer bit 5
. . . . *	Not used

X'0B': Modem-In Interface (Transmit)

Bit	Meaning	
	V.35	X.21
x	DSR	
. x	CTS	– I
. . * * * . . .	Not used	
. . . . . x . .	Received data	– R
. . . . . * .	Not used	
. x	CTS dropped	

X'0C': Modem-Out Interface (Transmit)

Bit	Meaning	
	V.35	X.21
x	DTR	
. x	CTS	– C
. . x		'T' lead enable
. . . x		'T' lead enable
. . . . x . . .	TC	
. . . . . x . .	Cable ID bit 0	
. . . . . x .	Cable ID bit 1	
. x	Cable ID bit 2	

X'0D': Diagnostic Register (Transmit)

Bit	Meaning
x	2 Mbps DCE wrap mode
. x	Diagnostic DCE wrap mode
. . x	Diagnostic DCE data bit
. . . x	Diagnostic DCE clock bit
. . . . x . . .	NRZI mode
. . . . . x . .	Line at mark (0) or continuous flags (1) after EOT
. . . . . * *	Not used

X'0E': SDLC Address Compare Register 1 (Receive)

Bit	Meaning
x	Station address bit 0
. x	Station address bit 1
. . x	Station address bit 2
. . . x	Station address bit 3
. . . . x . . .	Station address bit 4
. . . . . x . .	Station address bit 5
. . . . . . x .	Station address bit 6
. . . . x	Station address bit 7

X'0F': SDLC Address Compare Register 2 (Receive)

Bit	Meaning
x	Station extended address bit 0
. x	Station extended address bit 1
. . x	Station extended address bit 2
. . . x	Station extended address bit 3
. . . . x . . .	Station extended address bit 4
. . . . . x . .	Station extended address bit 5
. . . . . . x .	Station extended address bit 6
. . . . x	Station extended address bit 7

X'10': Diagnostics (DMA/CSP)

Bit	Meaning
x	Disable '+ DMA Ready' signal from switch card
. x	a] See note below
. . x	b]
. . . x	Force bad parity on external register address
. . . . x . . .	Force bad parity on cycle steal address
. . . . . x . .	Disable external register data parity checker
. . . . . . x .	Disable external RAM parity checkers
. . . . x	Disable all internal data bus parity checkers

Note: a b = 0 0 Normal operation
0 1 Force bad parity on FESH—to—SCTL transfer
1 0 Force bad parity on SCTL—to—FESH transfer (byte 0)
1 1 Force bad parity on SCTL—to—FESH transfer (byte 1)

X'11': Local Attach Line Speed (Transmit)

Bit	Meaning
x	Transmit clock failure
. x	Receive clock failure
. . * * * * . .	Not used
. . . . . x .	Line speed bit 0 ┐ See note below
. x	Line speed bit 1 ┘

Note: Line speed bits 6 7

0 0	245.78 kbps
0 1	1.8432 Mbps
1 0	1.47456 Mbps
1 1	Used by hardware

Error Detection and Reporting

Program/Hardware Checks

In addition to the program/hardware errors reported in the command status via level 2 interrupts, the CCU may be notified by a CCU level 1 interrupt that a program or hardware check occurred.

To obtain the error information, the control program issues a get error status instruction, which transfers a two-byte error status to the CCU.

The control program also resets the check and the interrupt, and performs the recovery actions. The following conditions may cause a level 1 program or hardware check:

1. CCU/HSS problems:
   - IOH/IOHI instruction not supported.
   - IOH/IOHI rejected because there is already an outstanding command on the interconnection. For example, a second transmit command has been sent while a transmit command is already outstanding.
   - IOH/IOHI rejected because a set mode command has not yet been received for that line.
   - Abnormal conditions detected during I/O operations on the IOC bus. These errors may be detected by the CCU or by the HSS. Errors are related to CCU storage and address checks, invalid sequences, timed-out IOH/IOHI instructions.
2. HSS problems:
   - Invalid interrupts.
   - Microcode-detected program failures. (These set the microcode check bit in the error status and cause the NCP to issue a get microcode check instruction.)
   - CCU level 2 interrupt stack overflow.
   - CSP or FESH hardware check (for example parity or address check).

After receiving a level 1 interrupt from the FESH, the CSP microcode builds the error status, freezes the FESH, and waits for the get error status IOH.

Once the get error status has been answered, the CSP enters the disconnect/stop environment and ignores all IOH instructions generated by the NCP. Re-IML of the CSP microcode is required to return to an operational state. The only exception to this sequence of events is a level 1 interrupt caused by a command reject.

Refer to “Error Status” on page 6-57 for the error status description.

Hardware Error Detection and Reporting

Two types of error:

- DMA and modem interface errors which raise the level 2 interrupt to the CSP.
- Errors which raise the level 0 interrupt to the CSP.

Internal Box Error (IBE) Reporting

The internal box errors generate box event records (BERs). For details on BERs, see chapter 12, "Box Event Records (BER)".

The IBEs can be divided into three categories:

1. CSP and FESH internal errors or events (similar to the errors defined for the CSP/FES in the LSS):
   - Adapter interconnection check
   - CSP interconnection error
   - FESH failing to answer
   - No interrupt from FESH
   - Invalid interrupt from FESH
   - Command rejected
   - Trace already active (event, not error)
   - FESH internal error
   - Local attach clock failure
   - AIO error
   - Line not accessible (one of the two possible lines is already active)
2. DMA errors detected by the FESH:
   - DMA parity error during write or read
   - DMA time out during write or read
   - DMA bus driver fault
   - DMA burst count error
   - DMA interconnection errors for improper DMA tag sequence.
3. Errors detected in the SCTL/switch cards:
   - Storage internal error
   - SCTL internal error
   - DMA internal error
   - DMA logical error
   - DMA storage protect/address exception
   - DMA interconnection error in read or write (a)
   - DMSW parity check main bus (b)
   - DMSW parity check primary/secondary bus (c)
   - DMSW driver fault. (d)

Notes:

1. The following errors can occur concurrently:
   - a and b
   - or b and c
   - or b and d
   - or a, b, and c
2. All the above-listed errors are reported to the NCP via a level 2 interrupt and associated status area as an LCS and ELCS code (refer to “Line Communi-

cation Status (LCS)" on page 4-191 and "Extended Line Communication Status (ELCS) (Initial Status=B'110') for HSS" on page 4-195 for code description).

3. The SCTL/switch errors and the FESH DMA interconnection errors are mutually exclusive. There is no double-reporting of errors.

DMA Interconnection Errors Detected by FESH (Register X'10')

DMA Tag Sequence

The FESH circuitry monitors the sequence of the DMA interconnection signals from the SCTL/switch card.

An error is reported when the tag sequence does not occur properly.

DMA Data Bus Parity Checker

This parity checker verifies the validity of the data received/sent, from/to the DMA data bus byte 0 and byte 1 by the FESH.

DMA Time out

One hardware timer is implemented to detect possible time out conditions on the DMA bus.

The duration of the timer is in the range of 100 ms to cover a complete transfer operation on the DMA bus.

DMA Burst Count Checker

This checker verifies that the transfer is satisfactorily completed on the DMA bus when the burst count in the FESH reaches zero.

SCTL/Switch Card Detected Errors Reported by FESH

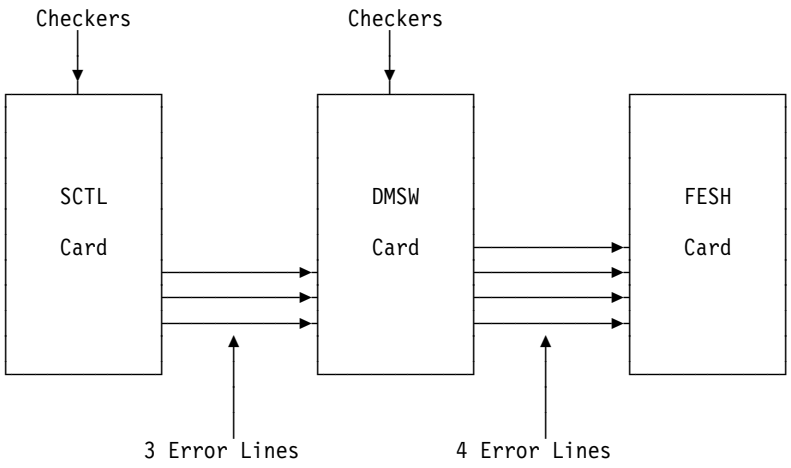
The SCTL-DMA card and the switch cards have internal checkers which detect the following error conditions which may occur during a DMA transfer initiated by an HSS (see the figure 'Line Error Hexadecimal Code' next):

Line Error Hexadecimal Code	SCTL–DMA/Switch Error Conditions								
	a	b	c	d	e	f	g	h	i
0	Normal mode (no error)								
1	x								
2		x							
3			x						
4				x					
5					x				
6						x			
7							x		
8								x	
9									x
A					x	x			
B						x	x		
C						x		x	
D									
E									
F					x	x	x		

Figure 6-7. Line Error Hexadecimal Code

- SCTL error detection:
  a. DMA internal error
  b. DMA logical error
  c. DMA storage protect/address exception error
  d. Storage unrecoverable error or control error
  e. DMA interconnection error
     - Switch card error detection:
  f. DMSW parity check main bus
  g. DMSW parity check primary/secondary bus
  h. DMSW DMA driver fault
  i. Not used

The error conditions just described are encoded by the SCTL-DMA card and the switch card, and reported on 4 x SCTL/DMSW error lines which go from the DMSW card to the FESH card as shown next:



Reporting

Reporting DMA errors is done by issuing a level 2 interrupt to the CSP. The nature of the error is set into an LCS/ELCS (refer to “Line Communication Status (LCS)” on page 4-191 and “Extended Line Communication Status (ELCS) (Initial Status=B'110') for HSS” on page 4-195 for code description).

When any of the above checkers becomes active:

1. The hardware:
   - Stores the corresponding error condition in an error register X'10' and X'11'.
   - Interrupts the CSP microcode.
2. The CSP microcode
   - Stops the transmit and receive operations in process.
   - In case of transmit, puts the transmit data line at mark.
   - In case of receive, stops the receive command and modem monitoring.

DMA/SCTL Errors

They are reported by the FESH through a level 2 interrupt and then both interface are disabled by the microcode.

The CSP microcode fills the LCS field of the PSA status with a status byte telling the reason for the error (refer to “Line Communication Status (LCS)” on page 4-191 and “Extended Line Communication Status (ELCS) (Initial Status=B'110') for HSS” on page 4-195 for code description).

The microcode then raises CCU level 2 interrupt.

Line interfaces are started again by the CSP microcode when the NCP sends the proper SDLC command sequence.

CSP Interconnection Errors

The CSP communicates with the FESH through the external registers located in the FESH (register range X'0D' to X'17').

The FESH completes the operation with the 'acknowledge' signal to the CSP if no error conditions were detected.

The FESH monitors the CSP interconnection for the following errors:

- Interconnection error signal from the CSP
- Bidirectional cycle steal data bus parity error
- External register address and select out parity error
- Data out odd parity error during an external register write operation.
- External register address invalid.

If an error occurs in the external register address because of a parity error or because the external register does not exist in the FESH, the 'acknowledge' signal is not sent to the CSP.

Also, if the data bus parity is incorrect during an external register write, the 'acknowledge' signal is not sent to the CSP.

When 'acknowledge' is not returned to the CSP by the FESH, the CSP sets the adapter interconnection check bit ON (external register X'03' bit 6 = 1) and terminates the operation.

The FESH does not report any error condition.

Parity errors occurring on the cycle steal interconnection can be detected by the FESH or by the CSP.

If the FESH detects a parity error on the data bus during a cycle steal write, the FESH sets a level 2 interrupt to the CSP with the CSP interconnection error bit ON (external register X'10' bit 3=1) after completing the operation.

The parity checking on the cycle steal address bus and the CSP data bus during a cycle steal or external register read operation is performed by the CSP.

When the CSP detects a parity error, the CSP sets the adapter interconnection check in CSP register X'03' and activates the 'cycle steal error' line.

When the FESH detects this signal, the cycle steal operation ceases and the FESH activates a level 2 interrupt to the CSP.

The CSP interconnection error bit is set ON in FESH external register X'10'.

Detection of this error causes a level 2 interrupt to the CSP.

If an NCP transmit or receive operation is in progress, it continues until the CSP microcode stops reception of data for the receive command, or stops transmission of data and sets the transmission line to mark.

FESH Internal Checkers

Data Parity Checkers

All the microcode (DMA layer, CSP layer, bit-layer, byte-layer) and data are checked for parity when the FESH internal buffers are read or written.

NCP Buffer Handling Logic Checker

In order to check that the hardware logic which calculates the NCP buffer data area address from the NCP buffer prefix is working properly, the transmit and receive byte layer microcodes perform a predetermined calculation during inactivity periods.

If there is a mismatch between the result of the calculation and the predetermined result, the FESH hardware reports an internal error condition.

Reporting

When any of the above checkers becomes active:

- The FESH:
  - Stores the corresponding error condition in an error register.
  - Interrupts the CSP microcode at level 0.
- The CSP microcode:
  - Stops the transmit and receive operations in process.
  - In case of transmit, puts the transmit data line at mark.
  - In case of receive, stops the phase monitor.

Line Interface Check

A driver check function is implemented on the line interfaces of the FESH (V.35 / X.21).

When a driver check is detected, the hardware:

- Sets the driver check bit in the transmission status register.
- Interrupts the CSP.

No other action (no line interface disabling) is taken by the hardware.

Error Status

Error Status Byte 0

Bit	Type 1	Type 2	Type 3
x...	R/W (IOH)	R/W (AIO)	Always ON
.x..	I/O bus check	I/O bus check	Invalid level 0 int.
..x.	Not used	Cycle steal grant	Invalid level 1 int.
...x	I/O bus tag I/O	I/O bus tag I/O	Invalid level 2 int.
.... x...	Halt	Halt	Microcode check
.... .x..	TA	Not used	CS/CCU L2 stack overf.
.... ..x.	TD	TD	Reject: command on cmd
....x	Not used	Not used	Disconnect state

Error Status Byte 1

Bit	Type 1	Type 2	Type 3
x...	TA select	Not used	Command reject
.x..	Not used	Cycle steal select	Invalid output IOH type
..x.	Not used	Not used	┐
...x	Not used	Line interface address bit 0	│
.... x...	Not used	Line interface address bit 1	│
.... .x..	Not used	Line interface address bit 2	├ See note below
.... ..x.	Not used	Line interface address bit 3	│
....x	Invalid input IOH	Line interface address bit 4	┘
....x			Adapter interconn. check

Note: Next comes the decoding of bits 0 to 7 when command reject occurs.

Bit	Normal Command Reject	Trace Command Reject	Invalid Output IOH
x...	Command reject	Command reject	Always OFF
.x..	Always OFF	Always ON	Invalid output IOH
..x.	┐	Not used	Not used
...x	│ Line interface	Not used	┐
.... x...	├ address	┐	│ Line interface
.... .x..	│ (0 to 3F)	├ Slot number	├ address
.... ..x.	│	│ (0 to F)	│ (0 to 1F)
....x	┘	┘	┘

Four types of error may be reported:

Type 1 Error detected by the CCU during PIO. A halt is send to the CSP, which results in a CCU or MOSS level 1 interrupt.

Type 2 Error detected by the CCU during AIO. A halt is send to the CSP, which results in a CCU or MOSS level 1 interrupt.

Type 3 Internal logical errors detected by the CSP microcode. A CCU level 1 or MOSS level 4 interrupt is set.

Hard Stop A CSP microprocessor check has been encountered. The CSP hardware responds with the error status.

The following tables shows the detailed responses that may be presented to a get error status command:

Hard Stop Error Status (Detected by CSP Hardware)

Byte 0

Bit	Meaning
* * * * * . . .	Not used
. . . . . x . .	Control store data check
. . . . . . x .	LSR or external register parity check
. . . . x	Internal check

Only if processor check

Byte 1

Bit	Meaning
x	Unexpected adapter acknowledgment
. x	Control store write data check
. . x	Processor check
. . . x	External register address check
. . . . x . . .	Control store address check
. . . . . x . .	LSR address check
. . . . . * *	Not used

Miscellaneous Status Fields

Refer to the “Miscellaneous Status Fields” on page 4-191 for description of these PSA status fields.

Diagnostic Facilities

Refer to the *3745 Diagnostic Descriptions*, SY33-2059, for more details.

Problem Determination Aids

The following tools are provided to help define which area is failing:

1. Scanner interface trace (SIT) and checkpoint trace (Refer to Chapter 13, "Traces, Dumps and file transfer" in this manual).
2. Line interface display (LID).
3. LSS functions from the MOSS service menu (see *Service Functions Manual*, SY33-2055).

Microcode Service Aids

The FESH registers, the microcode RAM locations and the external data control RAM locations can be accessed, using the following facilities (See *Service Functions Manual*, SY33-2055, and *Advanced Operations Guide*, SA33-0097):

1. Alter/display
2. CSP address compare
3. CSP dumps.

These facilities, invoked from the operator console, help in analyzing/modifying the contents of the HSS storage and registers (CSP and FESH): (see “HSS Registers” on page 6-40 for register description).

Programming Support for Problem Determination

It includes, as for LSS microcode:

1. Error detection
2. Error collection
3. Error reporting.

Types of error tracked are:

- CSP/IOC bus interconnection errors
- CSP internal errors
- CSP/FESH interconnection errors
- DMA/SCTL/Switch errors
- FESH errors
- FESH-to-line interface errors.

NCP Buffer Prefix Validity Checking in Receive

This test is performed by the microcode for the first buffer only, by using the parameters coming from the PSA.

SIT Trace

The scanner interface trace (SIT) traces the address and control field, and up to forty data bytes of each SDLC frame transmitted or received by the high-speed front-end scanner (FESH).

For the CSP, the NCP commands and the CCU IOH commands are also traced to provide a listing of the command and data transmission sequence for the line.

Two halfword control blocks are reserved in the FESH RAM for the SIT trace. These control blocks are located at the following addresses:

- Transmit interface X'C3B'

- Receive interface X'C3C'.

  Refer to Chapter 13 "Traces, Dumps and File Transfer" in this manual, for more information.

Problem Isolation and Network Management

External Wrap Facility

After a power-ON reset, the interface defaults to the 245.76 kbps clock speed if the cable ID bits specify local attach.

The interface is neither selected nor enabled after a power-ON reset.

A different clock selection can be made by the NCP at set mode time with indirect register X'11'.

The FESH also provides an external interface wrap facility by inserting a wrap plug at the tail gate connection. Commands initiating the wrap are sent from the MOSS console.

Notes:

1. The wrap plugs are described on the *External Cable References* manual, SY33-2075.
2. The procedure to perform a wrap test at the tail gate, using a wrap plug, is described in the *IBM Maintenance Information Procedures (MIP)*.

The cable ID bits are changed by the wrap plug. The X.21 or V.35 signals are wrapped as specified by the interface ID bit (indirect register X'06' bit 1) and the clock defaulted to the clock speed selected by the NCP at set mode during a wrap.

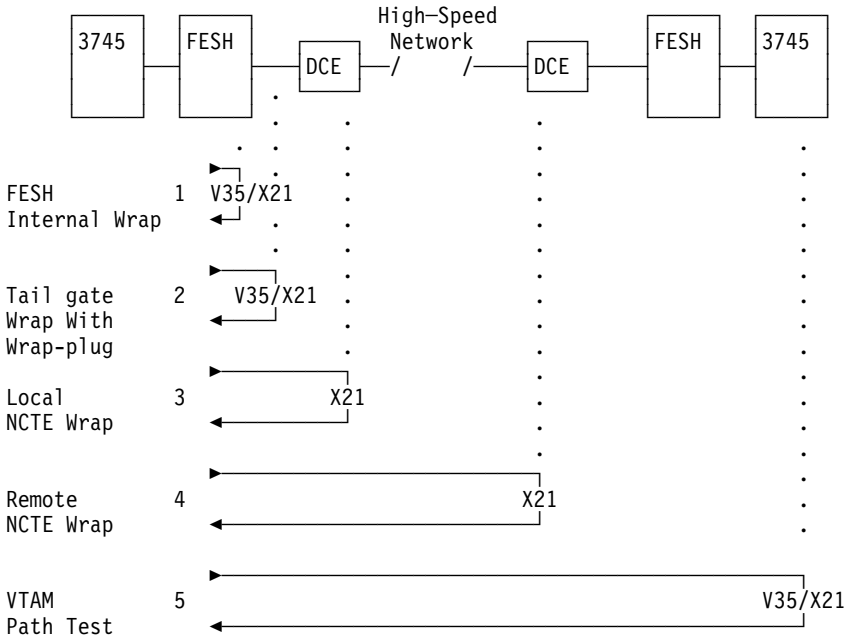
The external clock is under microcode control as specified by external register X'11'.

Wrap Mode at DCE Level

The wrap is started from the MOSS console.

The diagnostics can perform a wrap function from the transmit to the receive interface on the logic side of the line drivers/receivers, at a speed of 1.966 Mbps or at a speed controlled by the diagnostics.

The following figure illustrates the problem determination and testing configuration for V.35/X.21 network attachment.



Note: Test is also available from the right hand side.

Figure 6-8. V.35/X.21 Configuration Showing Wrap Tests or Loop Tests 1 to 5

Manual V.35/X.21 Wrap or Loop Tests

The manual wrap or loop tests are initiated from the MOSS console. (Loop test 3 and 4 are for X.21 only).

Internal Wrap Or **Loop Test 1** checks the ability of the HSS to transmit and receive, up to the output of the FESH card.

Tail Gate Wrap Or **Loop Test 2** in addition to loop test 1 checks the cables between the FESH card and the tail gate. A wrap plug is required.

Local NCTE Wrap Test Or **Loop Test 3** checks the transmit and receive ability of the 3745, up to the first network communication terminal equipment (NCTE).

Remote NCTE Wrap Test Or **Loop Test 4** checks the transmit and receive ability of the 3745, up to the second NCTE and including the communication media.

VTAM Path Test Or **Loop Test 5** checks the transmit and receive ability of the two controllers.

Communication Interfaces

The HSS interfaces external high-speed data links to either the 3745 or the 3725:

- Remotely via DCE attachment
- Locally via direct attachment to another HSS or LIC type 3/4 on the 3725.

The physical and logical interfaces are either:

- CCITT V.35 or,
- CCITT X.21 leased (including French Transfix).

The high-speed data links access the HSS directly through the FESH via the tail gate without a LIC card.

FESH-DCE Interface

The FESH is physically able to support two interfaces. However, only one interface can be active and communicating, while the other interface is disabled.

The NCP controls the enabling and disabling of each interface.

On reception of the line address activation from the NCP, the microcode sets the corresponding bit in the FESH to select the proper port.

To determine which interface was selected by the hardware (V.35 or X.21) on the selected port, the microcode reads the cable ID in the FESH.

The FESH is also capable of supporting different electrical interfaces.

Each of the two physical interfaces can independently support the following interfaces to the network communication terminal equipment (NCTE):

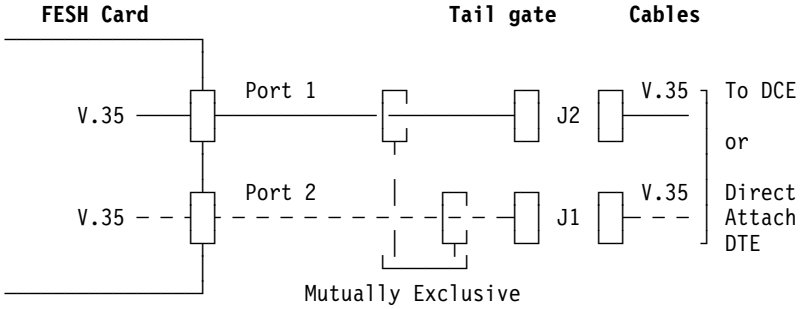
V.35
X.21

Any combination of physical interfaces are supported. The physical interface is identified by cable ID signals in the cable. The following combinations are possible:

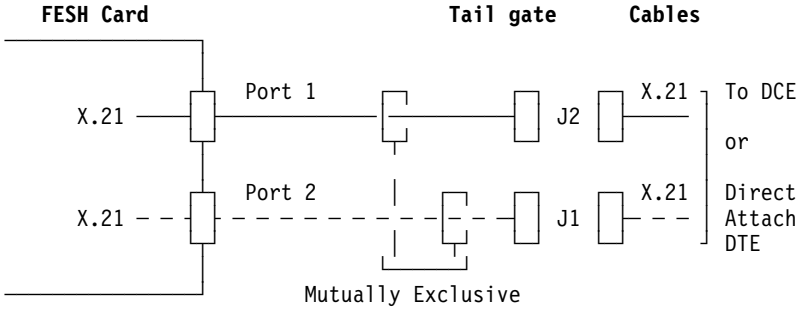
- Two V.35 interfaces
- Two X.21 interfaces
- One V.35 and one X.21 interface

NOTE: Before unplugging the cable from the tail gate or DCE, ensure that the line is not active by disabling the interface, using VTAM commands. Failure to perform this step can cause an FESH adapter check.

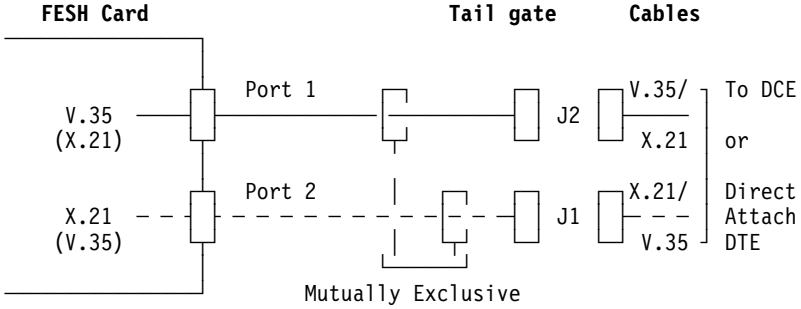
Two V.35 Cables Connected (Example)



Two X.21 Cables Connected (Example)



One V.35 and One X.21 Cables Connected (Example)



The FESH supports the CCITT standard V.35 interface. All interface signals conform to the electrical specifications as stated in the various CCITT standards.

X.21 Interface

The HSS supports the 1987 CCITT X.21 standard for transmitting data at speeds up to 2.048 Mbps.

Cable Diagrams

DCE interface signals exit the FESH using two top card connectors, one for interface 1 and one for interface 2.

Each interface cable contains the V.35, X.21, and cable ID signals to the 3745 tail gate.

All balanced signals use twisted pairs from the tail gate to top card connector.

Unbalanced signals use a twisted pair of wires with one signal wire and one ground wire to eliminate any noise problems.

The **external cable** attached to the tail gate determines the physical interface supported, using the cable ID bits and the V.35 or X.21 identifier.

The FESH hardware gates the appropriate drivers and receivers to the network adapters.

Note: For cable information refer to *External Cable References*, SY33-2075.

Clocking

Because of the high transmission speeds and propagation delays in the cable, the transmit clock received from the DCE or NCTE is re-driven and sent to the DCE or NCTE in synchronization with the data.

Local Attachment

The HSS supports direct attachment (no DCE) with another HSS using the X.21 or V.35 interface.

When directly connected together, one FESH is designated as local attach by the cable ID bits and automatically provides the receive clock to the other FESH.

The other FESH attaches in DCE mode with the external clock supplied by the local attach HSS. Three attachment speeds are offered as specified in indirect register X'11'.

1. 1.8432 Mbps
2. 1.47456 Mbps
3. 245.76 Kbps

List of Abbreviations

A	ampere
abend	abnormal end of task
ABP	active bypass card
AC	1) alternating current 2) abandon call 3) address compare
ACB	adapter control block
ACF	Advanced Communications Function
ACK	affirmative acknowledgement (BSC)
ACPW	ac power box
ACR	1) add character register (instruction) 2) abandon call request
ACU	automatic calling unit
ACUN	acccess unit (token ring access unit such as the IBM 8228)
AC1	ac power box (ACPW) installed in position 1 of the 3746-900
AC2	ac power box (ACPW) installed in position 2 of the 3746-900
ADB1	adapter bus 1
ADB2	adapter bus 2
ADB3	adapter bus 3
ADB4	adapter bus 4
AE	address exception
AEK	address exception key
AFD	airflow detector
AGC	automatic gain control (signal)
AHR	add halfword register (instruction)
AIO	adapter-initiated operation
AIT	algorithm interface table
ALC	Airlines Line Control
ALU	arithmetic and logic unit
AMD	air moving device
ANSI	American National Standards Institute
AR	add register (instruction)
ARC	active remote connector
ARI	add register immediate (instruction)
AS	autoselection chain
ASCII	American National Standard Code for Information Interchange
AUI	attachment unit interface
AXB	adapter expansion block
B	1) branch (instruction) 2) byte
BAL	branch and link (instruction)
BALR	branch and link register (instruction)
BAT	basic assurance test
BB	branch on bit (instruction)
BCC	block check character (BSC)
BCCA	buffer chaining channel adapter
BCCW	bit clock control word
BCD	binary-coded decimal notation
BCL	branch on C latch (instruction)
BCLE	buffer control list element
BCT	branch on count (instruction)
BER	box event record
B/M	bill of material
BPC1	bus propagation card type 1
BPC2	bus propagation card type 2
bps	bits per second
BR	bus request
BRC	BER reference code
BSC	binary synchronous communication
BT	branch trace
BTAM	Basic Telecommunications Access Method
BTAM-ES	BTAM extended support
BZL	branch on Z latch (instruction)
C	1) Celsius 2) control (X.21 signal)
CA	channel adapter
CAB	channel adapter board
CAC	common adapter code
CACM	channel adapter concurrent maintenance
CADR	channel adapter driver receiver card
CADRUK	channel adapter driver receiver type UK card
CADS	channel adapter data streaming
CAL	channel adapter logic card
CAL6	CAL type 6 for CADS
CAL7	CAL type 7 for BCCA

CAMPOR CA MOSS power-ON-reset (register)

CARST CA reset (register)

CATPS channel adapter with two-processor switch

CB circuit breaker

CBC controller bus coupler

CBTRA controller bus and token-ring adapter

CBSA controller bus and service adapter (CBSP+CBC+TIC3)

CBSP controller bus and service processor

CCITT Comite Consultatif International Telegraphique et Telephonique. The International Telegraph and Telephone Consultative Committee

CCMD current command (storage)

CCN communications controller node

CCPF common customer profile facility

CCR compare character register (instruction)

CCU central control unit

CCW channel command word

CD 1) carrier detector (signal)
2) connector

CDF configuration data file

CDG concurrent diagnostic

CDS configuration data set (NCP/EP)

CE customer engineer

CEPT Comite Europeen des Postes et Telecommunications

CHCV channel control vector

CHCW channel control word

CHIO channel input/output

CHPID channel path identification

CHR compare halfword register (instruction)

CI calling indicator (signal)

CLDP controller load/dump program

CLP communication line processor

CMOS complementary metal oxide semiconductor

CMSA CCU/MOSS status register A

CMSB CCU/MOSS status register B

CMSC CCU/MOSS status register C

CNM communication network management

CNMI communication network management interface

CNSL console

CO/CS contact operate/contact sense

CONFSW configuration switch

CP 1) communication processor, control program
2) circuit protector

CPIT control program information table

CPM connection point manager

CPN customer problem number

CPR channel pointer register

CPT checkpoint trace

CR 1) compare register (instruction)
2) call request (signal)

CRC cyclic redundancy check character

CRI compare register immediate (instruction)

CRP check record pool

CRQ call request

CRU customer replaceable unit

CS 1) cycle steal
2) communication scanner
3) connectivity switch

CSA common subassembly

CSC connectivity switch cable

CSCE connectivity switch cable extension

CSCW cycle steal control word

CSG cycle steal grant

CSGH cycle steal grant high

CSGL cycle steal grant low

CSP communication scanner processor

CSR cycle steal request

CSRH cycle steal request high

CSRL cycle steal request low

CSS control subsystem

CSU 1) customer setup
2) customer service unit (DCE-like for high-speed communication lines)

CSW channel status word

CTS clear to send (signal)

CW control word

CZ carry/zero (latch)

DAF destination address field (SNA)

DB data byte

DC 1) direct current
2) data chaining (channel status)

DCAF Distributed Console Access Facility

DCDP dc distribution and protection box

DCE data circuit-terminating equipment

DCF diagnostic control function

DCM diagnostic control monitor

DCPW dc power box

DCRLSD data channel receive line signal detector (same as CD)

DDS digital data service

DE device end (channel status)

DFA disk file adapter card

DFI defect-free installation

DI data in

DICO DMA IOC connection card

DIFF differentiator

DIV diagnostic information vector

DLE data link escape character

DLO data line occupied (signal)

DMA direct memory access

DMSW direct memory access switch card

DMUX double multiplex card for board on LIC unit 1

DO data out

DOI duration of interrupt

DP digit present (signal)

DPR digit present request

DRA duration of repair action

DRS data rate select

DRV driver

DS data streaming

DSC distant station connected

DSI data store interface

DSR data set ready (signal)

DSRS data signaling rate selection (signal)

DSU data service unit (DCE-like for high-speed communication lines)

DTE data terminal equipment

DTER DMA bus terminator

DTR data terminal ready (signal)

DVB device block

DX duplex

EAC Ethernet adapter card

EBCDIC extended binary-coded decimal interchange code

EC engineering change

ECB even control block

ECC error checking and correction

EDE elementary data exchange

ED/FI error detection/fault isolation

EIA Electronic Industries Association

EIB error intermediate block

EINTP1 extended interrupt 1 (register)

EIRV error interrupt request vector

ELA Ethernet LAN adapter

ELCS extended line communication status

ENQ enquiry (BSC)

EOT end of transmission (BSC)

EP emulation program

EPO emergency power-OFF

ERC error reference code

EREP environmental recording, editing, and printing (program)

ERP error recovery procedure

ESC emulation subchannel (address)

ESCA ESCON channel adapter. An ESCA consists of an ESCON channel processor (ESCP) and an ESCON channel coupler (ESCC)

ESCH emulation subchannel high (address)

ESCC ESCON channel coupler. A communication controller hardware unit which is the interface between the ESCON channel processor and the ESCON fiber optic cable

ESCC2 ESCON channel coupler type 2

ESCL emulation subchannel low (address)

ESCON channel A channel having an Enterprise System Connection* channel-control-unit interface that uses optical cables as a transmission medium

ESCP ESCON channel adapter. A communication controller hardware unit which provides the channel data link control for the ESCON channel adapter

ESD electrostatic discharge

ESS Ethernet subsystem

ETB end-of-transmission block character (BSC)

ETG Ethernet tail gate

ETX end-of-text character (BSC)

EXP expected

FAC flag address control (SDLC frame)

FALC front end scanner low speed card for Air Line Control (ALC) lines

FCC Federal Communications Commission

FCPS final call progress signals (X.21)

FCS frame check sequence

FDD flexible disk drive

FDS flat distribution system

FDX full-duplex (synonym for duplex)

FE field engineering

FEIS field engineering information system

FERR FESA error register

FES front-end scanner

FESA front-end scanner adapter

FESH front-end scanner (high-speed)

FESL front-end scanner (low-speed)

FID4 format identification 4

FM frequency modulation

FPS FES parameter/status

FRPE frame relay performance enhancement

FRU field-replaceable unit

ft foot

GPR general purpose register

GPT generalized PIU trace

GTF generalized trace facility

HCS Hardware Central Service

HDD hard disk drive

HDR header

HDX half-duplex

hex hexadecimal

hh hexadecimal value hh

HLIR high-level interrupt request

HLU highest logical unit (largest CPU in an establishment)

HPP bus high-performance parallel bus

HPTSS high-performance transmission subsystem

HSB high-speed buffer

HSC high-speed channel

HSS high-speed scanner

HW hardware

Hz Hertz

I indication (signal)

IACK interrupt acknowledgement

IAR instruction address register

IBE internal box error

IC insert character (instruction)

ICA integrated communication adapter

ICB interface control block (storage)

ICF internal clock function

ICT insert character and count (instruction)

ICW interface control word

ID identifier

IEEE Institute of Electrical and Electronics Engineers

IFT internal function test

IMB in mailbox (MOSS)

IML initial microcode load

in. inch

IN input (instruction)

INN intermediate network node

INOP inoperative (line, modem, or terminal)

INS information network system

INTP1 interrupt 1 (register)

INTP4 interrupt 4 (register)

IOC input/output control

I/O input/output

IOCB input/output control bus

IOCS input/output control system

IOH input/output halfword (instruction)

IOHI input/output halfword immediate (instruction)

IOIRR input/output interrupt request register

IOIRV input/output interrupt request vector

IOSW input/output switch (card) for 3745 models 21x and 41x

IOSW2 input/output switch (card) for 3745 models 31x and 61x

IPF instruction pre-fetch

IPL initial program load

IPR isolated pacing response (SNA)

IR interrupt request

IRR interrupt request removed

ISDN integrated service digital network

ISL inbound serial link

ISO International Organization for Standardization

ITB intermediate text block (BSC)

ITER IOC bus terminator

IVT isolation verification tests

K 1024 (bytes or words)

KB kilobyte (1024 bytes)

KBD keyboard

kbps kilobits per second

kg kilogram

kHz kilohertz

L load (instruction)

LA 1) load address (instruction)
2) line adapter

LAB line adapter board

LAN local area network

LAP line adapter processor

LAR lagging address register

LAS line adapter status

LCB line control block (storage)

LCBB line connection box base

LCBE line connection box expansion

LCD line control definer (storage)

LCEB line connection enclosure base

LCEE line connection enclosure expansion

LCOR load character with offset register (instruction)

LCPB line connection power base

LCPE line connection power expansion

LCR load character register (instruction)

LCS line communication status (storage)

LDF line description file

LED light-emitting diode

LERR line error register/driver check

LH load halfword (instruction)

LHOR load halfword with offset register (instruction)

LHR load halfword register (instruction)

LIB 1) line interface buffer
2) LIC board

LIB1 LIC board type 1 for LICs type 1, 3, and 4

LIB2 LIC board type 2 for LICs type 5 and 6

LIC line interface coupler card

LIC1 line interface coupler type 1 (card)

LIC3 line interface coupler type 3 (card)

LIC4 line interface coupler type 4 (card)

LIC5 line interface coupler type 5 (card)

LIC6 line interface coupler type 6 (card)

LID line interface display

LIU line interface coupler unit

LIU1 LIC unit 1 for LICs type 1, 3, and 4

LIU2 LIC unit 2 for LICs type 5, and 6

LLAP LIC line analysis procedure

LLB local loopback

LLIR low-level interrupt request

LL2 link level 2 test

LNVT line vector table

LOR load with offset register (instruction)

LPDA Link Problem Determination Aid

LR load register (instruction)

LRC longitudinal redundancy check

LRI load register immediate (instruction) local storage

LRU least-recently used

LS local storage

LSAR local storage address register

LSI large scale integration

LSR local storage register (CSP)

LSS low-speed scanner

LSSD level-sensitive scan design

LT local test

LTC1 line terminator card for CAB1 addressing

LTC2 line terminator card for CAB2 addressing

LU logical unit

m meter

mA milliampere

MAC MOSS adapter card for 3745 models 21x and 41x

MAC2 MOSS adapter card for 3745 models 31x and 61x

MAP maintenance analysis-procedure

MAT manual assurance test

MAU media access unit

MB megabyte; 1 048 576 bytes

MCA MOSS console adapter card

MCAD MOSS/CA adapter

MCC MOSS control card

MCCU MOSS/CCU adapter

MCF microcode fix

MCPC machine check/program check

MCT machine configuration table

MDOR MOSS data operand register

MDR miscellaneous data record

MERR MUX error

MES miscellaneous equipment specification

MFM modified frequency modulation

MHz megahertz

MICB MOSS interface control block

MIM Maintenance Information Manual

min minute

MIO MOSS input/output

MIOC MOSS I/O control bus

MIOH MOSS input/output halfword

MIOHI MOSS input/output halfword immediate

MIP Maintenance Information Procedures

MIR Maintenance Information Reference

MIT MOSS interface table

MLA MOSS LAN adapter

MLC machine level control

MLT machine load table

mm millimeter

MMIO memory mapped input/output

MMOD MOSS mode

MOD modifier

MOSS maintenance and operator subsystem

MOSS-E MOSS extended

MPC MOSS processor card for 3745 Models 210 to 610

MPC2 MOSS processor card for 3745 Models 21A to 61A

MPS multiple port sharing

ms millisecond

MSA machine status area

MSAU multistation access unit

MSC MOSS storage card for 3745 Models 210 to 610

MSC2 MOSS storage card for 3745 Models 21A to 61A

MSD machine status display

MUX multiplex function

mV millivolt

MVS Multi Virtual Storage

NA not applicable

NAK negative acknowledgment character (BSC)

NCCF Network Communications Control Facility

NCP Network Control Program

NCR AND character register (instruction)

NCTE network communication terminal equipment

NHR AND halfword register (instruction)

NLDM Network Logical Data Manager

NMPF network management program facilities

NMVT network management vector transport

NO-OP no-operation instruction

NOSP network operation support program (VTAM)

NPDA Network Problem Determination Application

NPM NetView performance monitor

NPSI network packet switching interface

NR AND register (instruction)

NRI AND register immediate (instruction)

NRZI see NRZ-1

NRZ-1 non return-to-zero change on ones recording

NS new sync (signal)

ns nanosecond

NSC native subchannel (address)

NTO Network Terminal Option

NTT Nippon Telegraph and Telephone (Japanese PTT)

N/A	Not available or not applicable
oc	overcurrent
OCR	OR character register
ODG	offline diagnostic
OEM	original equipment manufacturer
OEMI	original equipment manufacturer's interface
OHR	OR halfword register
OLT	online test
OLTEP	online test executive program
OLTSEP	online test stand-alone execution (program)
OLTS	online test system
OLTT	online terminal test
OMB	out mailbox
OP	operation decode
OR	OR register (instruction)
ORI	OR register immediate (instruction)
OS	Operating System
OSL	outbound serial link
OUT	output (instruction)
ov	overvoltage
PAC	power analog card
PAP	previous adapter present
PAR	problem analysis and repair
PC	personal computer
PCB	power control bus
PCF	primary control field (storage)
PCI	program-controlled interrupt
PCR	power check reset
PCSS	power control subsystem
PCW	processor control word
PCWC	power control wrap card
PD	problem determination
PDAID	problem determination aids
PDB	power distribution board
PDF	parallel data field (storage)
PE	Product Engineering
PEP	partitioned emulation program
PF	programmable function
PFAR	prefetch address register
PI	power indication (signal)
PIO	program-initiated operation
PIRR	program interrupt request register
PIRV	program interrupt request vector
PIU	pass information unit
PKD	portable keypad display
PLC	power logic card
PN	part number
PND	present next digit (signal)
POPR	prefetch operation register
POR	power-ON reset
POS	power ON services
PRC	processor
PROM	programable read-only memory
PS	power supply
PSA	program status area
PSS	power subsystem
PSTCE	product support trained CE
PSTY	power supply type
PSV	program status vector
PSW	program status word
PSx	power supply type x
PTCE	product-trained CE
PTER	power bus terminator
PTF	program temporary fix
PTT	Post, Telephone and Telegraph (agency)
PTX	phototransistor
PU	physical unit
PUC	processor unit card (mpdels 31x and 61x)
PUC1	processor unit card type 1 (models 21A and 41A starting EC D55657)
PV	parity valid (signal)
QAM	quadrature amplitude modulation
RA	repair action
RAC	repair action code
RAS	reliability, availability, and serviceability
RC	receive clock
RCDB	reference code data base
RCV	receive
RD	receive data (signal)
RDB	reference code data base
RECFMS	record formatted maintenance statistics

RECMS record maintenance statistics

REQMS request for maintenance statistics

RETAIN Remote Technical Assistance Information Network

RFS ready for sending (signal) (or clear to send CTS)

RH request/response header

RI 1) register to immediate operand (instruction)
2) ring indicator (same as CI)

RIM request initialization mode (SDLC)

RLSD receive line signal detector

RNIO OS/VS VTAM IO trace

ROK read-only key

ROS read-only storage

ROSAR read-only storage address register

rpm revolutions per minute

RPO 1) remote power-off
2) request power-off

RPQ request for price quotation

RR register-to-register (instruction)

RS register-to-storage (instruction)

RSA register-to-storage with addition (instruction)

RSET receive signal element timing (same as RC)

RSF remote support facility

RTC retry count (X.21)

RTM retry timer (X.21)

RTS request to send (signal)

RU request/response unit (SNA)

RVI reverse interrupt (BSC)

R/W read/write

s second

SAC storage and control board assembly

SACL storage and control lower assembly for 3745 models 21x and 41x

SACU storage and control upper assembly for 3745 models 21x and 41x

SACL2 storage and control lower assembly for 3745 models 31x and 61x

SACU2 storage and control upper assembly for 3745 models 31x and 61x

SALT stand-alone link test

SAR storage address register

SAT specific assurance test

SCB scanner control block (storage)

SCF secondary control field (storage)

SCP signal converter product (or DCE)

SCR 1) subtract character register (instruction)
2) serial clock receive (signal)

SCT serial clock transmit (signal)

SCTL storage control card for 3745 models 21A and 41A

SCTL2 storage control card for 3745 models 31x and 61x

SCTL3 storage control card for 3745 models 31A and 61A

SD send data (signal)

SDF serial data field (storage)

SDLC Synchronous Data Link Control

SE system engineer

SES secondary status (storage)

SET signal element timing (signal)

SHM short hold mode

SHR subtract halfword register (instruction)

SI select in

SIDI serial in data in

SIM set initialization mode (SDLC)

SIO start input/output

SIT scanner interface trace

SKA storage key address

SKDR storage-protect key data register

SL serial link

SMPS switching module power supply

SMUXA single multiplex card for lower board on LIC 2

SMUXB single multiplex card for upper board on LIC 2

SNA Systems Network Architecture

SNRM set normal response mode (SDLC)

SO select out

SODO serial out data out

SOH start of heading (BSC)

SP storage protect

SPAE storage protect/ address exception

SPDn signal and power distribution card

SPK storage protect key

SPS service and power support

SR subtract register (instruction)

SRC system reference code

SRI subtract register immediate (instruction)

SRL shift register latch

SS start-stop

SSA system services architecture

SSB system status block

SSCP system services control point

SSP system support programs

ST store (instruction)

STAT0 status 0 register

STAT1 status 1 register

STAT4 status 4 register

STC store character (instruction)

STCT store character and count (instruction)

STER switch terminator

STH store halfword (instruction)

STG storage

STO storage (card)

STX start of text (BSC)

SVC supervisor call

SW switch

SWAD MOSS/SWL adapter

SWER switch error register

SWL switching logic

SWLA switching logic A

SWLB switching logic B

SYN synchronous idle (BSC)

SYSGEN system generation

T transmit (signal)

TA tag address

TAP trace analysis program

TAR temporary address register

TB terminator block

TC transmit clock

TCAM Telecommunications Access Method

TCB task control block

TCC trace correlation counter (storage)

TCM 1) thermal conduction module
2) treillis coded modulation

TCP test connector pin

TCS two-channel switch

TCTR transient error counter

TD 1) tag data
2) transmitted data (signal)

TERM terminator

TG transmission group

TH transmission header

TI test indicator (signal)

TIC token-ring interface coupler

TIC1 token-ring interface coupler type 1 (card)

TIC2 token-ring interface coupler type 2 (card)

TICB trace interface control block

TIO test I/O

TLNVT trace line vector table

TOD time of day

TPF transaction process facility

TPS two-processor switch

TPSA trace parameter status area

TRA token-ring adapter

TRM 1) token-ring multiplexer card that controls up to two TICs
2) test register under mask (instruction)

TRP token-ring processor

TRSS token-ring subsystem

TRU trace record unit

TSET transmitter signal element timing (signal, same as TC)

TSS transmission subsystem

TSSB FRU name for LA board (basic) with no TRA adapters

TSST FRU name for LA board (basic) with TRA adapters

TTA translate table area

TTD temporary text delay (BSC)

T1 US service for very high speed transmissions at 1.5 million bps

UA unnumbered acknowledgment (SDLC)

UC universal controller

UCW unit control word

UE unit exception (channel status)

UEPO unit emergency power-off

UK United Kingdom

UKA user key address

UKP user key program

UKDR user key data register

UKL user key level interrupt

URSF universal remote support facility

USASCII (see *ASCII*)

μs microsecond

uv undervoltage

V volt

VB valid byte (signal)

VAC volts, alternating current

VCNA VTAM node control application

VDC volts, direct current

VFO variable frequency oscillator

VH valid halfword (signal)

VPD vital product data

VRC vertical redundancy check

VS virtual storage

VSE Virtual Storage Extended

VTAM Virtual Telecommunications Access Method

V.24 CCITT V.24 recommendation

V.25 CCITT V.25 recommendation

V.28 CCITT V.28 recommendation

V.35 CCITT V.35 recommendation

W watt

WACK wait before transmit positive acknowledgment (BSC)

WB wrapback (signal)

WLOB wire lobe (cable connecting token-ring adapters to token-ring access units)

WKR work register

WSDR wide storage data register

XI X.25 SNA interconnection

XID exchange identification

XCR exclusive OR character register (instruction)

XHR exclusive OR halfword register (instruction)

XOR exclusive OR

XR exclusive OR register (instruction)

XREG external registers

XRI exclusive OR register immediate (instruction)

X.21 CCITT X.21 recommendation

X.25 CCITT X.25 recommendation

YZxxx wiring diagram

ZI zero insert

ZREG Z register

Glossary

This glossary defines all new terms used in this manual. It also includes terms and definitions from the *IBM Dictionary of Computing,* GC20-1699.

adapter-initiated operation (AIO). A transfer of up to 256 bytes between an adapter (CA or LA) and the CCU storage. The transfer is initiated by an IOH/IOHI instruction, and is performed in cycle stealing via the IOC bus.

addressing. A technique where the control station selects, among the DTEs that share a transmission line, the DTE to which it is going to send a message.

alarm. A message sent to the MOSS console. In case of an error a reference code identifies the nature of the error.

alert. A message sent to the host console. In case of an error a reference code identifies the nature of the error.

asynchronous transmission. Transmission in which each character is individually synchronized, usually by the use of start and stop elements. The start-stop link protocol, for example, uses asynchronous transmission. Contrast with *synchronous transmission*.

auto-answer. A machine feature that allows a DCE to respond automatically to a call that it receives over a switched line.

auto-call. A machine feature that allows a DCE to initiate a call automatically over a switched line.

autoBER. A program to automatically analyse a BER file.

automaint. A function that uses autoBER to isolate failing FRUs.

availability. The degree to which a system or resource is ready when needed to process data.

buffer chaining channel adapter (BCCA). A channel adapter that handles buffer chaining in write channel program and both buffer chaining and PIU chaining in read channel program. BCCA works only under NCP.

Bell 212A. Bell recommendations on transmission interface

binary synchronous communication (BSC). A uniform procedure, using standardized set of control characters and character sequences, for synchronous transmission of binary-coded data between stations.

box event record (BER). Information about an event detected by the controller. It is recorded on the disk/diskette and can be displayed on the operator console for event analysis.

block multiplexer channel. A multiplexer channel that interleaves blocks of data. See also *byte multiplexer channel*. Contrast with *selector channel*.

byte multiplexer channel. A multiplexer channel that interleaves bytes of data. See also *block multiplexer channel*. Contrast with *selector channel*.

cache. A high-speed buffer storage that contains frequently accessed instructions and data; it is used to reduce access time.

central control unit (CCU). In the 3745, the controller hardware unit that contains the circuits and data flow paths needed to execute instructions and to control its storage and the attached adapters.

channel. A one-way path between a host and the controller.

channel adapter (CA). A communication controller hardware unit used to attach the controller to a host processor.

channel interface. The interface between the controller and the host processors.

clear channel. Mode of data transmission where the data passes through the DCE and network, and arrives at the receiving communication controller (for example, the IBM 3745) unchanged from the data transmitted. The DCE or network can modify the data during transmission because of certain network restrictions, but must ensure the received data stream is the same as the transmitted data stream.

command list. In NetView, a sequential list of commands and control statements that is assigned a name. When the name is invoked (as a command) the commands in the list are executed.

communication common carrier. In the USA and Canada, a public data transmission service that provides the general public with transmission service facilities. For example, a telephone or telegraph company (see also *Post Telephone and Telegraph* for countries outside the USA and Canada).

communication controller. A communication control unit that is controlled by one or more programs stored and executed in the unit. Examples are the IBM 3705, IBM 3725/3726, IBM 3720, and IBM 3745.

communication network management (CNM) application program. An ACF/VTAM application program authorized to issue formatted management services request units containing physical-unit-related requests and to receive formatted management services request units containing information from physical units.

communication scanner. See *scanner*.

communication scanner processor (CSP). The processor of a scanner.

common customer profile facility (CCPF). It is used to create customer profile records for new IBM customers. The records then form the customer profile library, which includes the customer's data processing site, machines and programs used, IBM branch, region, and support center servicing.

communication subsystem. The part of the controller that controls the data transfers over the transmission interface.

configuration data file (CDF). A MOSS file that contains a description of all the hardware features (presence, type, address, and characteristics).

control panel. A panel that contains switches and indicators for the use of the customer's operator and service personnel.

control program. A computer program designed to schedule and to supervise the execution of programs of the controller.

control subsystem (CSS). The part of the controller that stores and executes the control program, and monitors the data transfers over the channel and transmission interfaces.

customer engineer (CE). See *IBM service representative*

cyclic redundancy check. A system of error checking performed at both the sending and receiving station after a block check character has been accumulated.

cyclic redundancy check character (CRC). A character used in a modified cyclic code for error detection and correction.

data circuit-terminating equipment (DCE). The equipment installed at the user's premises that provides all the functions required to establish, maintain, and terminate a connection, and the signal conversion and coding between the data terminal equipment (DTE) and the line. For example, a modem is a DCE (see *modem*.)

Note: The DCE may be separate equipment or an integral part of other equipment.

data communication channel. See *channel*.

data host. A host running application programs only.

data terminal equipment (DTE). That part of a data station that serves as a data source, data sink, or both, and provides for the data communication control function according to protocols.

DIN. Technology of connector contacts.

direct attachment. The attachment of a DTE to another DTE without a DCE.

direct-current interlock (DCI). A mode of data transfer over an I/O interface to enable communication between data processing systems through a channel.

diskette. A thin, flexible magnetic disk, and its protective jacket, that records diagnostics, microcode, and 3745 files.

diskette drive. A mechanism that reads and writes diskettes.

DOS/VS. Disk Operating System/Virtual Storage.

duplex transmission. Data transmission in both directions at the same time. Contrast with *half-duplex*.

Emulation Program (EP). An IBM licensed program that allows a channel-attached communication controller to emulate the functions of an IBM 2701 Data Adapter Unit, an IBM 2702 Transmission Control, or an IBM 2703 Transmission Control.

error recovery procedure (ERP). A procedure designed to help isolate and, where possible, to recover from errors in equipment. The procedures are often used in conjunction with programs that record the information on machine malfunctions.

Ethernet line adapter (ELA). Ethernet-type LAN line adapter composed of a CSP card and an EAC card.

Ethernet subsystem (ESS). The part of the controller that controls the data transfers over the Ethernet-type LAN.

The ESS consists of up to eight Ethernet line adapters (ELAs).

fallback. In twin-backup mode, a state where the traffic of the failing CCU has been redirected to the second one.

In standby mode, a state where the traffic of the failing CCU has been redirected to the standby CCU after it is IPLed.

front-end scanner (FES). A circuit that scans the transmission lines, serializes and deserializes the transmitted characters, and manages the line services. It is part of the scanner.

half-duplex. Data transmission in either direction, one direction at a time. Contrast with *duplex*.

high-performance transmission subsystem (HPTSS). The part of the controller that controls the data transfers over the high-speed transmission interface (speed up to 2 million bps).

The HPTSS consists of up to eight high-speed scanners (HSSs).

high-speed scanner. Line adapter for lines up to 2 million bps, composed of a communication scanner processor (CSP) and a front-end high-speed scanner (FESH).

high-speed transfer. A mode of high-speed data transmission over an I/O interface to enable communication between data processing systems through a channel.

hit. In cache operation, indicates that the information is in the cache storage.

host processor. 1) A processor that controls all or part of a user application netwo rk. 2) In a network, the processing unit in which the access method for the network resides. (3) In an SNA network, the processing unit that contains a system services control point (SSCP). (4) A processing unit that executes the access method for attached communication controllers. Also called *host.*

IBM service representative. An individual in IBM who performs maintenance services for IBM products or systems.

initial microcode load (IML). The process of loading the microcode into a scanner or into MOSS.

initial program load (IPL). The initialization procedure that causes 3745 control program to commence operation.

input/output control (IOC). The circuit that controls the input/output from/to the channel adapters and scanners via the IOC bus.

internal clock function. A LIC function that provides a transmit clock for sending data, and retrieves a receive clock from received data, when the modem does not provide those timing signals. When the terminal is connected in direct-attach mode (without modem) the ICF also provides the transmit and receive clocks to the terminal, via the LIC card.

internal function test (IFT). A set of diagnostic programs designed and organized to detect and isolate a malfunction.

LIC module. A group of four adjacent LICs.

LIC unit. A line interface coupler unit (LIU) consisting of:

- One power supply (PS) associated with
- Two LIC boards (LIBs), housing
- Multiplex cards (DMUX, SMUXA, or SMUXB), and
- Line interface coupler cards (LICs)

line. See *transmission line*.

line adapter (LA). The part of the TSS, HPTSS, or TRSS that scans and controls the transmission lines. Also called *scanner*.

For the TSS the line adapters are low-speed scanners (LSSs).

For the HPTSS the line adapters are high-speed scanners (HSSs).

For the TRSS the line adapters are token-ring adapters (TRAs).

line interface coupler (LIC). A circuit that attaches up to four transmission cables to the controller.

Link Problem Determination Aid (LPDA). A set of test facilities resident in the IBM 386X/586X modems and activated from the control program in the controller and from host.

link protocol. The set of rules by which a logical data link is established, maintained, and terminated, and by which data is transferred across the link.

Logrec. Error logging program managed via the operating system.

longitudinal redundancy check (LRC). A system of error checking performed at the receiving station after a block check character has been accumulated.

low-speed scanner. Line adapter for lines up to 256 kbps, composed of a communication scanner processor (CSP) and a front-end low-speed scanner (FESL).

maintenance and operator subsystem (MOSS). The part of the controller that provides operating and servicing facilities to the customer's operator and the IBM service representative.

microcode. A program, that is loaded in a processor (for example, the MOSS processor) to replace a hardware function. The microcode is not accessible to the customer.

miss. In cache operation, indicates that the information is not in the cache storage.

modem (modulator-demodulator). A functional unit that transforms logical signals from a DTE into analog signals suitable for transmission over telephone lines (modulation), and conversely (demodulation). A modem is a DCE. It may be integrated in the DTE.

MOSS input/output control (MIOC). The circuit that controls the input/output from/to the MOSS.

multiplexer channel. A channel designed to operate with a number of I/O devices simultaneously. Several I/O devices can transfer records at the same time by interleaving items of data. See also *byte multiplexer, block multiplexer*.

multiplexing. In data transmission, a function that permits two or more data sources to share a common transmission medium so that each data source has its own channel.

multipoint connection. A connection established for data transmission among more than two data stations. The connection may include switching facilities.

NetView. An IBM licensed program used to monitor a network, manage it, and diagnose its problems.

network. See *user application network*.

Network Control Program (NCP). An IBM licensed program that provides communication controller support for single-domain, multiple-domain, and interconnected network capability.

nonswitched line. A connection between systems or devices that does not have to be made by dialing. The connection can be point-to-point or multipoint. The line can be leased or private. Contrast with *switched line.*

online tests. Testing of a remote data station concurrently with the execution of the user's programs (that is, with only minimal effect on the user's normal operation).

Operating System/Virtual Storage (OS/VS). A family of operating systems that control IBM System/360 and System/370 computing systems. OS/VS includes VS1, VS2, MVS/370, and MVS/XA:

operator console. The IBM Operator Console that is used to operate and service the 3745 through the MOSS. A local console must be located within 7 m of the 3745. Optionally an alternate console may be installed up to 120 m from the 3745, or a remote console may be connected to the 3745 through the switched network.

owning host. A host which can IPL a 3745 and also run application programs.

partitioned emulation programming (PEP) extension. A function of a network control program that enables a communication controller to operate some telecommunication lines in network control mode while simultaneously operating others in emulation mode.

phototransistor. An electronic part used to sense the light of a light-emitting diode.

point-to-point connection. A connection established between two data stations for data transmission. The connection may include switching facilities.

polling. The process whereby remote stations are invited, one at a time, to transmit.

post telephone and telegraph (PTT). A generic term for the government-operated common carriers in countries other than the USA and Canada. Examples of the PTT are British Telecom in the United Kingdom, Deutsche Bundespost in Germany, and Nippon Telephone and Telegraph Public Corporation in Japan.

program-initiated operation (PIO). A transfer of four bytes between a general register in the CCU and an adapter (channel or scanner). The transfer is initiated by IOH/IOHI instruction and is executed via the IOC bus.

reliability. The ability of a functional unit to perform a required function under stated conditions, for a stated period of time.

scanner. A device that scans and controls the transmission lines. Also called *line adapter*.

selector channel. An I/O channel designed to operate with only one I/O device at a time. Once the I/O device is selected, a complete record is transferred one byte at a time. Contrast with *block multiplexer channel, multiplexer channel*.

services. A set of functions designed to facilitate the maintenance of a device or system.

serviceability. The capability to perform effective problem determination, diagnosis, and repair on a data processing system.

single. Configuration with one CCU

start-stop. A data transmission system in which each character is preceded by a start signal and is followed by a stop signal.

switchback. Operation to reset a twin-backup configuration from fallback to initial state.

switched line. A transmission line with which the connections are established by dialing, only when data transmission is needed. The connection is point-to-point and uses a different transmission line each time it is established. Contrast with *nonswitched line*.

Synchronous Data Link Control (SDLC). A discipline conforming to subsets of the Advanced Data Communication Control Procedures (ADCCP) of the American National Standards Institute (ANSI) and High-level Data Link Control of the International Organization for Standardization, for managing synchronous, code-transparent, serial-by-bit information transfer over a link connection. Transmission exchanges may be duplex or half-duplex over switched or nonswitched links. The configuration of the link connection may be point-to-point, multipoint, or loop.

synchronous transmission. Data transmission in which the sending and receiving instruments are operating continuously at substantially the same frequency and are maintained, by means of correction, in a desired phase relationship. Contrast with *asynchronous transmission*.

Systems Network Architecture (SNA). The description of the logical structure, formats, protocols, and operational sequences for transmitting information through a user application network. The structure of SNA allows the users to be independent of specific telecommunication facilities.

time out. The time interval allotted for certain operations to occur.

token-ring subsystem (TRSS). The part of the controller that controls the data transfers over an IBM Token-Ring Network.

The TRSS consists of up to four token-ring adapters (TRAs).

token-ring adapter (TRA). Line adapter for an IBM Token-Ring Network, composed of one token-ring multiplexer card (TRM), and two token-ring interface couplers (TICs).

The TRSS consists of up to four token-ring adapters (TRAs).

transmission interface. The interface between the controller and the user application network.

transmission line. The physical means for connecting two or more DTEs (via DCEs). It can be nonswitched or switched. Also called *line*.

transmission subsystem (TSS). The part of the controller that controls the data transfers over low- and medium-speed, switched and non switched transmission interfaces.

The TSS consists of:

- Up to 32 low-speed scanners (LSSs) associated with
- LIC units (LIUs), through
- Serial links (SLs).

TSST board. line adapter board for token-ring adapters

twin. Configuration with two CCUs.

twin-dual. Mode of operation with two CCUs operating simultaneously in two distinct subareas.

twin-backup. Mode of operation identical to twin-dual with fallback capability.

twin-standby. Mode of operation with one CCU active and the other in standby, ready to take over.

two-processor switch (TPS). A feature of the channel adapter that connects a second channel to the same adapter.

user application network. A configuration of data processing products, such as processors, controllers, and terminals, for the purpose of data processing and information exchange. This configuration may use circuit-switched, packet-switched, and leased-circuit services provided by carriers or the PTT. Also called *user network*.

vertical redundancy check (VRC). An odd parity check performed on each character of a block as the block is received.

V.24. CCITT V.24 recommendation

V.25. CCITT V.25 recommendation

V.28. CCITT V.28 recommendation

V.35. CCITT V.35 recommendation

X.20. CCITT X.20 recommendation

X.21. CCITT X.21 recommendation

X.21 bis. CCITT X.21 bis recommendation

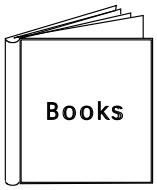
X.25. CCITT X.25 recommendation

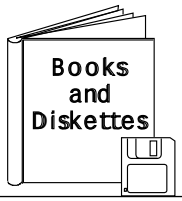
Bibliography

Customer Documentation for the 3745 (Models 210, 21A, 310, 31A, 410, 41A, 610, and 61A) and 3746 (Model 900)

Table X-1 (Page 1 of 4). Customer Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

This customer documentation has the following formats:

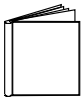




Finding Information

3745 Models A and 3746 Books

Starting with engineering change (EC) F12380, all of the books in the 3745 Models A and 3746 library are available on the CD-ROM that contains the Licensed Internal Code (LIC) for this EC.



SA33-0172

IBM 3745 Communication Controller
Models 210 to 61A
IBM 3746 Expansion Unit Model 900

Customer Master Index[1]

Provides references for finding information in the customer documentation library.

Evaluating and Configuring

GA33-0092

IBM 3745 Communication Controller
Models 210, 310, 410, and 610

Introduction

Gives an introduction about the IBM Models 210 to 610 capabilities.

For Models A refer to the *Overview*, GA33-0180.

GA33-0180

IBM 3745 Communication Controller Models A[2]
IBM 3746 Nways Multiprotocol Controller
Models 900 and 950

Overview

Gives an overview of connectivity capabilities within SNA, APPN, and IP networking.

Table X-1 (Page 2 of 4). Customer Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

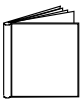
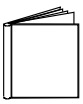
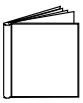
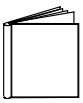
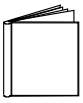
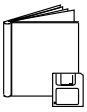
	GA33-0457	***IBM 3745 Communication Controller Models A***[2] ***IBM 3746 Expansion Unit Model 900*** ***Models 900 and 950*** ***Planning Guide*** Planning for: • Field upgrades • Service processor and alert management configuration • Network integration (NCP, APPN, and IP control) • Physical installation.
Preparing Your Site		
	GC22-7064	***IBM System/360, System/370, 4300 Processor*** ***Input/Output Equipment Installation Manual-Physical Planning*** (Including Technical News Letter GN22-5490) Provides information for physical installation for the 3745 Models 130 to 610. For 3745 Models A and 3746 Model 900, refer to the *Planning Guide*, GA33-0457.
	GA33-0127	***IBM 3745 Communication Controller*** ***Models 210, 310, 410, and 610*** ***Preparing for Connection*** Helps for preparing the 3745 Models 210 to 610 cable installation. For 3745 Models A refer to the *Connection and Integration Guide*, SA33-0129.
Preparing for Operation		
	GA33-0400	***IBM 3745 Communication Controller All Models***[3] ***IBM 3746 Nways Multiprotocol Controller*** ***Models 900 and 950*** ***Safety Information***[1] Provides general safety guidelines.
	SA33-0129	***IBM 3745 Communication Controller All Models***[3] ***IBM 3746 Nways Multiprotocol Controller Model 900*** ***Connection and Integration Guide***[1] Contains information for connecting hardware and integrating network of the 3745 and 3746-900 after installation.
	SA33-0416	***Line Interface Coupler Type 5 and Type 6*** ***Portable Keypad Display*** ***Migration and Integration Guide*** Contains information for moving and testing LIC types 5 and 6.
	SA33-0158	***IBM 3745 Communication Controller All Models***[3] ***IBM 3746 Nways Multiprotocol Model 900*** ***Console Setup Guide***[1] Provides information for: • Installing local, alternate, or remote consoles for 3745 Models 130 to 610 • Configuring user workstations to remotely control the service processor for 3745 Models A and 3746 Model 900 using: – DCAF program – Telnet Client program.
Customizing Your Control Program		

Table X-1 (Page 3 of 4). Customer Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

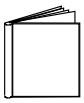
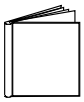
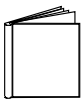
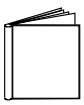
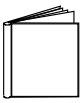
	SA33-0178	***Guide to Timed IPL and Rename Load Module*** Provides VTAM procedures for: • Scheduling an automatic reload of the 3745 • Getting 3745 load module changes transparent to the operations staff.
Operating and Testing		
	SA33-0098	***IBM 3745 Communication Controller*** ***All Models***[4] ***Basic Operations Guide***[1] Provides instructions for daily routine operations on the 3745 Models 130 to 610.
	SA33-0177	***IBM 3745 Communication Controller Models A***[2] ***IBM 3746 Nways Multiprotocol Controller Model 900*** ***Basic Operations Guide***[1] Provides instructions for daily routine operations on the 3745 Models 17A to 61A, and 3746 Model 900 operating as an SNA node (using NCP), APPN/HPR Network Node and IP Router.
	SA33-0097	***IBM 3745 Communication Controller*** ***All Models***[3] ***Advanced Operations Guide***[1] Provides instructions for advanced operations and testing, using the 3745 MOSS console.
	On-line Information	***Controller Configuration and Management Application*** Provides a graphical user interface for configuring and managing a 3746 APPN/HPR Network Node and IP Router, and its resources. Is also available as a stand-alone application, using an OS/2 workstation. Defines and explains all the 3746 Network Node and IP Router configuration parameters through its on-line help.
	SH11-3081	***IBM 3746 Nways Multiprotocol Controller*** ***Models 900 and 950*** ***Controller Configuration and Management: User's Guide***[5] Explains how to use CCM and gives examples of the configuration process.
Managing Problems		
	SA33-0096	***IBM 3745 Communication Controller*** ***All Models***[3] ***Problem Determination Guide***[1] A guide to perform problem determination on the 3745 Models 130 to 61A.
	On-line Information	***Problem Analysis Guide*** An on-line guide to analyze alarms, events, and control panel codes on: • IBM 3745 Communication Controller Models A[2] • IBM 3746 Nways Multiprotocol Controller Models 900 and 950.

Table X-1 (Page 4 of 4). Customer Documentation for the 3745 Models X10 and X1A, and 3746 Model 900



SA33-0175

IBM 3745 Communication Controller Models A[2]
IBM 3746 Expansion Unit Model 900
IBM 3746 Nways Multiprotocol Controller Model 950

Alert Reference Guide

Provides information about events or errors reported by alerts for:

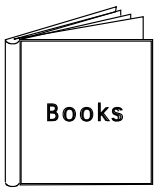
- IBM 3745 Communication Controller Models A[2]
- IBM 3746 Nways Multiprotocol Controller Models 900 and 950.

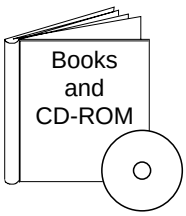
[1] Documentation shipped with the 3745.
[2] 3745 Models 17A to 61A.
[3] 3745 Models 130 to 61A.
[4] Except 3745 Models A.
[5] Documentation shipped with the 3746-900.

Service Documentation for the IBM 3745 (Models 210, 21A, 310, 31A, 410, 41A, 610, and 61A) and 3746 (Model 900)

Table X-2 (Page 1 of 4). Service Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

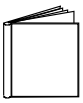
This service documentation has the following formats:





SY33-2080	***IBM 3745 Communication Controller Models 210 to 61A*** ***Service Master Index***[1] Provides references for finding information in the IBM 3745 Models X10 and X1A shipping group documentation.
SY33-2057	***IBM 3745 Communication Controller Models 210 to 61A*** ***Installation Guide***[1] Provides instructions for installing or relocating the IBM 3745 Models X10 and X1A.
SY33-2114	***IBM 3746 Nways Multiprotocol Controller Model 900*** ***Installation Guide***[2] Provides instructions for installing or relocating a 3746-900.
SY33-2116	***IBM 3746 Nways Multiprotocol Controller Model 900*** ***Service Guide***[2] Provides procedures for isolating and fixing the IBM 3746-900 problems.
SY33-2055	***IBM 3745 Communication Controller Models 210, 310, 410, and 610*** ***IBM 3746 Expansion Units Models A11, A12, L13, L14, and L15*** ***Service Functions***[1] Describes MOSS functions using the IBM 3745 Models X10 and X1A consoles.
SY33-2054	***IBM 3745 Communication Controller Models 210 to 61A*** ***Maintenance Information Procedures***[1] Provides procedures for isolating and fixing the IBM 3745 Models X10 and X1A problems.

Table X-2 (Page 2 of 4). Service Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

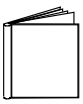


SY33-2115

***IBM 3745 Communication Controller Models A*[3]**
IBM 3746 Expansion Unit Model 900
IBM 3746 Nways Multiprotocol Controller Model 950

***Service Processor Installation and Maintenance*[4]**
(Based on the 7585, 3172, 9585, or 9577)

Provides information on installing and maintaining the service processor based on PS/2 Types 7585, 3172, 9585, or 9577.
Can be for systems with microcode that has up to and including EC D46130 (any level) installed.

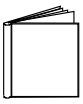


SY33-2120

***IBM 3745 Communication Controller Models A*[3]**
IBM 3746 Expansion Unit Model 900
IBM 3746 Nways Multiprotocol Controller Model 950

***Service Processor Installation and Maintenance*[4]**
(Based on the 7585, 3172, or 9585)

Provides information on installing and maintaining the service processor based on PS/2 Types 7585, 3172, or 9585.
Can be for systems with microcode EC F12380 or higher installed.

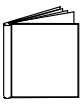


SY33-2118

IBM 3746 Nways Multiprotocol Controller Models 900 and 950

***Multiaccess Enclosure Installation and Maintenance*[4]**

Provides information on installing and maintaining the Multiaccess Enclosure (MAE).

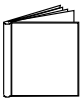


SY33-2112

IBM 3746 Nways Multiprotocol Controller
Models 900 and 950

***Network Node Processor Installation and Maintenance*[4]**
(Based on the 7585 or 3172)

Provides information on installing and maintaining the network node processor based on the PS/2 Type 7585 or 3172.

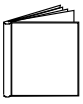


SY33-2056

IBM 3745 Communication Controller
Models 210 to 61A

***Maintenance Information Reference*[1]**

Provides in-depth hardware reference information on the IBM 3745 Models X10 and X1A.

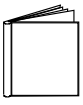


SY33-2075

IBM 3745 Communication Controller
***All Models*[6]**

***External Cable References*[1]**

Provides references to console and line cables used for connecting the IBM 3745 Models 130 to 61A.



SY33-2117

IBM 3746 Nways Multiprotocol Controller
Models 900 and 950

***External Cable Reference*[7]**

Provides references to console and line cables used for connecting the IBM 3746 Models 900 and 950.

Table X-2 (Page 3 of 4). Service Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

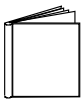
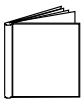
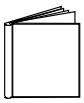
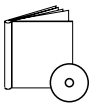
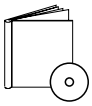
	S135-2015	***IBM 3746 Nways Multiprotocol Controller Models 900 and 950*** ***Parts Catalog***[7] Provides reference information for ordering parts for the IBM 3746 Models 900 and 950.
	S135-2010	***IBM 3745 Communication Controller Models 210 to 61A*** ***Parts Catalog***[1] Provides reference information for ordering IBM 3745 Models X10 and X1A parts.
	S135-2014	***IBM Controller Expansion*** ***Parts Catalog*** Provides reference information for ordering parts for the controller expansion attached to the IBM 3745 Models A[3], and 3746 Models 900 and 950.

Table X-2 (Page 4 of 4). Service Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

CD-ROM Bibliography		
	ZK2T-8214	***IBM Networking*** ***Softcopy Collection Kit*** Allows service manuals consulting via CD-ROM viewer. EMEA version.
	ZK2T-8187	***IBM Networking*** ***Softcopy Collection Kit*** Allows service manuals consulting via CD-ROM viewer. US version.

[1] Documentation shipped with the 3745.
[2] Documentation shipped with the 3746-900.
[3] 3745 Models 17A to 61A.
[4] Documentation shipped with the processor.
[5] Product integrated information
[6] 3745 Models 130 to 61A.

Index

Numerics

A

B

C

D

E

F

G

H

I

K

L

M

N

O

P

R

S

T

U

V

W

X

Readers' Comments — We'd Like to Hear from You

IBM 3745 Communication Controller
Models 210 to 61A
Maintenance Information Reference
Part 1

Publication No. SY33-2056-8

Please send us your comments concerning this book. We will greatly appreciate them and will consider them for later releases of the present book.

If you prefer sending comments by FAX or electronically, use:

- FAX: 33 4 93 24 77 97
- E-mail: FRIBMQF5 at IBMMAIL
- IBM Internal Use: LGERCF at LGEPROFS
- Internet: rcf_lagaude@vnet.ibm.com

In advance, thank you.

Your comments:

Name

Address

Company or Organization

Phone No.

Readers' Comments — We'd Like to Hear from You
SY33-2056-8

Cut or Fold
Along Line

Fold and Tape | **Please do not staple** | Fold and Tape

PLACE
POSTAGE
STAMP
HERE

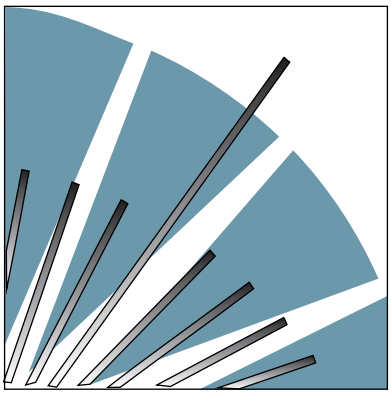
IBM France
Centre d'Etudes et Recherches
Service 0798 - BP 79
06610 La Gaude
France

Fold and Tape | **Please do not staple** | Fold and Tape

Cut or Fold
Along Line

Part Number: 26F1659

Printed in Denmark by IBM Danmark A/S



26F1659

SY33-2056-8